PHOENIX DISPLAY INTERNATIONAL, INC.

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SPECIFICATION FOR LCD MODULE

CUSTOMER	
PART NUMBER	PDIS070QWU142FN-FL150-GF
DESCRIPTION	7.0" Color TFT Display
VERSION	1.0
ISSUE DATE	2023.7.25

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Record of Revisions

Version	Revise Date	Description	Page
1.0	2023-7-25	First Release	-

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1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	7.0	inch
Number of Pixels	1200 (H) RGB x 1920 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	o' clock
Interface	MIPI	-
Display Colors	16.7M	colors
Outline Dimension	120.50 (H) x 183.20 (V) x 4.95 (D)	mm
Active Area	94.50 (H) x 151.20 (V)	mm
Pixel Pitch	0.07875 (H) x 0.07875 (V)	mm
Driver IC	FT8206	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Power Voltage	VSP	0	6.5	V	Note 1
	VSN	-6.5	-	V	Note 1
Digital supply voltage	IOVCC	-0.3	3.6	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

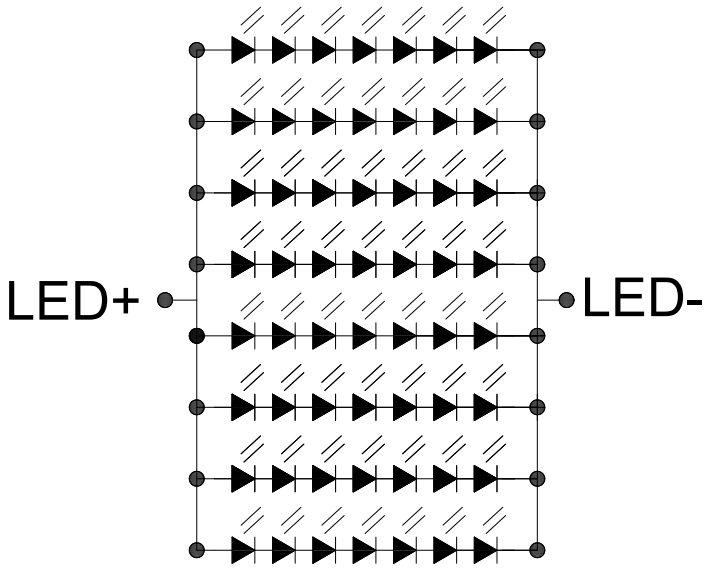
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Logic supply voltage	IOVCC	1.65	1.8	3.3	V	
Logic supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=1.8V
Power supply for LCD	VSP	5.3	5.5	5.7	V	
	VSN	-5.7	-5.5	-5.3	V	
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	240	400	mA	
Driving Voltage	V_F	18.9	-	23.8	V	
Power consumption	W_{BL}	4.536	-	9.52	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	IOVCC	-	1.8	-	V	
Analog supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=1.8V
Input high-level voltage	VIH	0.7*IOVCC	-	IOVCC	V	
Input low -level voltage	VIL	GND	-	0.3*IOVCC	V	

4. Interface Pin Assignment

4.1 LCM Pin Assignment

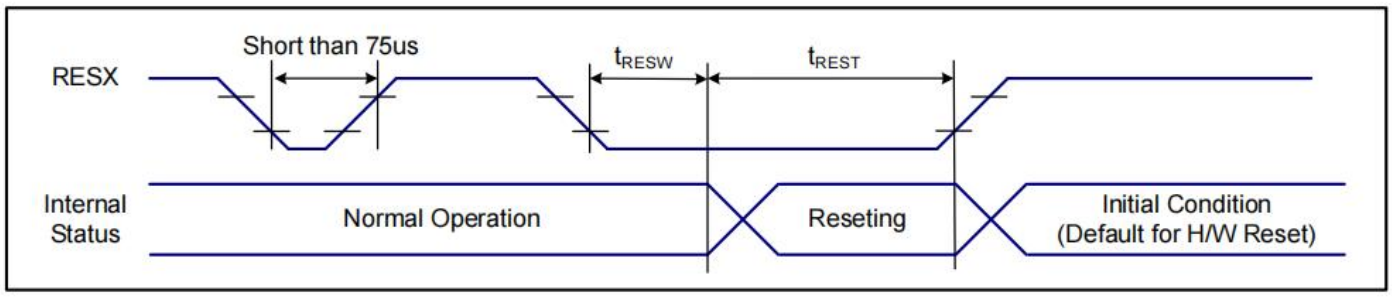
No.	Symbol	Description
1	NC	No connection
2-3	IOVCC	Power supply(1.8V)
4	GND	Ground
5	RESET	Global reset pin
6	TP_EXT_RSTN	Reset Pin for CTP
7	GND	Ground
8	MIPI_D0N	MIPI Negative data signal(-)
9	MIPI_D0P	MIPI Positive data signal(+)
10	GND	Ground
11	MIPI_D1N	MIPI Negative data signal(-)
12	MIPI_D1P	MIPI Positive data signal(+)
13	GND	Ground
14	MIPI_CKN	MIPI Negative clock signal(-)
15	MIPI_CKP	MIPI Positive clock signal(+)
16	GND	Ground
17	MIPI_D2N	MIPI Negative data signal(-)

18	MIPI_D2P	MIPI Positive data signal(+)
19	GND	Ground
20	MIPI_D3N	MIPI Negative data signal(-)
21	MIPI_D3P	MIPI Positive data signal(+)
22	GND	Ground
23-24	NC	No connection
25	GND	Ground
26	NC/TE	No connection
27	PWMO	The PWM frequency output for LCD driver control
28	NC/BIST	No connection
29	NC	No connection
30	GND	Ground
31	TP_I2C_SCL	I2C clock input for CTP
32	TP_I2C_SDA	I2C data input and output for CTP
33	TP_INT	Interrupt signal for CTP
34-35	VSN	Analog supply Negative voltage(5~6V)
36	NC	No connection
37-38	VSP	Analog supply positive voltage(5~6V)
39-40	NC	No connection

5. Interface Characteristics

5.1 Reset timing characteristics

RESW shorter than 75us, Reset will be rejected.



VSS=0V, VDDI = 1.65V ~ 1.95V, Ta = -30°C to 85°C

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse minimum width	150	-	-	Reset signal recognized	us
t_{REST}	*2) Reset complete time	5	-	120	Reset action complete	ms

Table: Reset input timing

Note 1. RESX low pulse that is too short does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 75us	Reset Rejected
Longer than 150us	Reset Recognized
Between 75us and 150us	Reset sequence starts (It depends on voltage and temperature condition.)

Note 2. Once Reset low pulse is recognized, system requires RESX remaining low for another 5ms to complete H/W reset.

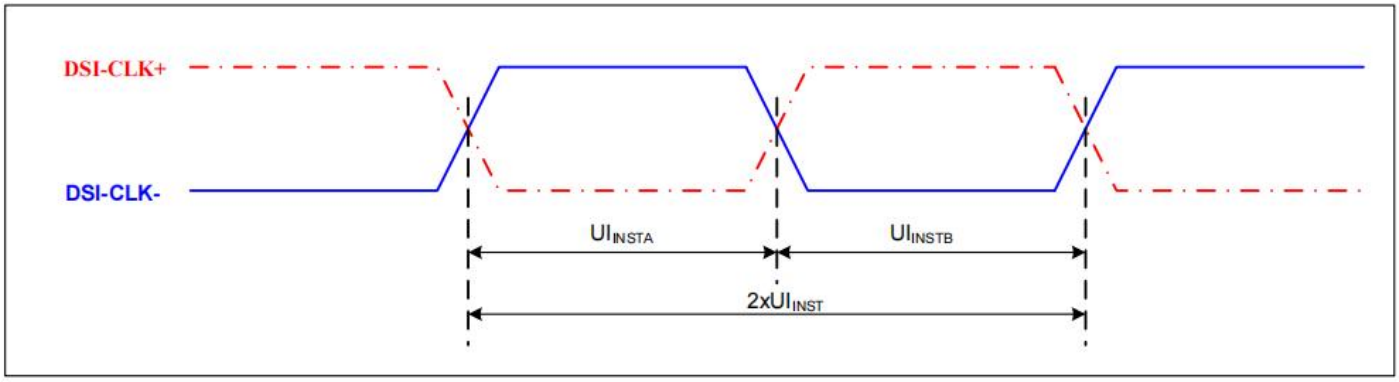
Note 3. During H/W Reset flow, ID0 ~ ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when H/W reset is complete ; The H/W reset sequence is complete when RESX is remaining low longer than tRESW + tREST.

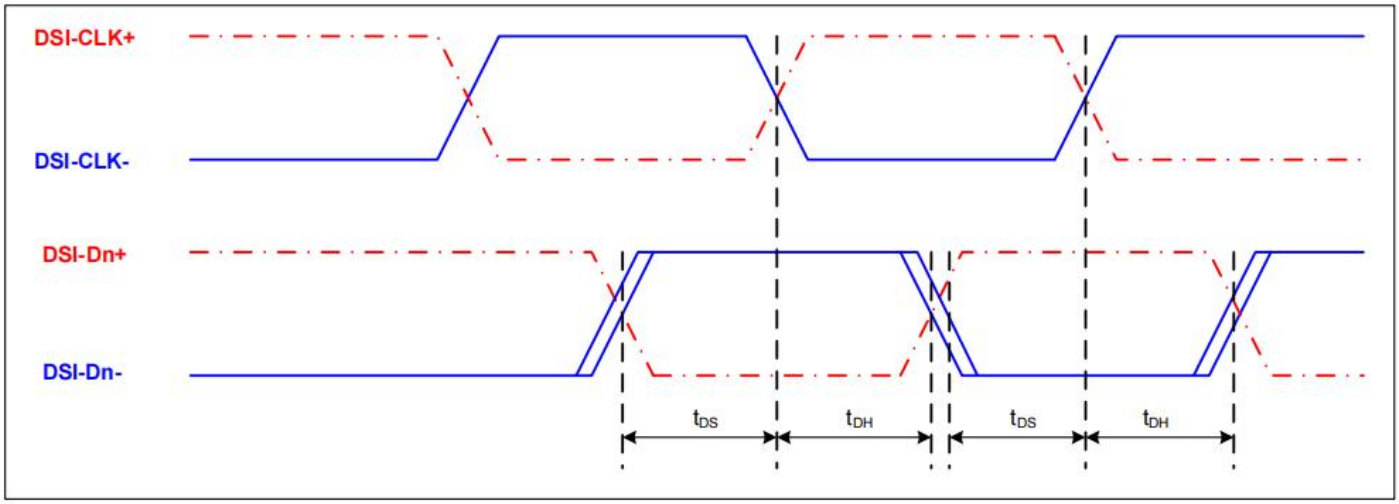
Note 4. It is necessary to wait 15msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

5.2 MIPI D-PHY AC characteristics

5.2.1 High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.54	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	0.77	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





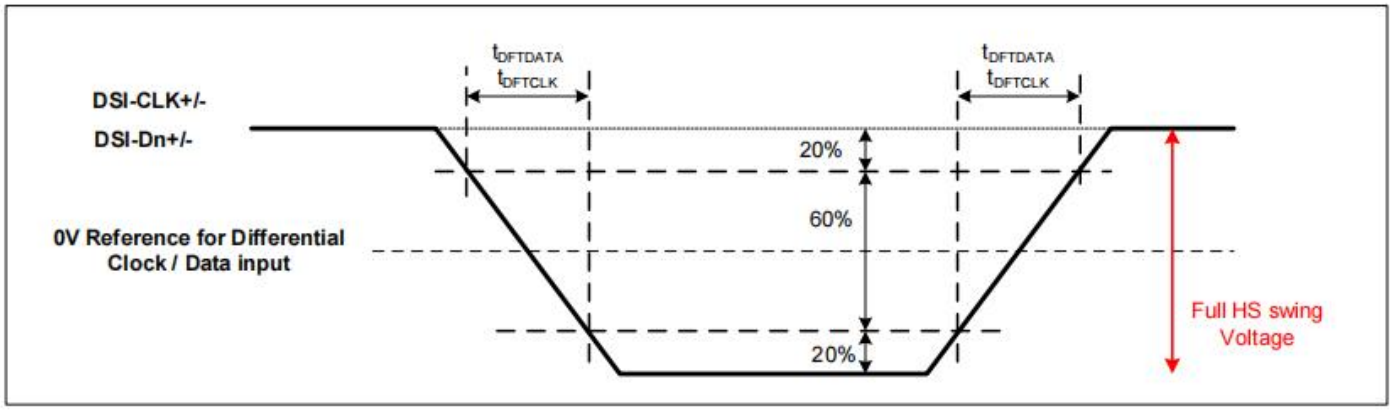


Figure: AC characteristics for MIPI-DSI High speed mode

5.2.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

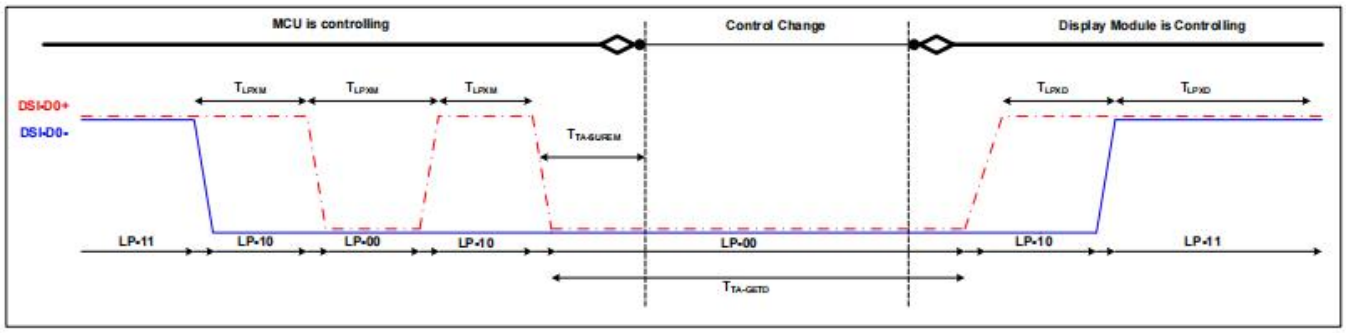


Figure: BTA from the MCU to the Display Module

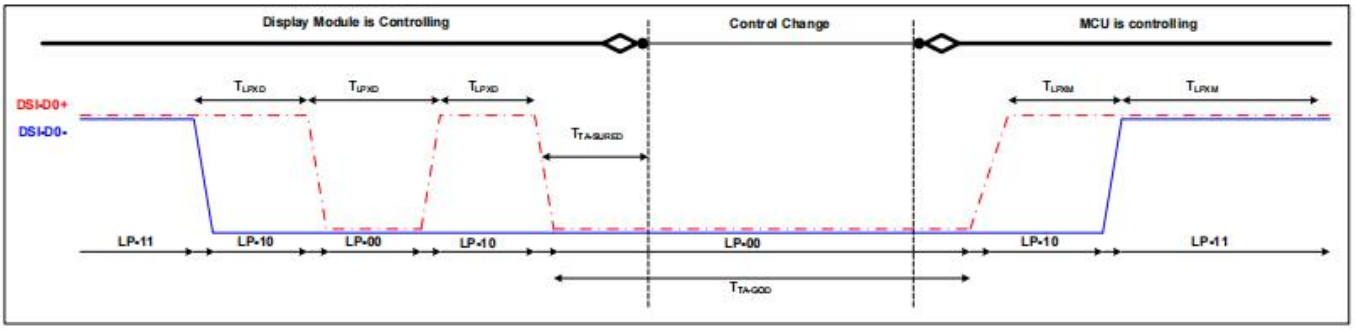
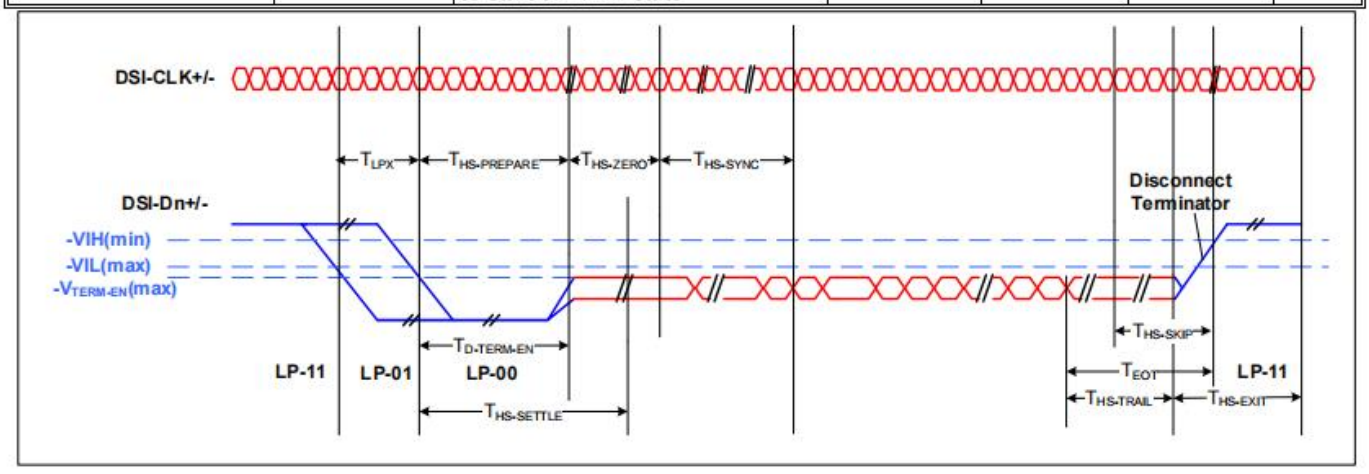


Figure: BTA from the Display Module to the MCU

5.2.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns



Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

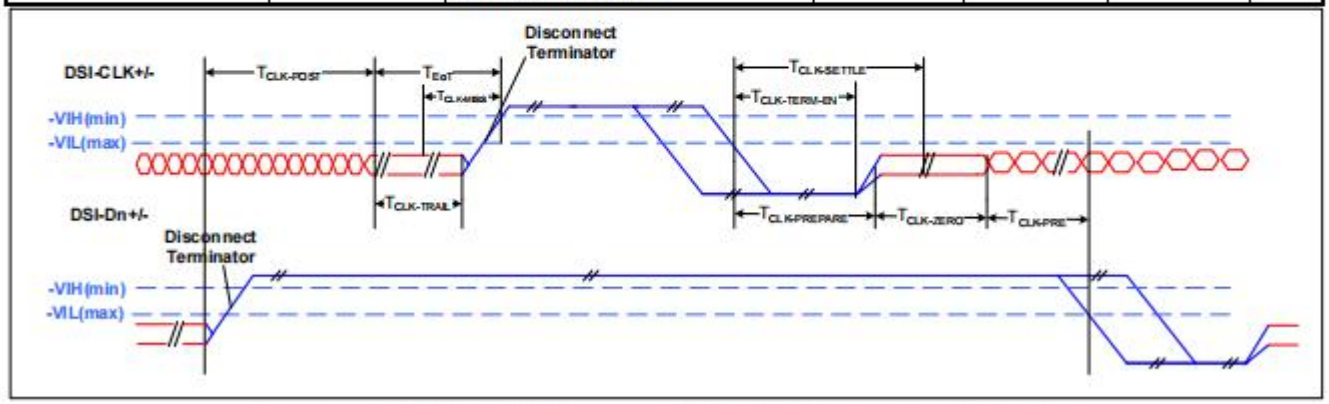


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

5.2.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

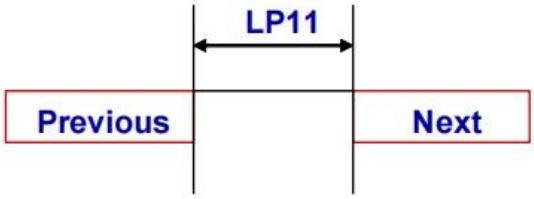
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-



5.3 MIPI C-PHY AC characteristics

5.3.1 C-PHY HS Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
$t_{UI-AVERAGE}$	UI average	1	0.833	-	12.5	ns
t_{MID-RX}	Data rate ≦1Gsps	-	$t_{UI-AVERAGE}$ – 1000ps			ps
	Data rate ≧1Gsps	-	0			-
$T_{EYE-RAMP-RX-LR}$	Eye ramp time at th reference channel output	-	-	-	250	ps
$T_{EYE-WIDTH-RX-LR}$	Eye width at th reference channel output	-	-	-	500+t_{MID-RX}	ps

Note:

1. Date rate range: 80Msps ~ 1.2Gsps.

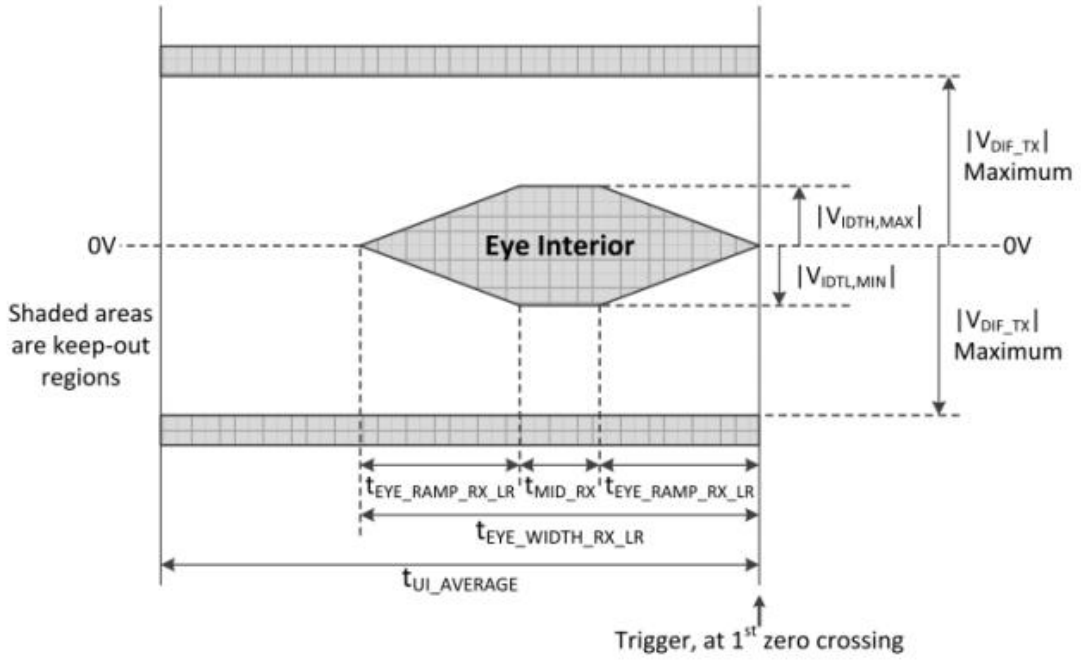


Figure: HS DATA Eye diagram at receiver

5.3.2 C-PHY LP Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX-M}	Transmitted length of any Low-Power state period (MCU)	-	50	-	-	ns
$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	-	T_{LPX-M}	-	$2*T_{LPX-M}$	ns
$T_{TA-GO-M}$	The display module drives the LP-00 before releasing MCU control	-	$4*T_{LPX-M}$			ns
$T_{TA-GET-M}$	The display drives the LP-00 after accepting control	-	$5*T_{LPX-M}$			ns
Ratio T_{LPX}	Ratio of (T_{LPX-M}/T_{LPX-D}) for driving overlap	-	2/3	-	3/2	
T_{LPX-D}	Transmitted length of any Low-Power state period (Display)	-	58	-	-	ns
$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	-	T_{LPX-D}	-	$2*T_{LPX-D}$	ns
$T_{TA-GO-D}$	The MCU drives the LP-00 before releasing Display control	-	$4*T_{LPX-D}$			ns
$T_{TA-GET-D}$	The MCU drives the LP-00 after accepting control	-	$5*T_{LPX-D}$			ns

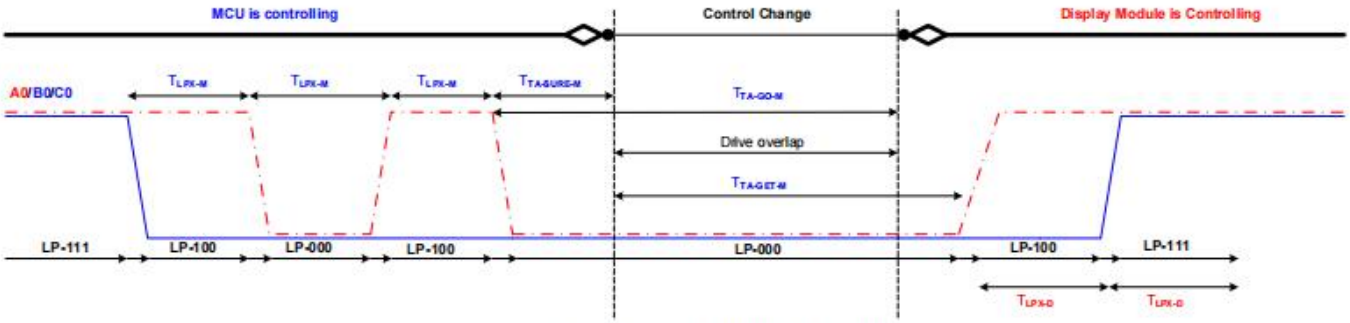


Figure: BTA from the MCU to the Display Module

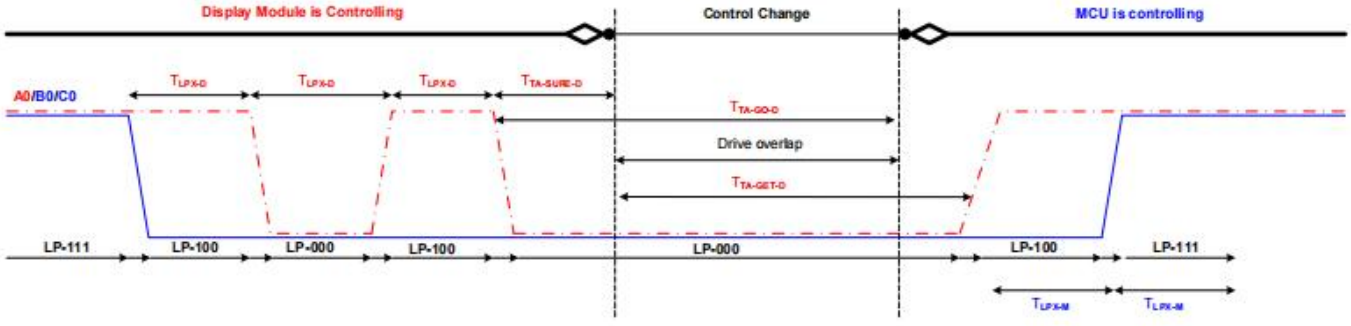


Figure: BTA from the Display Module to the MCU

5.3.3 C-PHY HSDT Bursts

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX}	Length of any LP state period	2	50	-	-	ns
$T_{3\text{-TERM-EN}}$	Time for the receiver to enable the HS line termination, starting from the time point when the A,B,C wrie cross $V_{IL\text{-MAX}}$	1,3	-	-	38	ns
$T_{3\text{-PREPARE}}$	Time that the transmitter drives the 3-wire LP-000 Line state immediately before the start of the HS Transmission	2	38		95	ns
$T_{3\text{-SETTLE}}$	Time interval during whith the HS receiver should ignore any HS transitions on the lane,starting from the beginning of $T_{3\text{-PREPARE}}$	3,4	$T_{3\text{-PREPARE}}$ +6UI	-	$T_{3\text{-PREPARE}}$ +$T_{3\text{-PREBEGIN}}$	ns
$T_{3\text{-PREBEGIN}}$	The length of the first part of the preamble	2,5	7	-	448	UI
$T_{3\text{-PROGSEQ}}$	The length of the programmable sequence section of the Preamble	2	0 or 14			UI
$T_{3\text{-PREEND}}$	The length of the end of the preamble	2	7			UI
$T_{3\text{-PREAMBLE}}$	The length of the entire preamble including $T_{3\text{-PREBEGIN}}$, $T_{3\text{-PROGSEQ}}$ and $T_{3\text{-PREEND}}$	2	$T_{3\text{-PREBEGIN}}$ + $T_{3\text{-PROGSEQ}}$ + $T_{3\text{-PREEND}}$			UI
$T_{3\text{-sync}}$	The length of the Sync Word	2	7			UI
$T_{3\text{-POST}}$	The length of the post-sequence at the end of the Burst	2,6	7	-	224	UI
$T_{HS\text{-EXIT}}$	Time that the transmitter drives LP-111 following a HS burst	2	100	-	-	ns

Note:

1. The receiver termination impedances shall not be enabled until the single-ended voltages on all of A,B and C fall below V_{TERM_EN}
2. Transmitter-specific parameter.
3. Receiver-specific parameter.
4. $T_{3\text{-SETTLE}}$ should end before the end of $T_{3\text{-PREBEGIN}}$ so the receiver's internal clock can run for a sufficient time to be able to initialize the PHY and protocol circuitry in the receiver.
5. $T_{3\text{-PREBEGIN}}$ should be adjustable at the transmitter from 7UI to 448UI in increments of 7UI.
6. $T_{3\text{-POST}}$ should adjustable at the transmitter from 7UI to 224UI in increments of 7UI.

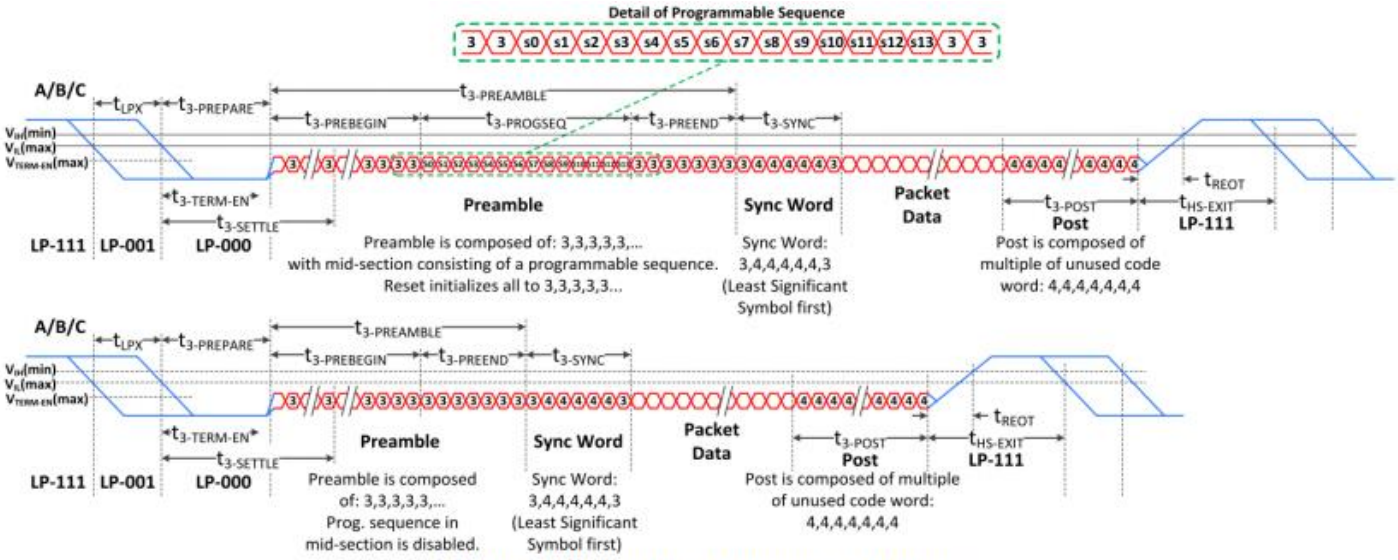


Figure: High Speed Data Transmission in Bursts

5.3.4 CPHY: LP-111 between High Speed and Low Power Modes

High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-111) when 4 different combinations, what are listed below, are possible:

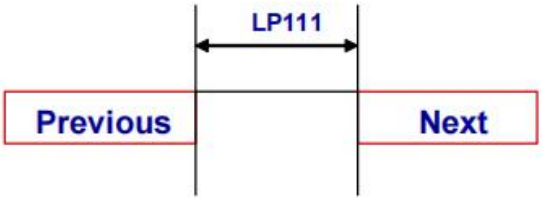
1. High Speed Mode => Stop State (SS, LP-111) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-111) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-111) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-111) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-111) Timings from Previous mode to Next mode

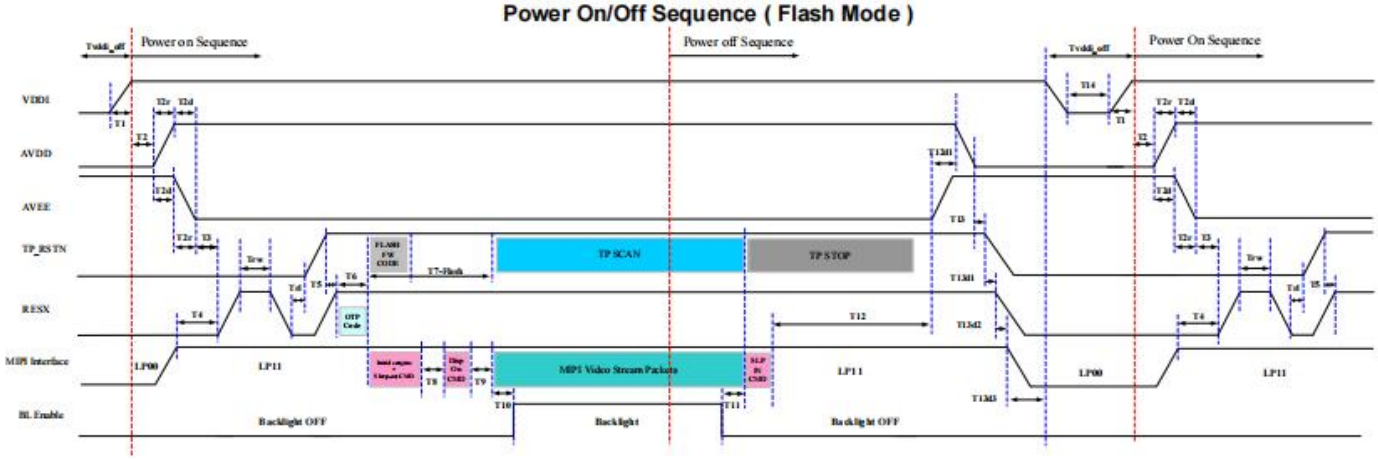
Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	400ns + 8UI	-	100 ns	-
HSDT	170ns + 52UI	-	520ns + 60UI	-	170ns + 52UI	-
BTA	100 ns	-	400ns + 8UI	-	100 ns	-



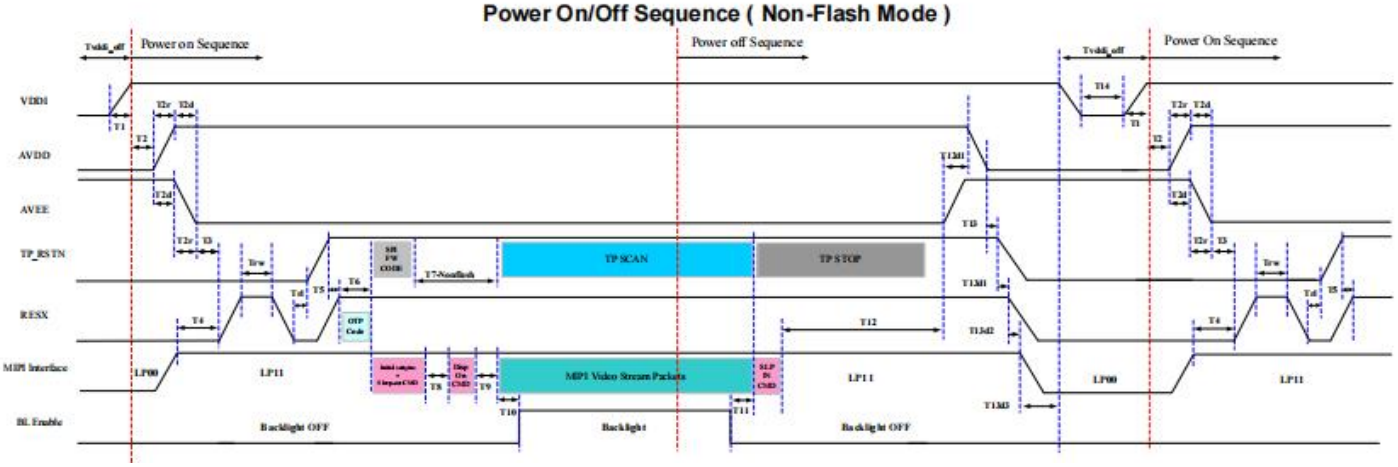
5.4 Power On/Off Sequence

1. There will be no hard-damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off sequences.
3. There will be no abnormal visible effects on the display between end of Power On sequence and before receiving Sleep-Out command. Also between receiving Sleep-In command and Power Off sequence.
4. RESX and TP_RSTN must be held stablely by host during Power On Sequence, otherwise function is not guaranteed.
5. During Abnormal power dropping, VDDI can start power down 3ms after AVDD/AVEE power down.
6. BL Enable timing is for reference only and not restricted (T10/T11).
7. 2nd reset timing is requested for RESX assertion and is optional for TP_RSTN assertion.
8. All input signals should be kept GND, floating or LP00 status during Tvddi_off.

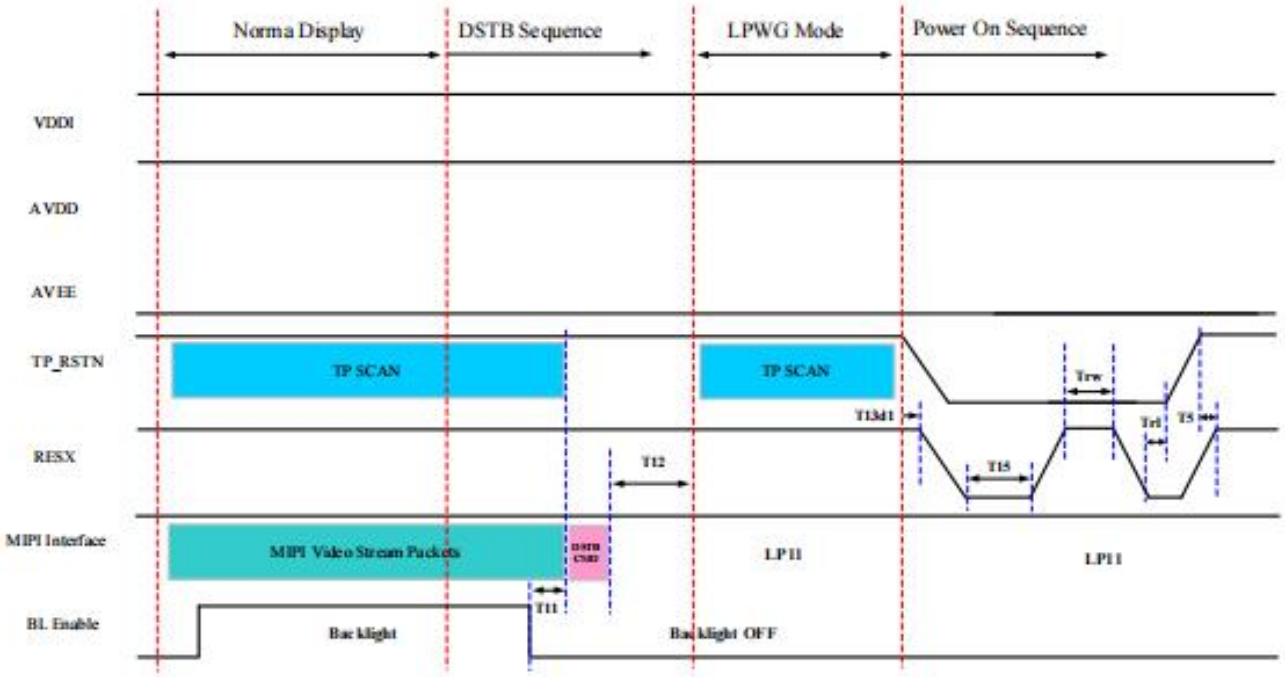
Power On/Off Sequence (Flash Mode)



Power On/Off Sequence (Non-Flash Mode)



TP Gesture Mode Exit Sequence



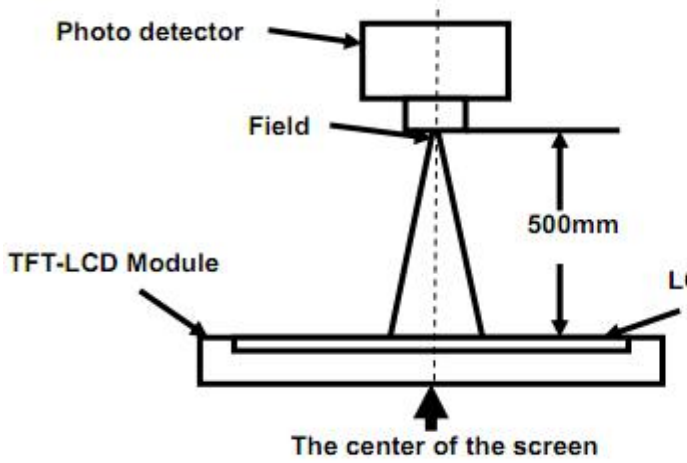
FT8206 Power On / Off Sequence Timing					
Parameter	Description	Min	Typ	Max	ms
T1	Rise time from 0.1*VDDI to 0.9*VDDI	0		5	ms
T2	AVDD power up after VDDI power on	3			ms
T2d	AVEE power up after AVDD power up	0			ms
T2r	Rise time from 0.1*AVDD to 0.9*AVDD Rise time from 0.1*AVEE to 0.9*AVEE	0.1		5	ms
T3	RESX reset release time after AVDD/AVEE power on	5			ms
T4	MIPI signals start (Hi-Z/GND to LP11) to RESX rising edge	0			ms
T5	TP Reset release to LCD Reset release	0			ms
T6	FLASH/OTP Settings download finished after RESX released MIPI may start to send Initial Settings + Sleep-out CMD SPI/Flash may start to send FW code			35	ms
T7-Nonflash	SPI FW Code download finish to TP SCAN Start (Non-flash mode)			200	ms
T7-Flash	Flash FW Code download start to TP SCAN Start (Flash mode)			280	ms
T8	Sleep-out CMD to Display-On CMD		120		ms
T9	Display-On CMD to MIPI Video Stream On time	10			ms
T10	MIPI Video Stream On time to Backlight On time	100			ms
T11	Backlight Off time to MIPI Video Stream Off time	100			ms
T12	AVEE power down after Sleep-In CMD	150			ms
T12d1	AVDD power down after AVEE power down	0			ms
T13	TP_RSTN falling edge after AVDD power down	0			ms
T13d1	In Power Off Sequence, TP_RSTN falling edge to RESX falling edge	0			ms
T13d2	In Power Off Sequence, RESX falling edge to MIPI interface power down	0			ms
T13d3	In Power Off Sequence, MIPI Interface power down to VDDI power down	3			ms
T14	VDDI rise again after VDDI power down (0.1*VDDI)	50			ms
T15	RESX falling edge (Exit from DSTB Mode) to RESX rising edge	5		120	ms
Trl	2nd RESX reset low width to TP_RSTN rising	5			ms
Trw	RESX high level width before 2nd RESX reset	5		10	ms

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	75	80	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	75	80	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	75	80	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	75	80	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	12	15	msec	Note4
	T_{OFF}		-	12	15	msec	Note4
Contrast Ratio	CR		1200	-	-	-	Note1 Note3
Color Chromaticity	W_X		0.245	0.295	0.345	-	Note1 Note5
	W_Y		0.254	0.304	0.354	-	Note1 Note5
Luminance	L		IF=240mA,1800cd/m2(TYP),1600cd/m2 (MIN) IF=400mA,3100cd/m2(TYP),2800cd/ m2(MIN)				Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		72	77	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

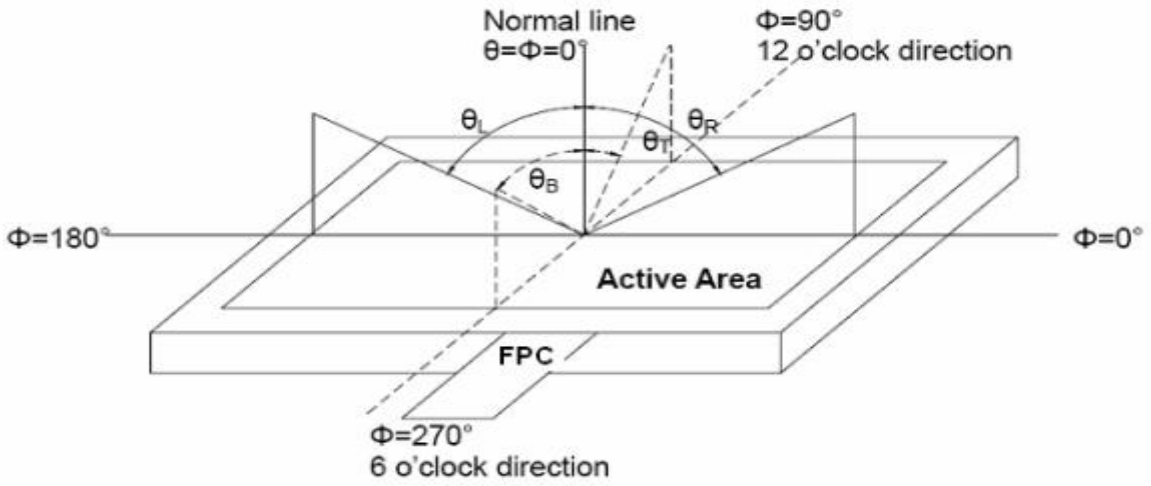


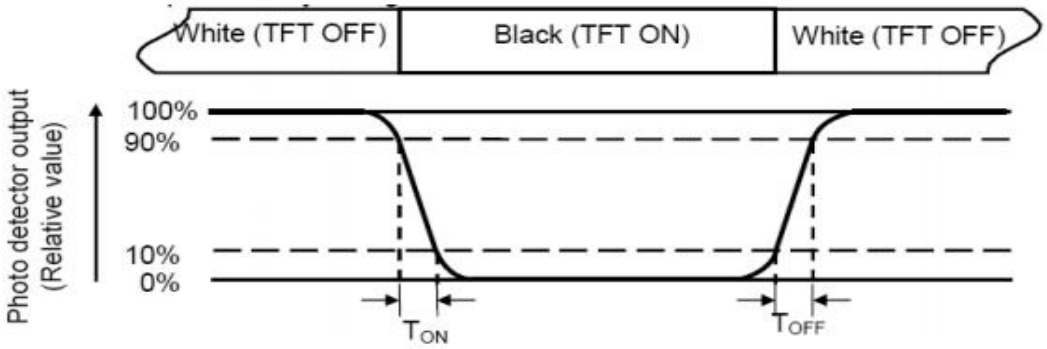
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

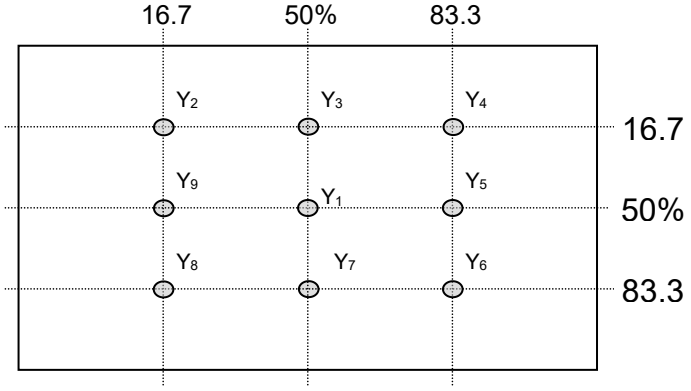


Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn).

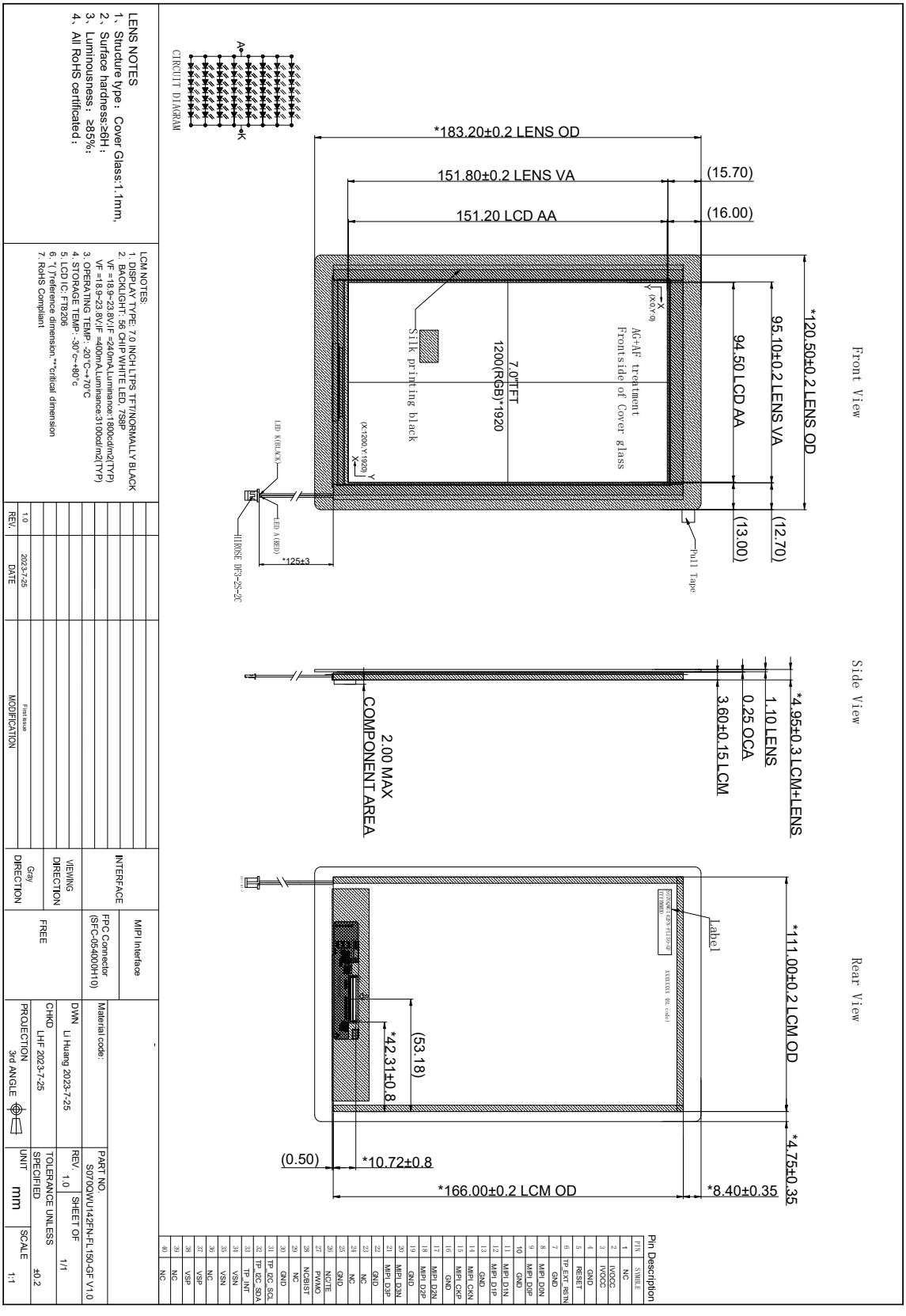
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

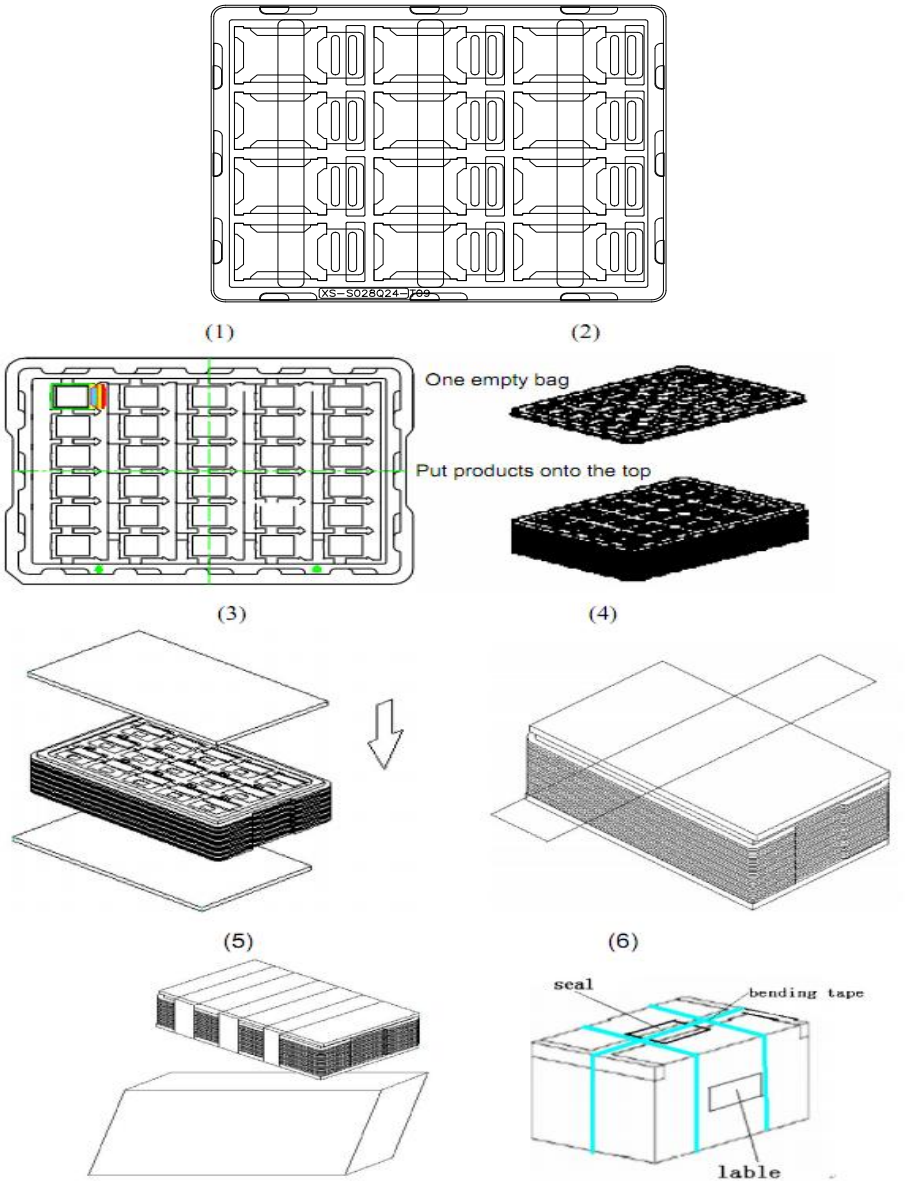
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.