PHOENIX DISPLAY INTERNATIONAL, INC.

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SPECIFICATION FOR LCD MODULE

CUSTOMER	
PART NUMBER	PDI040WVHS-16
DESCRIPTION	3.97" 480 x 800 TFT
VERSION	V1.0
ISSUE DATE	28-May-20

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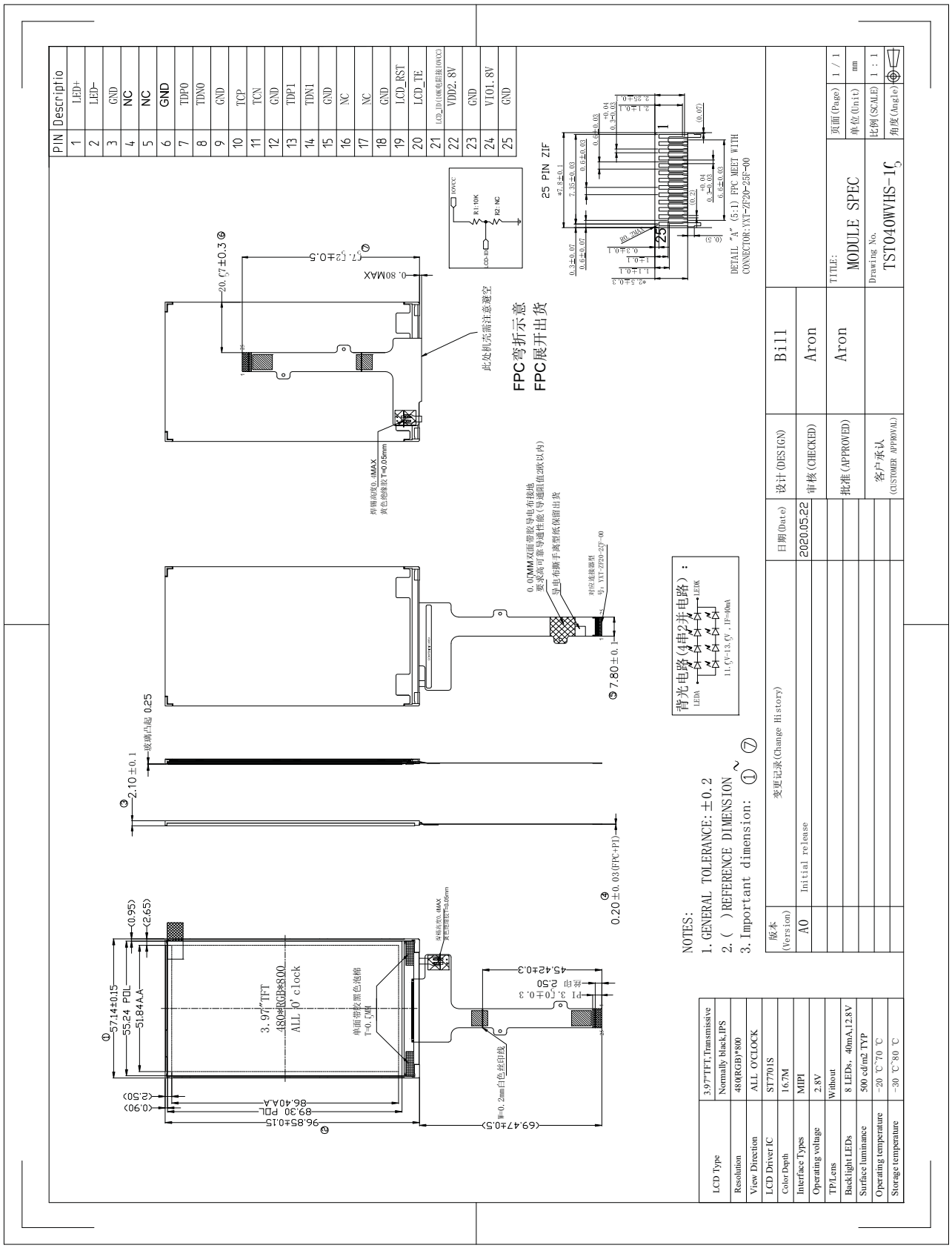
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1 General Characteristics

ITEM	Specification	Unit
LCD Type	TFT,Transmissive,Normally black,IPS	-
LCD Size	3.97	inch
Resolution (W x H)	480 x (RGB) × 800	pixel
LCM (W × H × D)	57.14(W) x 96.85(H) x 2.1(D)	mm
Active Area (W × H)	51.84 (W) x 86.4 (H)	mm
pixel Pitch (W × H)	0.108 x 0.108	mm
Viewing Direction	ALL o'clock	-
Gray Scale Inversion Direction	ALL o'clock	-
Viewing Angle	Top:80,Bottom:80; Left/ Right:80	deg.
Color Depth	16.7M	-
Pixel Arrangement	RGB-stripe	-
Backlight Type	8 LEDs	-
Surface Luminance	500	cd/m2
Surface Treatment	-	-
Polarizer	-	-
Driver IC	ST7701S	-
Interface Type	MIPI	-
Input Voltage	2.8	V
With/Without TP	without	-
Weight	TBD	g

Note 1: RoHS compliant
Note 2: LCM weight tolerance: ± 5%.

2 Product drawings



3 Interface description

PIN NO.	Symbol	description
1	LED+	Backlight A Aothod input pin.
2	LED-	Backlight K Cathode input pin.
3	GND	System Ground. (0V)
4	NC	No connect
5	NC	No connect
6	GND	System Ground. (0V)
7	TDP0	MIPI data aothod input pin
8	TDN0	MIPI data cathode input pin
9	GND	System Ground. (0V)
10	TCP	MIPI clock aothod input pin
11	TCN	MIPI clock cathode input pin
12	GND	System Ground. (0V)
13	TDP1	MIPI data aothod input pin
14	TDN1	MIPI data cathode input pin
15	GND	System Ground. (0V)
16	NC	No connect
17	NC	No connect
18	GND	System Ground. (0V)
19	LCD_RST	Reset input signal
20	LCD_TE	Tearing Effect output signal
21	LCDID(10K to IOVCC)	10K resistor connect IOVCC
22	VDD2.8V	Power supply +2.8Vt
23	GND	System Ground. (0V)
24	VIO1.8V	Voltage input pin for logic I/O +1.8V
25	GND	No connect

4 LCM Interface Timing

4.1 Reset Timing

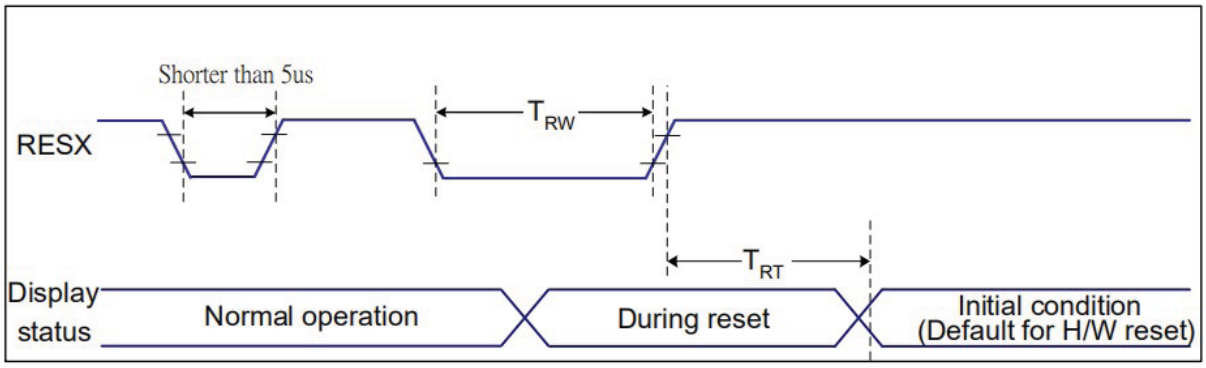


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

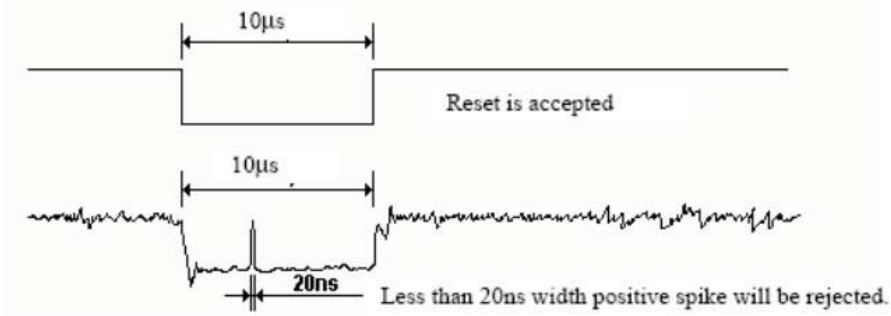
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.2 DSI Timing Characteristics

High Speed Mode

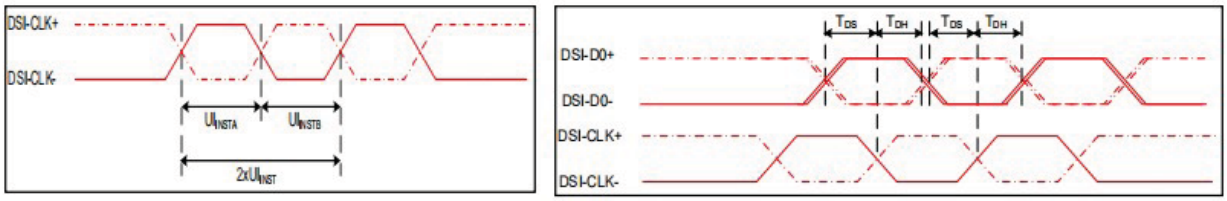


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

Lowe Power Mode

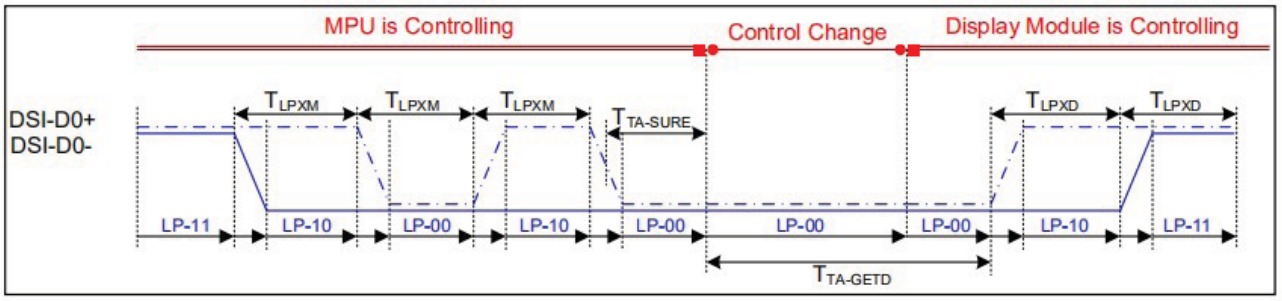


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

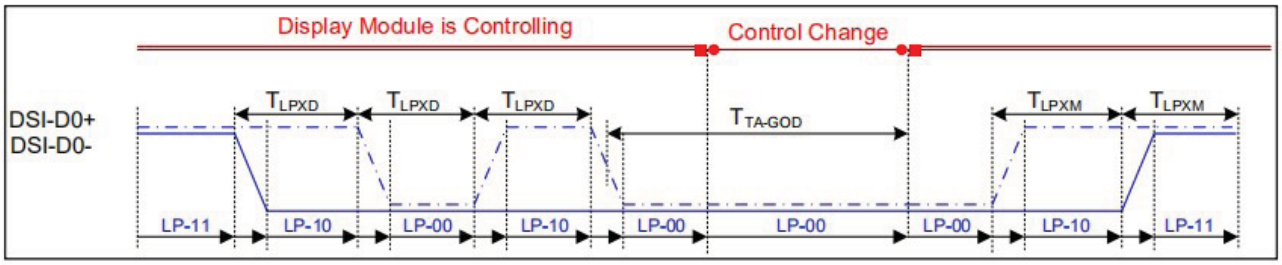


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

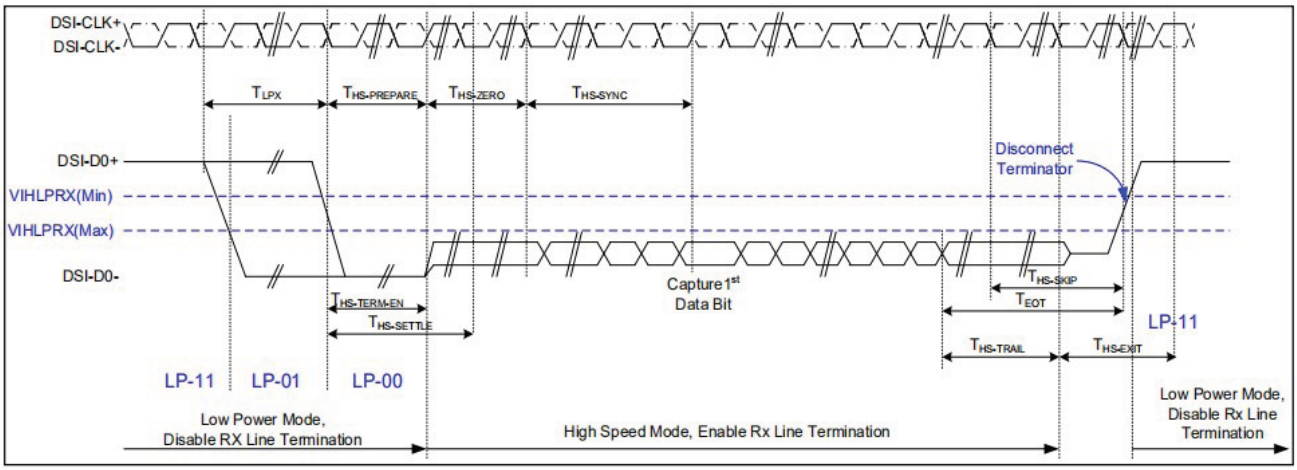


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

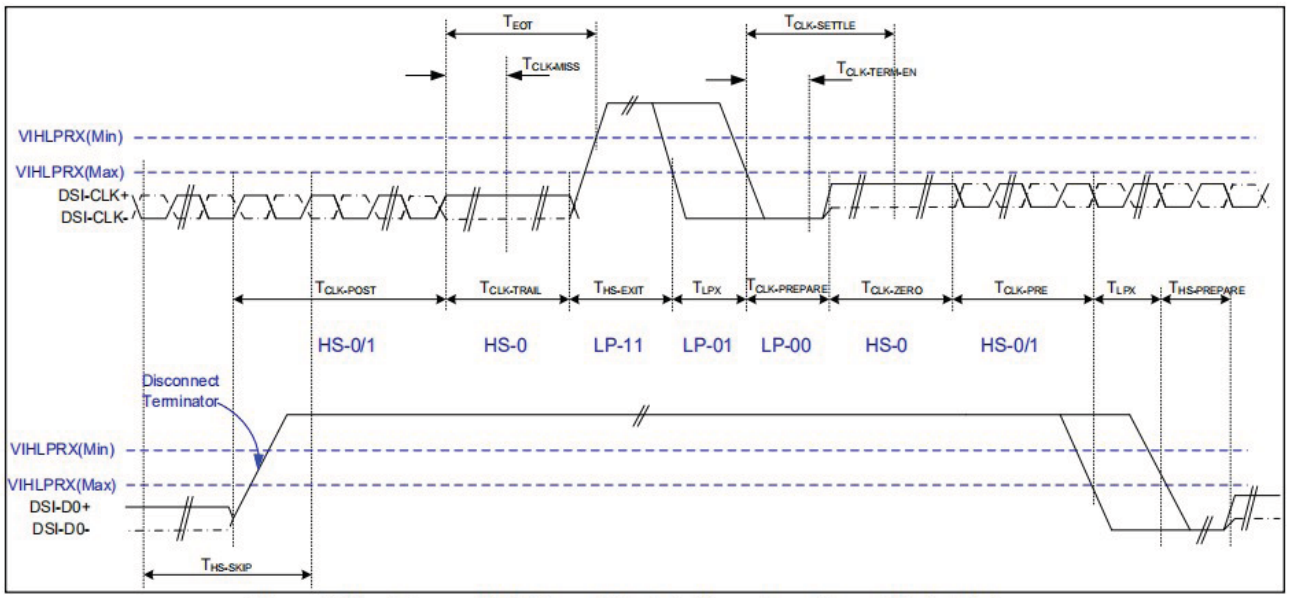


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

5 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Analog)	VCC~GND	-0.3	4.6	V
Logic signal voltage(I/O)	IOVCC~GND	-0.3	4.6	V
Operating Temperature	TOP	-20	70	° C
Storage Temperature	TST	-30	80	° C
Humidity	RH	-	90%(Max 60° C)	RH

6 Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog operating voltage	VCC	2.5	2.8	3.3	V
Logic operating voltage	IOVCC	1.65	1.8	3.3	V
Input Current	IDD	-	TBD	-	mA
Input Voltage ' H ' level	VIH	0.7IOVCC	-	IOVCC	V
Input Voltage ' L ' level	VIL	GND	-	0.3IOVCC	
Output Voltage ' H ' level	VOH	0.8IOVCC	-	IOVCC	
Output Voltage ' L ' level	VOL	GND	-	0.2IOVCC	

7 Backlight Characteristics

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Voltage for LED backlight	V_f	-	12.8	-	V
Current for LED backlight	I_f	-	40	-	mA
Power consumption	Wbl	-	512	-	mW
Uniformity	Avg	80	-	-	%
LED Life Time	-	30000	40000	-	Hrs

Note:

1.The LED life time is defined as the module brightness decrease to 50% original brightness at Ta=25°C, 60%RH ±5 %.

2. The life time of LED will be reduced if LED is driven by high current, high ambient temperature and humidity conditions.

3. Typical operating life time is an estimated data.

4. Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded .Functional operation should be restricted to the conditions described under normal operating conditions.

8 LCD Optical specifications

Item	Symbol	Condition	Specification			Unit	Remark
			Min	Typ	Max		
Response time (By Quick)	Tr+Tf	θ = 0°	-	20	30	ms	Note 5
Contrast ratio	CR	θ = 0°	550	800	-		Note 2,6
Viewing angle	Top	CR≧10	80	85	-	Deg.	Note 2,6,7
	Bottom	CR≧10	80	85	-		
	Left	CR≧10	80	85	-		
	Right	CR≧10	80	85	-		
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	Wx	θ = 0°	TBD	TBD	TBD		Note 3
	Wy			TBD			
	Rx			TBD			
	Ry			TBD			
	Gx			TBD			
	Gy			TBD			
	Bx			TBD			
	By			TBD			
NTSC			57%	60%	-		Note 3
Cross talk	Ct		-	-	2%		Note 9
Transmittance	Trans		-	3.9%	-		Note 4

Note 1: Ambient temperature = 25°C.

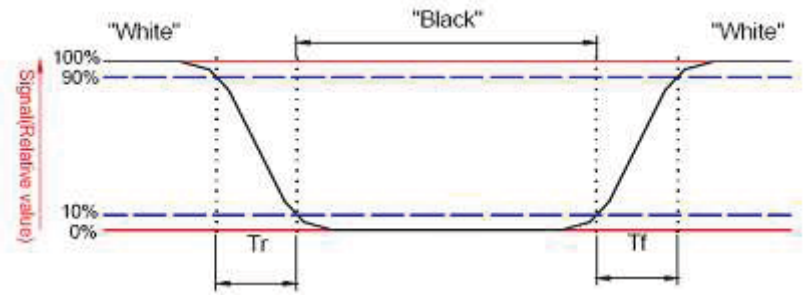
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer. The tolerance of Transmittance is ±10%.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to “White” (falling time) and from “White” to “Black” (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

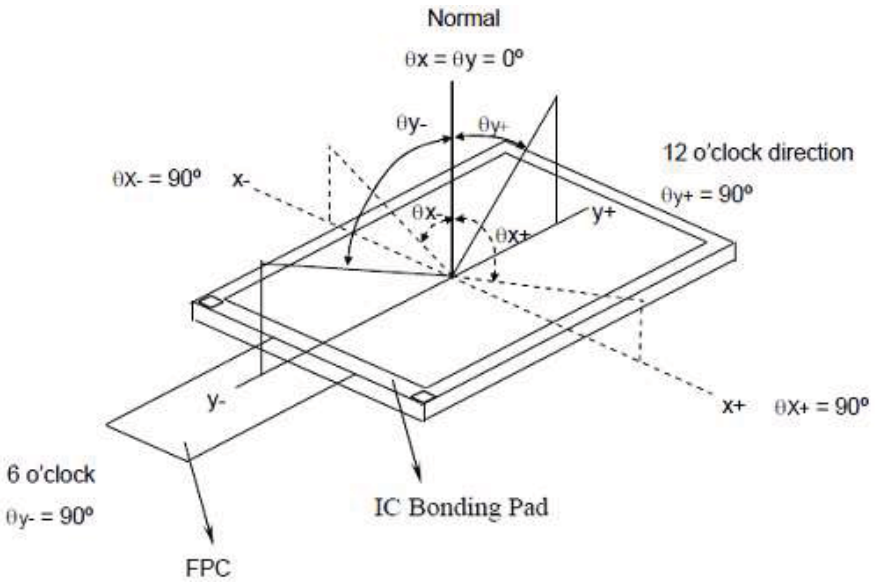


Note 6: Definition of contrast ratio:

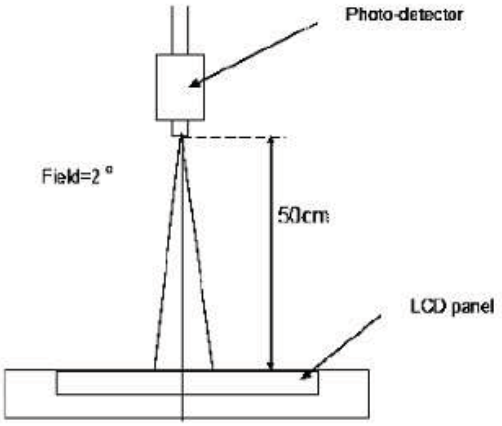
Contrast ratio is calculated by the following formula.

Contrast ratio (CR)= $\frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$

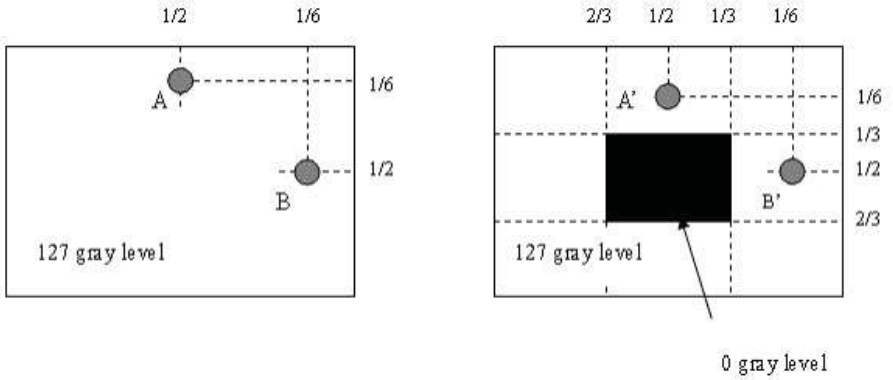
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note 9:



l LA-LA' l / LA x 100%= 2% max., LA and LA' are brightness at location A and A'.

l LB-LB’ l / LB x 100%= 2% max., LB and LB’ are brightness at location B and B’.

9 RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	INSPECTION AFTER TEST
1	High Temperature Storage	80±2°C/96 hours	Inspection after 2~4 hours storage at room temperature and humidity. The condensation is not accepted. The sample shall be free from defects: 1. Air bubble in the LCD 2. Seal leak 3. Non-display 4. Missing segments 5. Glass crack
2	Low Temperature Storage	-30±2°C/96 hours	
3	High Temperature Operating	70±2°C/96 hours	
4	Low Temperature Operating	-20±2°C/96 hours	
5	Temperature Cycle	-30±2°C ~ 25~ 80± 2°C × 10 cycles (30 min.) (5min.) (30min.)	
6	Damp Proof Test	60°C ±5°C × 90%RH/96 hours	
7	Vibration Test	Frequency 10Hz~55Hz Stroke: 1.5mm Sweep: 10Hz~150 Hz~10Hz 2 hours For each direction of X, Y, Z	
8	Shock Test	Half-sine, wave, 300m/s	
9	Packing Drop Test	Height: 80 cm 1 corner, concrete floor	
10	Electrostatic Discharge Test	C=150pF, R=330 Ω Air: ±8KV 150pF/330Ω 30 times Contact: ±4KV,20 times	

10 Suggestions for using LCD modules

10.1 Handling of LCM

1. The LCD screen is made of glass. Don't give excessive external shock, or drop from a high place.

2. If the LCD screen is damaged and the liquid crystal leaks out, do not lick and swallow. When the liquid is attach to your hand, skin, cloth etc, wash it off by using soap and water thoroughly and immediately.
3. Don't apply excessive force on the surface of the LCM.
4. If the surface is contaminated, clean it with soft cloth. If the LCM is severely contaminated, use Isopropyl alcohol/Ethyl alcohol to clean. Other solvents may damage the polarizer. The following solvents is especially prohibited: water , ketone Aromatic solvents etc.
5. Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
6. Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
7. Don't disassemble the LCM.
8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

9. Do not alter, modify or change the the shape of the tab on the metal frame.
10. Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
11. Do not damage or modify the pattern writing on the printed circuit board.
12. Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector
13. Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
14. Do not drop, bend or twist LCM.

10.2 Storage

1. Store in an ambient temperature of 5 to 45 C, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.
2. Storage in a clean environment, free from dust, active gas, and solvent.
3. Store in antistatic container.