GC9106

a-Si TFT LCD Single Chip Driver

128RGBx160 Resolution and 262K color

Specification

Preliminary Version 1.00
3/8/2017

GalaxyCore Incorporation

GalaxyCore Inc. reserves the right to change the contents in this document without prior notice.

Table of Content

Table of Content 2
1. Introduction 5
2. Features 6
3. Block Diagram 7
3.1. Block diagram 7
3.2. Pin Descriptions 8
3.3. PAD coordinates 12
4. Interface setting 18
4.1. MCU interfaces 18
4.1.1. MCU interface selection 18
4.1.2. 8080 Series Parallel Interface 19
4.1.3. Write Cycle Sequence 19
4.1.4. Read Cycle Sequence 20
4.1.5. Serial Interface 22
4.1.6. Write Cycle Sequence 22
4.1.7. Read Cycle Sequence 24
4.1.8. Data Transfer Break and Recovery 26
4.1.9. Data Transfer Pause 28
4.1.10. Serial Interface Pause 29
4.1.11. Parallel Interface Pause 29
4.1.12. Data Transfer Mode 29
4.1.13. Data Transfer Method 1 29
4.1.14. Data Transfer Method 2 30
4.2. Display Data Format 31
4.2.1. 3-line Serial Interface 31
4.2.2. 4-line Serial Interface 33
4.2.3. 2-data line mode 35
4.2.4. 8-bit Parallel MCU Interface 37
5. Function Description 39
5.1. Display data GRAM mapping 39
5.1.1. 132RGBx132 resolution (GM = “01”) 39
5.1.2. 128RGBx160 resolution (GM = “11”) 40
5.2. Address Counter (AC) of GRAM 41
5.2.1 128RGBx160 (GM == ‘11’) 43
5.2.1. 132RGBx132 (GM == ‘01’) 44
5.2.2. Frame Data Write Direction 45
5.3. GRAM to display address mapping 47
5.3.1. Normal display on or partial mode on, vertical scroll off 47
5.3.2. Vertical scroll display mode 49
5.4. Tearing effect output line 52
5.4.1. Tearing effect line modes 52

Preliminary

5.4.2. Tearing effect line timing 52
5.5. Source driver 53
5.6. Gate driver 53
5.7. LCD power generation circuit 54
5.7.1. Power supply circuit 54
5.7.2. LCD power generation scheme 55
5.8. Gamma Correction 56
5.9. Power Level Definition 58
5.9.1. Power Levels 58
5.9.2. Power Flow Chart 59
6. Command 60
6.1. Command List 60
USER REG 60
INTER REG 63
6.2. Description of User Command 65
6.2.1. Read Display Identification (00h) 65
6.2.2. Software Reset (01h) 66
6.2.3. Read display identification information 2 (04h) 67
6.2.4. Read Display Status (09h) 68
6.2.5. Read Display Power Mode (0Ah) 71
6.2.6. Read Display MADCTL (0Bh) 72
6.2.7. Read Display Pixel Format (0Ch) 73
6.2.8. Read Display Image Format (0Dh) 74
6.2.9. Read Display Signal Mode (0Eh) 75
6.2.10. Read Display Self-Diagnostic Result (0Fh) 76
6.2.11. Sleep In (10h) 77
6.2.12. Sleep Out (11h) 78
6.2.13. Partial Mode ON (12h) 80
6.2.14. Normal Display Mode ON (13h) 81
6.2.15. Display Inversion OFF (20h) 82
6.2.16. Display Inversion ON (21h) 83
6.2.17. Display OFF (28h) 84
6.2.18. Display ON (29h) 85
6.2.19. Column Address Set (2Ah) 86
6.2.20. Row Address Set (2Bh) 88
6.2.21. Memory Write (2Ch) 90
6.2.22. Partial Area (30h) 92
6.2.23. Vertical Scrolling Definition (33h) 95
6.2.24. Tearing Effect Line OFF (34h) 99
6.2.25. Tearing Effect Line ON (35h) 100
6.2.26. Memory Access Ctrl (36h) 102
6.2.27. Vertical Scrolling Start Address (37h) 105
6.2.28. Idle Mode OFF (38h) 107
6.2.29. Idle Mode ON (39h) 108

Preliminary

6.2.30. COLMOD: Pixel Format Set (3Ah) 110
6.2.31. Scan line set (44h) 111
6.2.32. Scan line Get (45h) 112
6.2.33. Display Inversion Control (B4h) 113
6.2.34. Read ID1 (DAh) 114
6.2.35. Read ID2 (DBh) 115
6.2.36. Read ID3 (DCh) 116
6.3. Description of Internal Command 117
6.3.1. Inter register enable 1 (FEh) 117
6.3.2. Inter register enable 2 (EFh) 118
6.3.3. Frame Rate Set(A3h) 119
6.3.4. SPI 2 DATA(AAh) 121
6.3.5. AVDD_CLK (C0h) 122
6.3.6. AVEE_CLK (C1h) 123
6.3.7. VGH_CLK (C2h) 124
6.3.8. VGL_CLK (C3h) 125
6.3.9. CHP_SOU_CLK (C6h) 126
6.3.10. VREG1_CTL (E6h) 127
6.3.11. VREG2_CTL (E7h) 129
6.3.12. CHP_CLAMP_CTL1 (EAh) 131
6.3.13. CHP_CLAMP_CTL2 (EBh) 132
6.3.14. SET_GAMMA1 (F0h) 134
6.3.15. SET_GAMMA2 (F1h) 135
7. Application 136
7.1 APPLICATION CIRCUIT 136
7.2 Voltage Generation 137
8. Electrical Characteristics 138
8.1. Absolute Maximum Ratings 138
8.2. DC Characteristics 139
8.3. AC Characteristics 141
8.3.1. Display Parallel 8-bit Interface Timing Characteristics (8080) 141
8.3.2. Display Serial Interface Timing Characteristics (3-line SPI system) 143
8.3.3. Display Serial Interface Timing Characteristics (4-line SPI system) 144
9. Revision History 145

Preliminary

1. Introduction

The GC9106 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 128RGBx160dots, comprising a 384-channel source driver, a 160-channel gate driver, 48,114 bytes GRAM for graphic display data of 128RGBx160 dots, and power supply circuit.

The GC9106 supports parallel 8-bit data bus MCU interface, and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The GC9106 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9106 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9106 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

Preliminary

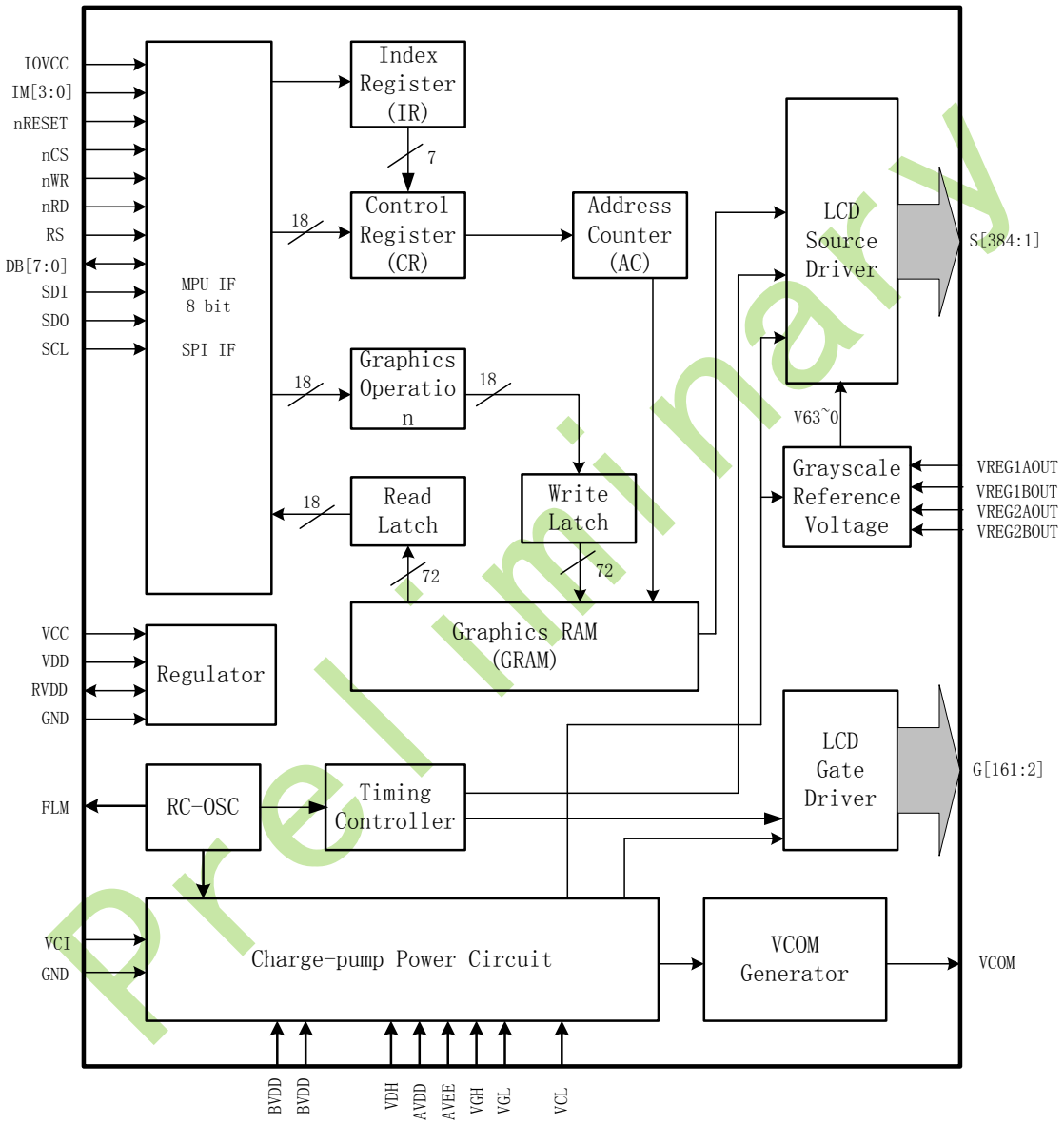
2. Features

- No need for external electronic component.
- Display resolution: [128xRGB](H) x 160(V)
- Output:
  - 384 source outputs
  - 160 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 48,114 bytes
- System Interface
  - 8-bits interface with 8080 MCU
  - 3-line / 4-line serial interface
  - 2-data line SPI interface
- Driving Algorithm Support
  - 1-dot/2-dot/4-dot/8-dot Inversion
  - Column Inversion
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - 8-color mode
  - Standby mode
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Window address function to specify a rectangular area for internal GRAM access
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- On-Chip Power System
  - Source Voltage (VREG1A, VREG2A,VREG1B/ VREG2B): +6.0V,-3.0V,+1.5V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +10.0V
  - Gate driver LOW level (VGL to AGND): -10.0V
- Operate temperature range: -40℃to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

Preliminary

3. Block Diagram

3.1. Block diagram



Preliminary

3.2. Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VCI	I	Power	Power supply for analog, digital system and booster circuit
IOVCC	I	Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
DGND	I	Digital Ground	System ground level for logic blocks and I/O circuit
AGND	I	Analog Ground	System ground level for analog blocks and booster circuit.

Interface Logic Signals			
Pin Name	I/O	Type	Descriptions
IM2	I	(VDDI/DGND)	MCU Parallel interface bus and Serial interface select - IM2=’1’;Parallel-8bit Interface - IM2=’0’;Serial Interface
SPIW4	I	(VDDI/DGND)	SPI interface selection pin SPI4W=’0’: 3-wire SPI. (default) SPI4W=’1’: 4-wire SPI. This pin is internal pull low.
RESX	I	MCU (VDDI/DGND)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	MCU (VDDI/DGND)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. *note1,2
D/CX （**SCL**）	I	MCU (VDDI/DGND)	This pin is used to select "Data or Command" in the parallel interface。 When DCX='1', data is selected. When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-write 8-bit serial data interface. If not used, this pin should be connected to VDDI or DGND.
RDX	I	MCU (VDDI/DGND)	8080 system (RDX): Serves as a read signal and MCU read data at the rising edge.
WRX **(RS)**	I	MCU (VDDI/DGND)	8080 system (WRX): Serves as a write signal and writes data at the rising edge. 4-write 8-bit serial data interface: serves as **RS**(data/command selection). Fix to VDDI level when not in use
D[7:1] **D0/SDA**	I/O	MCU (VDDI/DGND)	8-bit parallel bi-directional data bus for MCU system and D0 is also the serial input/output signal in SPI interface mode. Fix to DGND level when not in use
GM[1:0]	I	(VDDI/DGND)	Panel Resolution selection pins

GM1	GM0	Resolution	Source gate	Window set(2ah 2bh)
0	0	128X128	S1-S384, G2-G129	(0x00,0x7f) (0x00,0x7f)
0	1	128X128	S1-S384, G2-G129	(0x00,0x83) (0x00,0x83)
0	1	128X128	S1-S384, G2-G129	(0x02,0x81) (0x01,0x80)

Preliminary

			1	0	128X160	S1-S384, G2-G161	(0x00,0x83) (0x00,0xa1)
			1	0	128X160	S1-S384, G2-G161	(0x02,0x81) (0x01,0xa0)
			1	1	128X160	S1-S384, G2-G161	(0x00,0x7f) (0x00,0x9f)
TE	O	MCU (VDDI/DGND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.				

Note.

1. If CSX is connected to DGND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S396~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G160~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
AVDD	O	OPEN	Power pad for analog circuit, A power supply pin for generating VREG1A
AVEE	O	OPEN	Power pad for analog circuit, A power supply pin for generating VREG2A
BVDD	O	OPEN	Power pad for analog circuit, A power supply pin for generating SOURCE(positive)
BVEE	O	OPEN	Power pad for analog circuit, A power supply pin for generating SOURCE(negative)
VGH	O	Power	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits.
VGL	O	Power	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits.
VCL	O	Power	Power supply for VCOML. VCL=0~-VDD
VREG1A	O	OPEN	A power output of gray scale voltage generator(positive)
VREG1B	O	OPEN	A power output of gray scale voltage generator(positive)
VREG2A	O	OPEN	A power output of gray scale voltage generator(negative)
VREG2B	O	OPEN	A power output of gray scale voltage generator(negative)
VCOM	O		Power supply pad for the TFT-display counter electrode. VCOM=GND Connect this pad to the TFT-display counter electrode.
DGNDO	O		DGND voltage output level for monitoring

Preliminary

Test Pins			
Pin Name	I/O	Type	Descriptions
TEST2P TEST1P	I	Digital Ground	These test pins for driver vender test used Please connect these pins to DGND
TESTOP[8:1]	O	Open	These test pins for driver vender test used Please leave these pins open
DUMMYR	-	Open	These pins are dummy. During normal operation, leave these pads open.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

Preliminary

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		396 pins (132*RGB)
2	TFT Gate Driver		160ins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S396	V0~V63 grayscales
		G1~G160	VGH-VGL
		VCOM	GND
5	Input Voltage	IOVCC	1.65~3.30V
		VCI	2.50~3.30V
6	Liquid Crystal Drive Voltages	VREG1A	6.0V
		VREG2A	-3.0V
		VREG1B	1.5V
		VREG2B	1.5V
		VGH	10.0V
		VGL	-10.0V

Preliminary

3.3. PAD coordinates

No.	Pad name	X	Y
1	DUMMY	-4750.0	-223.5
2	DUMMY	-4700.0	-223.5
3	DUMMY	-4650.0	-223.5
4	DUMMY	-4600.0	-223.5
5	DUMMY	-4550.0	-223.5
6	DUMMY	-4500.0	-223.5
7	DUMMY	-4450.0	-223.5
8	DUMMY	-4400.0	-223.5
9	DUMMY	-4350.0	-223.5
10	DUMMY	-4300.0	-223.5
11	DUMMY	-4250.0	-223.5
12	DUMMY	-4200.0	-223.5
13	DUMMY	-4150.0	-223.5
14	DUMMY	-4100.0	-223.5
15	DUMMY	-4050.0	-223.5
16	DUMMY	-4000.0	-223.5
17	DUMMY	-3950.0	-223.5
18	DUMMY	-3900.0	-223.5
19	DUMMY	-3850.0	-223.5
20	DUMMY	-3800.0	-223.5
21	DUMMY	-3750.0	-223.5
22	DUMMY	-3700.0	-223.5
23	DUMMY	-3650.0	-223.5
24	DUMMY	-3600.0	-223.5
25	DUMMY	-3550.0	-223.5
26	DUMMY	-3500.0	-223.5
27	DUMMY	-3450.0	-223.5
28	DUMMY	-3400.0	-223.5
29	DUMMY	-3350.0	-223.5
30	DUMMY	-3300.0	-223.5
31	DUMMY	-3250.0	-223.5
32	DUMMY	-3200.0	-223.5
33	DUMMY	-3150.0	-223.5
34	DUMMY	-3100.0	-223.5
35	DUMMY	-3050.0	-223.5
36	DGNDO	-3000.0	-223.5
37	GM<1>	-2950.0	-223.5
38	IOVCC	-2900.0	-223.5
39	GM<0>	-2850.0	-223.5
40	DGNDO	-2800.0	-223.5
41	DUMMY	-2750.0	-223.5
42	DUMMY	-2700.0	-223.5
43	SPI4W	-2650.0	-223.5
44	IOVCC	-2600.0	-223.5
45	OSC_IN	-2550.0	-223.5
46	BIST_CLK	-2500.0	-223.5
47	BGR	-2450.0	-223.5
48	BIAS	-2400.0	-223.5
49	DUMMY	-2350.0	-223.5
50	OSC_TEST	-2300.0	-223.5
51	VCI	-2250.0	-223.5
52	VCI	-2200.0	-223.5
53	VCI	-2150.0	-223.5
54	VCI	-2100.0	-223.5
55	VCI	-2050.0	-223.5
56	VCI	-2000.0	-223.5
57	DGND	-1950.0	-223.5
58	DGND	-1900.0	-223.5
59	DGND	-1850.0	-223.5
60	DGND	-1800.0	-223.5
61	DGND	-1750.0	-223.5
62	DGND	-1700.0	-223.5
63	RDX	-1630.0	-223.5
64	DCX	-1570.0	-223.5
65	DUMMY	-1510.0	-223.5
66	DUMMY	-1450.0	-223.5
67	DUMMY	-1390.0	-223.5
68	DUMMY	-1330.0	-223.5
69	DUMMY	-1270.0	-223.5
70	DUMMY	-1210.0	-223.5
71	DUMMY	-1150.0	-223.5
72	DUMMY	-1090.0	-223.5
73	DUMMY	-1030.0	-223.5
74	DUMMY	-970.0	-223.5
75	DUMMY	-910.0	-223.5
76	DUMMY	-850.0	-223.5
77	D<1>	-790.0	-223.5
78	D<3>	-730.0	-223.5
79	D<5>	-670.0	-223.5
80	D<7>	-610.0	-223.5
81	TE	-550.0	-223.5
82	RESX	-490.0	-223.5
83	CS	-430.0	-223.5
84	D<6>	-370.0	-223.5
85	D<4>	-310.0	-223.5
86	D<2>	-250.0	-223.5
87	IM<2>	-190.0	-223.5
88	D<0>	-130.0	-223.5
89	WRX	-70.0	-223.5
90	DUMMY	0.0	-223.5
91	DUMMY	50.0	-223.5
92	DUMMY	100.0	-223.5
93	DUMMY	150.0	-223.5
94	VCI1	200.0	-223.5
95	DUMMY	250.0	-223.5
96	VREF_OUT	300.0	-223.5
97	AGND	350.0	-223.5
98	AGND	400.0	-223.5
99	AGND	450.0	-223.5
100	AGND	500.0	-223.5
101	AGND	550.0	-223.5
102	AGND	600.0	-223.5
103	IOVCC	650.0	-223.5
104	IOVCC	700.0	-223.5
105	IOVCC	750.0	-223.5
106	IOVCC	800.0	-223.5
107	IOVCC	850.0	-223.5
108	IOVCC	900.0	-223.5
109	VPP	950.0	-223.5
110	VPP	1000.0	-223.5
111	VPP	1050.0	-223.5
112	GVDD	1100.0	-223.5
113	GVDD	1150.0	-223.5
114	GVDD	1200.0	-223.5
115	VCORE	1250.0	-223.5
116	DUMMY	1300.0	-223.5
117	DUMMY	1350.0	-223.5
118	DUMMY	1400.0	-223.5
119	DUMMY	1450.0	-223.5
120	AVDD	1500.0	-223.5
121	AVDD	1550.0	-223.5
122	AVDD	1600.0	-223.5
123	AVDD	1650.0	-223.5
124	AVDD	1700.0	-223.5
125	DUMMY	1750.0	-223.5
126	DUMMY	1800.0	-223.5
127	DUMMY	1850.0	-223.5
128	DUMMY	1900.0	-223.5
129	DUMMY	1950.0	-223.5
130	DUMMY	2000.0	-223.5
131	DUMMY	2050.0	-223.5
132	DUMMY	2100.0	-223.5
133	DUMMY	2150.0	-223.5
134	DUMMY	2200.0	-223.5
135	DUMMY	2250.0	-223.5
136	DUMMY	2300.0	-223.5
137	DUMMY	2350.0	-223.5
138	DUMMY	2400.0	-223.5
139	DUMMY	2450.0	-223.5
140	DUMMY	2500.0	-223.5
141	DUMMY	2550.0	-223.5
142	DUMMY	2600.0	-223.5
143	DUMMY	2650.0	-223.5
144	DUMMY	2700.0	-223.5
145	DUMMY	2750.0	-223.5
146	AGND	2800.0	-223.5
147	AGND	2850.0	-223.5
148	AGND	2900.0	-223.5
149	VCL	2950.0	-223.5
150	VCL	3000.0	-223.5
151	VCL	3050.0	-223.5
152	DUMMY	3100.0	-223.5
153	DUMMY	3150.0	-223.5
154	DUMMY	3200.0	-223.5
155	DUMMY	3250.0	-223.5
156	DUMMY	3300.0	-223.5
157	DUMMY	3350.0	-223.5
158	DUMMY	3400.0	-223.5
159	DUMMY	3450.0	-223.5
160	DUMMY	3500.0	-223.5
161	DUMMY	3550.0	-223.5
162	DUMMY	3600.0	-223.5
163	DUMMY	3650.0	-223.5
164	DUMMY	3700.0	-223.5
165	DUMMY	3750.0	-223.5
166	DUMMY	3800.0	-223.5
167	DUMMY	3850.0	-223.5
168	DUMMY	3900.0	-223.5
169	DUMMY	3950.0	-223.5
170	VGL	4000.0	-223.5
171	VGL	4050.0	-223.5
172	VGL	4100.0	-223.5
173	VGH	4150.0	-223.5
174	VGH	4200.0	-223.5
175	VGH	4250.0	-223.5
176	DUMMY	4300.0	-223.5
177	DUMMY	4350.0	-223.5
178	DUMMY	4400.0	-223.5
179	DUMMY	4450.0	-223.5
180	DUMMY	4500.0	-223.5
181	DUMMY	4550.0	-223.5
182	VCOM	4600.0	-223.5
183	VCOM	4650.0	-223.5
184	VCOM	4700.0	-223.5
185	DUMMY	4750.0	-223.5
186	Dummy	4772.0	110.0
187	Dummy	4756.0	227.0
188	G<162>	4740.0	110.0
189	G<160>	4724.0	227.0
190	G<158>	4708.0	110.0
191	G<156>	4692.0	227.0
192	G<154>	4676.0	110.0
193	G<152>	4660.0	227.0
194	G<150>	4644.0	110.0
195	G<148>	4628.0	227.0
196	G<146>	4612.0	110.0
197	G<144>	4596.0	227.0
198	G<142>	4580.0	110.0
199	G<140>	4564.0	227.0
200	G<138>	4548.0	110.0

Preliminary

No.	Pad name	X	Y
201	G<136>	4532.0	227.0
202	G<134>	4516.0	110.0
203	G<132>	4500.0	227.0
204	G<130>	4484.0	110.0
205	G<128>	4468.0	227.0
206	G<126>	4452.0	110.0
207	G<124>	4436.0	227.0
208	G<122>	4420.0	110.0
209	G<120>	4404.0	227.0
210	G<118>	4388.0	110.0
211	G<116>	4372.0	227.0
212	G<114>	4356.0	110.0
213	G<112>	4340.0	227.0
214	G<110>	4324.0	110.0
215	G<108>	4308.0	227.0
216	G<106>	4292.0	110.0
217	G<104>	4276.0	227.0
218	G<102>	4260.0	110.0
219	G<100>	4244.0	227.0
220	G<98>	4228.0	110.0
221	G<96>	4212.0	227.0
222	G<94>	4196.0	110.0
223	G<92>	4180.0	227.0
224	G<90>	4164.0	110.0
225	G<88>	4148.0	227.0
226	G<86>	4132.0	110.0
227	G<84>	4116.0	227.0
228	G<82>	4100.0	110.0
229	G<80>	4084.0	227.0
230	G<78>	4068.0	110.0
231	G<76>	4052.0	227.0
232	G<74>	4036.0	110.0
233	G<72>	4020.0	227.0
234	G<70>	4004.0	110.0
235	G<68>	3988.0	227.0
236	G<66>	3972.0	110.0
237	G<64>	3956.0	227.0
238	G<62>	3940.0	110.0
239	G<60>	3924.0	227.0
240	G<58>	3908.0	110.0
241	G<56>	3892.0	227.0
242	G<54>	3876.0	110.0
243	G<52>	3860.0	227.0
244	G<50>	3844.0	110.0
245	G<48>	3828.0	227.0
246	G<46>	3812.0	110.0
247	G<44>	3796.0	227.0
248	G<42>	3780.0	110.0
249	G<40>	3764.0	227.0
250	G<38>	3748.0	110.0

No.	Pad	X	Y
251	G<36>	3732.0	227.0
252	G<34>	3716.0	110.0
253	G<32>	3700.0	227.0
254	G<30>	3684.0	110.0
255	G<28>	3668.0	227.0
256	G<26>	3652.0	110.0
257	G<24>	3636.0	227.0
258	G<22>	3620.0	110.0
259	G<20>	3604.0	227.0
260	G<18>	3588.0	110.0
261	G<16>	3572.0	227.0
262	G<14>	3556.0	110.0
263	G<12>	3540.0	227.0
264	G<10>	3524.0	110.0
265	G<8>	3508.0	227.0
266	G<6>	3492.0	110.0
267	G<4>	3476.0	227.0
268	G<2>	3460.0	110.0
269	Dummy	3444.0	227.0
270	Dummy	3428.0	110.0
271	Dummy	3412.0	227.0
272	Dummy	3396.0	110.0
273	S<396>	3380.0	227.0
274	S<395>	3364.0	110.0
275	S<394>	3348.0	227.0
276	S<393>	3332.0	110.0
277	S<392>	3316.0	227.0
278	S<391>	3300.0	110.0
279	S<390>	3284.0	227.0
280	S<389>	3268.0	110.0
281	S<388>	3252.0	227.0
282	S<387>	3236.0	110.0
283	S<386>	3220.0	227.0
284	S<385>	3204.0	110.0
285	S<384>	3188.0	227.0
286	S<383>	3172.0	110.0
287	S<382>	3156.0	227.0
288	S<381>	3140.0	110.0
289	S<380>	3124.0	227.0
290	S<379>	3108.0	110.0
291	S<378>	3092.0	227.0
292	S<377>	3076.0	110.0
293	S<376>	3060.0	227.0
294	S<375>	3044.0	110.0
295	S<374>	3028.0	227.0
296	S<373>	3012.0	110.0
297	S<372>	2996.0	227.0
298	S<371>	2980.0	110.0
299	S<370>	2964.0	227.0
300	S<369>	2948.0	110.0

No.	Pad name	X	Y
301	S<368>	2932.0	227.0
302	S<367>	2916.0	110.0
303	S<366>	2900.0	227.0
304	S<365>	2884.0	110.0
305	S<364>	2868.0	227.0
306	S<363>	2852.0	110.0
307	S<362>	2836.0	227.0
308	S<361>	2820.0	110.0
309	S<360>	2804.0	227.0
310	S<359>	2788.0	110.0
311	S<358>	2772.0	227.0
312	S<357>	2756.0	110.0
313	S<356>	2740.0	227.0
314	S<355>	2724.0	110.0
315	S<354>	2708.0	227.0
316	S<353>	2692.0	110.0
317	S<352>	2676.0	227.0
318	S<351>	2660.0	110.0
319	S<350>	2644.0	227.0
320	S<349>	2628.0	110.0
321	S<348>	2612.0	227.0
322	S<347>	2596.0	110.0
323	S<346>	2580.0	227.0
324	S<345>	2564.0	110.0
325	S<344>	2548.0	227.0
326	S<343>	2532.0	110.0
327	S<342>	2516.0	227.0
328	S<341>	2500.0	110.0
329	S<340>	2484.0	227.0
330	S<339>	2468.0	110.0
331	S<338>	2452.0	227.0
332	S<337>	2436.0	110.0
333	S<336>	2420.0	227.0
334	S<335>	2404.0	110.0
335	S<334>	2388.0	227.0
336	S<333>	2372.0	110.0
337	S<332>	2356.0	227.0
338	S<331>	2340.0	110.0
339	S<330>	2324.0	227.0
340	S<329>	2308.0	110.0
341	S<328>	2292.0	227.0
342	S<327>	2276.0	110.0
343	S<326>	2260.0	227.0
344	S<325>	2244.0	110.0
345	S<324>	2228.0	227.0
346	S<323>	2212.0	110.0
347	S<322>	2196.0	227.0
348	S<321>	2180.0	110.0
349	S<320>	2164.0	227.0
350	S<319>	2148.0	110.0

No.	Pad name	X	Y
351	S<318>	2132.0	227.0
352	S<317>	2116.0	110.0
353	S<316>	2100.0	227.0
354	S<315>	2084.0	110.0
355	S<314>	2068.0	227.0
356	S<313>	2052.0	110.0
357	S<312>	2036.0	227.0
358	S<311>	2020.0	110.0
359	S<310>	2004.0	227.0
360	S<309>	1988.0	110.0
361	S<308>	1972.0	227.0
362	S<307>	1956.0	110.0
363	S<306>	1940.0	227.0
364	S<305>	1924.0	110.0
365	S<304>	1908.0	227.0
366	S<303>	1892.0	110.0
367	S<302>	1876.0	227.0
368	S<301>	1860.0	110.0
369	S<300>	1844.0	227.0
370	S<299>	1828.0	110.0
371	S<298>	1812.0	227.0
372	S<297>	1796.0	110.0
373	S<296>	1780.0	227.0
374	S<295>	1764.0	110.0
375	S<294>	1748.0	227.0
376	S<293>	1732.0	110.0
377	S<292>	1716.0	227.0
378	S<291>	1700.0	110.0
379	S<290>	1684.0	227.0
380	S<289>	1668.0	110.0
381	S<288>	1652.0	227.0
382	S<287>	1636.0	110.0
383	S<286>	1620.0	227.0
384	S<285>	1604.0	110.0
385	S<284>	1588.0	227.0
386	S<283>	1572.0	110.0
387	S<282>	1556.0	227.0
388	S<281>	1540.0	110.0
389	S<280>	1524.0	227.0
390	S<279>	1508.0	110.0
391	S<278>	1492.0	227.0
392	S<277>	1476.0	110.0
393	S<276>	1460.0	227.0
394	S<275>	1444.0	110.0
395	S<274>	1428.0	227.0
396	S<273>	1412.0	110.0
397	S<272>	1396.0	227.0
398	S<271>	1380.0	110.0
399	S<270>	1364.0	227.0
400	S<269>	1348.0	110.0

Preliminary

No.	Pad name	X	Y
401	S<268>	1332.0	227.0
402	S<267>	1316.0	110.0
403	S<266>	1300.0	227.0
404	S<265>	1284.0	110.0
405	S<264>	1268.0	227.0
406	S<263>	1252.0	110.0
407	S<262>	1236.0	227.0
408	S<261>	1220.0	110.0
409	S<260>	1204.0	227.0
410	S<259>	1188.0	110.0
411	S<258>	1172.0	227.0
412	S<257>	1156.0	110.0
413	S<256>	1140.0	227.0
414	S<255>	1124.0	110.0
415	S<254>	1108.0	227.0
416	S<253>	1092.0	110.0
417	S<252>	1076.0	227.0
418	S<251>	1060.0	110.0
419	S<250>	1044.0	227.0
420	S<249>	1028.0	110.0
421	S<248>	1012.0	227.0
422	S<247>	996.0	110.0
423	S<246>	980.0	227.0
424	S<245>	964.0	110.0
425	S<244>	948.0	227.0
426	S<243>	932.0	110.0
427	S<242>	916.0	227.0
428	S<241>	900.0	110.0
429	S<240>	884.0	227.0
430	S<239>	868.0	110.0
431	S<238>	852.0	227.0
432	S<237>	836.0	110.0
433	S<236>	820.0	227.0
434	S<235>	804.0	110.0
435	S<234>	788.0	227.0
436	S<233>	772.0	110.0
437	S<232>	756.0	227.0
438	S<231>	740.0	110.0
439	S<230>	724.0	227.0
440	S<229>	708.0	110.0
441	S<228>	692.0	227.0
442	S<227>	676.0	110.0
443	S<226>	660.0	227.0
444	S<225>	644.0	110.0
445	S<224>	628.0	227.0
446	S<223>	612.0	110.0
447	S<222>	596.0	227.0
448	S<221>	580.0	110.0
449	S<220>	564.0	227.0
450	S<219>	548.0	110.0

No.	Pad	X	Y
451	S<218>	532.0	227.0
452	S<217>	516.0	110.0
453	S<216>	500.0	227.0
454	S<215>	484.0	110.0
455	S<214>	468.0	227.0
456	S<213>	452.0	110.0
457	S<212>	436.0	227.0
458	S<211>	420.0	110.0
459	S<210>	404.0	227.0
460	S<209>	388.0	110.0
461	S<208>	372.0	227.0
462	S<207>	356.0	110.0
463	S<206>	340.0	227.0
464	S<205>	324.0	110.0
465	S<204>	308.0	227.0
466	S<203>	292.0	110.0
467	S<202>	276.0	227.0
468	S<201>	260.0	110.0
469	S<200>	244.0	227.0
470	S<199>	228.0	110.0
471	S<198>	-228.0	110.0
472	S<197>	-244.0	227.0
473	S<196>	-260.0	110.0
474	S<195>	-276.0	227.0
475	S<194>	-292.0	110.0
476	S<193>	-308.0	227.0
477	S<192>	-324.0	110.0
478	S<191>	-340.0	227.0
479	S<190>	-356.0	110.0
480	S<189>	-372.0	227.0
481	S<188>	-388.0	110.0
482	S<187>	-404.0	227.0
483	S<186>	-420.0	110.0
484	S<185>	-436.0	227.0
485	S<184>	-452.0	110.0
486	S<183>	-468.0	227.0
487	S<182>	-484.0	110.0
488	S<181>	-500.0	227.0
489	S<180>	-516.0	110.0
490	S<179>	-532.0	227.0
491	S<178>	-548.0	110.0
492	S<177>	-564.0	227.0
493	S<176>	-580.0	110.0
494	S<175>	-596.0	227.0
495	S<174>	-612.0	110.0
496	S<173>	-628.0	227.0
497	S<172>	-644.0	110.0
498	S<171>	-660.0	227.0
499	S<170>	-676.0	110.0
500	S<169>	-692.0	227.0

No.	Pad name	X	Y
501	S<168>	-708.0	110.0
502	S<167>	-724.0	227.0
503	S<166>	-740.0	110.0
504	S<165>	-756.0	227.0
505	S<164>	-772.0	110.0
506	S<163>	-788.0	227.0
507	S<162>	-804.0	110.0
508	S<161>	-820.0	227.0
509	S<160>	-836.0	110.0
510	S<159>	-852.0	227.0
511	S<158>	-868.0	110.0
512	S<157>	-884.0	227.0
513	S<156>	-900.0	110.0
514	S<155>	-916.0	227.0
515	S<154>	-932.0	110.0
516	S<153>	-948.0	227.0
517	S<152>	-964.0	110.0
518	S<151>	-980.0	227.0
519	S<150>	-996.0	110.0
520	S<149>	-1012.0	227.0
521	S<148>	-1028.0	110.0
522	S<147>	-1044.0	227.0
523	S<146>	-1060.0	110.0
524	S<145>	-1076.0	227.0
525	S<144>	-1092.0	110.0
526	S<143>	-1108.0	227.0
527	S<142>	-1124.0	110.0
528	S<141>	-1140.0	227.0
529	S<140>	-1156.0	110.0
530	S<139>	-1172.0	227.0
531	S<138>	-1188.0	110.0
532	S<137>	-1204.0	227.0
533	S<136>	-1220.0	110.0
534	S<135>	-1236.0	227.0
535	S<134>	-1252.0	110.0
536	S<133>	-1268.0	227.0
537	S<132>	-1284.0	110.0
538	S<131>	-1300.0	227.0
539	S<130>	-1316.0	110.0
540	S<129>	-1332.0	227.0
541	S<128>	-1348.0	110.0
542	S<127>	-1364.0	227.0
543	S<126>	-1380.0	110.0
544	S<125>	-1396.0	227.0
545	S<124>	-1412.0	110.0
546	S<123>	-1428.0	227.0
547	S<122>	-1444.0	110.0
548	S<121>	-1460.0	227.0
549	S<120>	-1476.0	110.0
550	S<119>	-1492.0	227.0

No.	Pad name	X	Y
551	S<118>	-1508.0	110.0
552	S<117>	-1524.0	227.0
553	S<116>	-1540.0	110.0
554	S<115>	-1556.0	227.0
555	S<114>	-1572.0	110.0
556	S<113>	-1588.0	227.0
557	S<112>	-1604.0	110.0
558	S<111>	-1620.0	227.0
559	S<110>	-1636.0	110.0
560	S<109>	-1652.0	227.0
561	S<108>	-1668.0	110.0
562	S<107>	-1684.0	227.0
563	S<106>	-1700.0	110.0
564	S<105>	-1716.0	227.0
565	S<104>	-1732.0	110.0
566	S<103>	-1748.0	227.0
567	S<102>	-1764.0	110.0
568	S<101>	-1780.0	227.0
569	S<100>	-1796.0	110.0
570	S<99>	-1812.0	227.0
571	S<98>	-1828.0	110.0
572	S<97>	-1844.0	227.0
573	S<96>	-1860.0	110.0
574	S<95>	-1876.0	227.0
575	S<94>	-1892.0	110.0
576	S<93>	-1908.0	227.0
577	S<92>	-1924.0	110.0
578	S<91>	-1940.0	227.0
579	S<90>	-1956.0	110.0
580	S<89>	-1972.0	227.0
581	S<88>	-1988.0	110.0
582	S<87>	-2004.0	227.0
583	S<86>	-2020.0	110.0
584	S<85>	-2036.0	227.0
585	S<84>	-2052.0	110.0
586	S<83>	-2068.0	227.0
587	S<82>	-2084.0	110.0
588	S<81>	-2100.0	227.0
589	S<80>	-2116.0	110.0
590	S<79>	-2132.0	227.0
591	S<78>	-2148.0	110.0
592	S<77>	-2164.0	227.0
593	S<76>	-2180.0	110.0
594	S<75>	-2196.0	227.0
595	S<74>	-2212.0	110.0
596	S<73>	-2228.0	227.0
597	S<72>	-2244.0	110.0
598	S<71>	-2260.0	227.0
599	S<70>	-2276.0	110.0
600	S<69>	-2292.0	227.0

Preliminary

No.	Pad name	X	Y
601	S<68>	-2308.0	110.0
602	S<67>	-2324.0	227.0
603	S<66>	-2340.0	110.0
604	S<65>	-2356.0	227.0
605	S<64>	-2372.0	110.0
606	S<63>	-2388.0	227.0
607	S<62>	-2404.0	110.0
608	S<61>	-2420.0	227.0
609	S<60>	-2436.0	110.0
610	S<59>	-2452.0	227.0
611	S<58>	-2468.0	110.0
612	S<57>	-2484.0	227.0
613	S<56>	-2500.0	110.0
614	S<55>	-2516.0	227.0
615	S<54>	-2532.0	110.0
616	S<53>	-2548.0	227.0
617	S<52>	-2564.0	110.0
618	S<51>	-2580.0	227.0
619	S<50>	-2596.0	110.0
620	S<49>	-2612.0	227.0
621	S<48>	-2628.0	110.0
622	S<47>	-2644.0	227.0
623	S<46>	-2660.0	110.0
624	S<45>	-2676.0	227.0
625	S<44>	-2692.0	110.0
626	S<43>	-2708.0	227.0
627	S<42>	-2724.0	110.0
628	S<41>	-2740.0	227.0
629	S<40>	-2756.0	110.0
630	S<39>	-2772.0	227.0
631	S<38>	-2788.0	110.0
632	S<37>	-2804.0	227.0
633	S<36>	-2820.0	110.0
634	S<35>	-2836.0	227.0
635	S<34>	-2852.0	110.0
636	S<33>	-2868.0	227.0
637	S<32>	-2884.0	110.0
638	S<31>	-2900.0	227.0
639	S<30>	-2916.0	110.0
640	S<29>	-2932.0	227.0
641	S<28>	-2948.0	110.0
642	S<27>	-2964.0	227.0
643	S<26>	-2980.0	110.0
644	S<25>	-2996.0	227.0
645	S<24>	-3012.0	110.0
646	S<23>	-3028.0	227.0
647	S<22>	-3044.0	110.0
648	S<21>	-3060.0	227.0
649	S<20>	-3076.0	110.0
650	S<19>	-3092.0	227.0

No.	Pad	X	Y
651	S<18>	-3108.0	110.0
652	S<17>	-3124.0	227.0
653	S<16>	-3140.0	110.0
654	S<15>	-3156.0	227.0
655	S<14>	-3172.0	110.0
656	S<13>	-3188.0	227.0
657	S<12>	-3204.0	110.0
658	S<11>	-3220.0	227.0
659	S<10>	-3236.0	110.0
660	S<9>	-3252.0	227.0
661	S<8>	-3268.0	110.0
662	S<7>	-3284.0	227.0
663	S<6>	-3300.0	110.0
664	S<5>	-3316.0	227.0
665	S<4>	-3332.0	110.0
666	S<3>	-3348.0	227.0
667	S<2>	-3364.0	110.0
668	S<1>	-3380.0	227.0
669	Dummy	-3396.0	110.0
670	Dummy	-3412.0	227.0
671	Dummy	-3428.0	110.0
672	Dummy	-3444.0	227.0
673	G<1>	-3460.0	110.0
674	G<3>	-3476.0	227.0
675	G<5>	-3492.0	110.0
676	G<7>	-3508.0	227.0
677	G<9>	-3524.0	110.0
678	G<11>	-3540.0	227.0
679	G<13>	-3556.0	110.0
680	G<15>	-3572.0	227.0
681	G<17>	-3588.0	110.0
682	G<19>	-3604.0	227.0
683	G<21>	-3620.0	110.0
684	G<23>	-3636.0	227.0
685	G<25>	-3652.0	110.0
686	G<27>	-3668.0	227.0
687	G<29>	-3684.0	110.0
688	G<31>	-3700.0	227.0
689	G<33>	-3716.0	110.0
690	G<35>	-3732.0	227.0
691	G<37>	-3748.0	110.0
692	G<39>	-3764.0	227.0
693	G<41>	-3780.0	110.0
694	G<43>	-3796.0	227.0
695	G<45>	-3812.0	110.0
696	G<47>	-3828.0	227.0
697	G<49>	-3844.0	110.0
698	G<51>	-3860.0	227.0
699	G<53>	-3876.0	110.0
700	G<55>	-3892.0	227.0

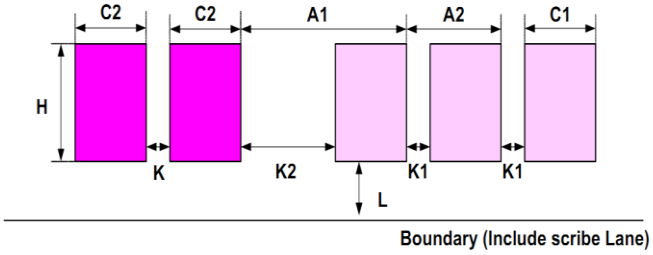
No.	Pad name	X	Y
701	G<57>	-3908.0	110.0
702	G<59>	-3924.0	227.0
703	G<61>	-3940.0	110.0
704	G<63>	-3956.0	227.0
705	G<65>	-3972.0	110.0
706	G<67>	-3988.0	227.0
707	G<69>	-4004.0	110.0
708	G<71>	-4020.0	227.0
709	G<73>	-4036.0	110.0
710	G<75>	-4052.0	227.0
711	G<77>	-4068.0	110.0
712	G<79>	-4084.0	227.0
713	G<81>	-4100.0	110.0
714	G<83>	-4116.0	227.0
715	G<85>	-4132.0	110.0
716	G<87>	-4148.0	227.0
717	G<89>	-4164.0	110.0
718	G<91>	-4180.0	227.0
719	G<93>	-4196.0	110.0
720	G<95>	-4212.0	227.0
721	G<97>	-4228.0	110.0
722	G<99>	-4244.0	227.0
723	G<101>	-4260.0	110.0
724	G<103>	-4276.0	227.0
725	G<105>	-4292.0	110.0
726	G<107>	-4308.0	227.0
727	G<109>	-4324.0	110.0
728	G<111>	-4340.0	227.0
729	G<113>	-4356.0	110.0
730	G<115>	-4372.0	227.0
731	G<117>	-4388.0	110.0
732	G<119>	-4404.0	227.0
733	G<121>	-4420.0	110.0
734	G<123>	-4436.0	227.0
735	G<125>	-4452.0	110.0
736	G<127>	-4468.0	227.0
737	G<129>	-4484.0	110.0
738	G<131>	-4500.0	227.0
739	G<133>	-4516.0	110.0
740	G<135>	-4532.0	227.0
741	G<137>	-4548.0	110.0
742	G<139>	-4564.0	227.0
743	G<141>	-4580.0	110.0
744	G<143>	-4596.0	227.0
745	G<145>	-4612.0	110.0
746	G<147>	-4628.0	227.0
747	G<149>	-4644.0	110.0
748	G<151>	-4660.0	227.0
749	G<153>	-4676.0	110.0
750	G<155>	-4692.0	227.0

No.	Pad name	X	Y
751	G<157>	-4708.0	110.0
752	G<159>	-4724.0	227.0
753	G<161>	-4740.0	110.0
754	Dummy	-4756.0	227.0
755	Dummy	-4772.0	110.0

Alignment mark	X	Y
Alignment_R	4841	-220
Alignment_L	-4841	-220

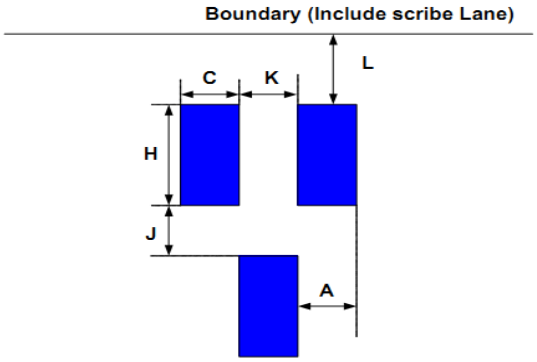
Preliminary

Input Pad



Item	Symbol	Size
Bump Pitch 1	A1	72.5um
Bump Pitch 2	A2	60um
Bump Width 1	C1	38um
Bump Width 2	C2	33um
Bump Height	H	73um
Bump Gap	K	17um
Bump Gap1	K1	22um
Bump Gap2	K2	34.5um
Bump Area 1	C1×H	3344um^2
Bump Area 2	C2×H	2904um^2
Chip Boundary(include	L	50um

Output Pad



Item	Symbol	Size
Bump Pitch	A	16um
Bump Width	C	13um
Bump Height	H	83um
Bump Gap1(Vertical)	J	18um
Bump Gap(Horizontal)	K	19um
Bump Area	C×H	1568um^2
Chip Boundary	L	50um

Pre-liminary

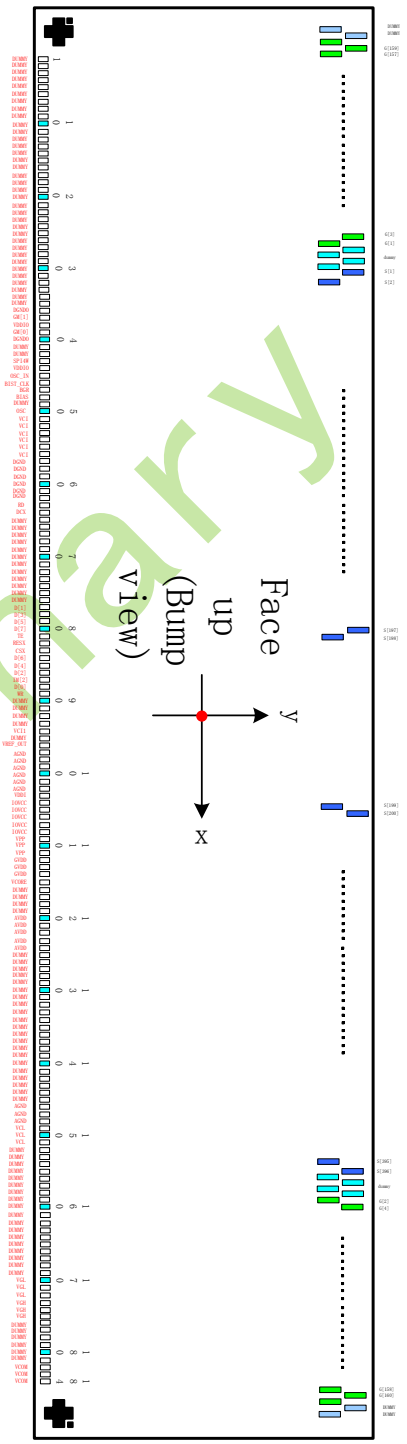
Chip Size: 10080um x 670um

Chip thickness: 280um(typ.)

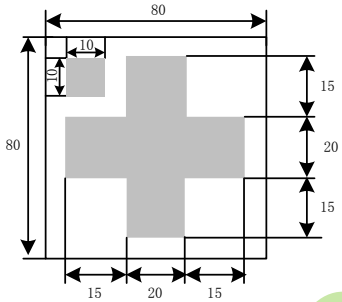
Pad Location: Pad Center.

Coordinate Origin: Chip center

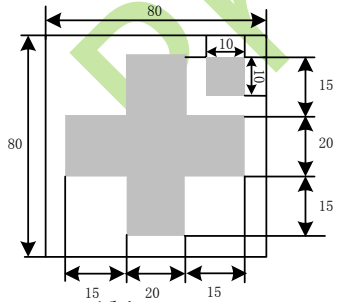
Au bump height: 12um(typ.)



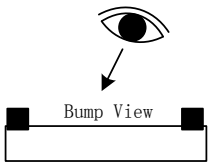
Alignment Marks



Alignment Mark:A1



Alignment Mark:A2



Preliminary

4. Interface setting

4.1. MCU interfaces

GC9106 provides the 8-bit parallel system interface for 8080, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [2] and the bit formal per pixel color order is selected by IFPF [2:0] bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins SPI4W, IM2, as shown in the following table.

SPI4W	IM2	MCU-Interface Mode	Pins in use	
			Register/Content	GRAM
X	1	8080 MCU 8-bit bus interface	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	serial interface 3 line	SCL,SDA,CSX	
1	0	serial interface 4 line	SCL,SDA,CSX,RS	

Preliminary

4.1.2. 8080 Series Parallel Interface

GC9106 can be accessed via 8-bit MCU 8080 series parallel interface. The chip select CSX (active low) is used to enable or disable GC9106 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D [7:0] is parallel data bus.

GC9106 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [7:0] bits are display RAM data or command's parameters. When D/CX='0', D [7:0] bits are commands.

The 8080 series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080 Interface selection is done when P68 pin is low state (DGND level). The selection of 8080 series parallel interface is shown as the table in the following.

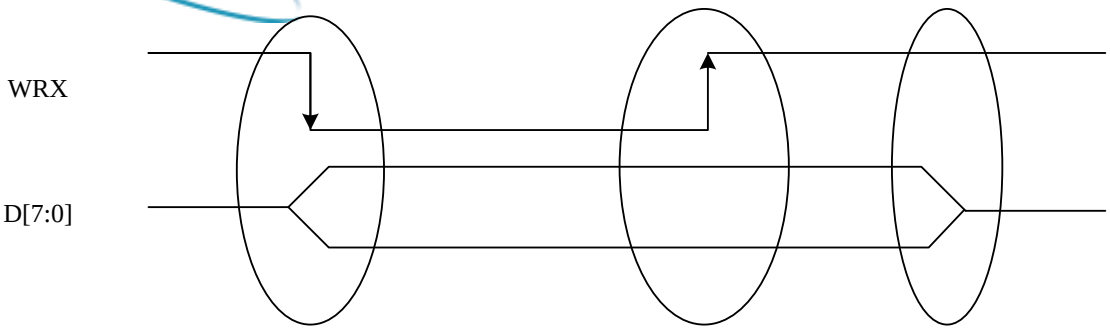
SPI4W	IM2	MPU-interface	CSX	WRX	RDX	D/CX	Function
X	1	8-bit parallel	"L"	↑	"H"	"L"	Write command code.
			"L"	"H"	↑	"H"	Read internal status.
			"L"	↑	"H"	"H"	Write parameter or display data.
			"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080 MCU interface.

Preliminary

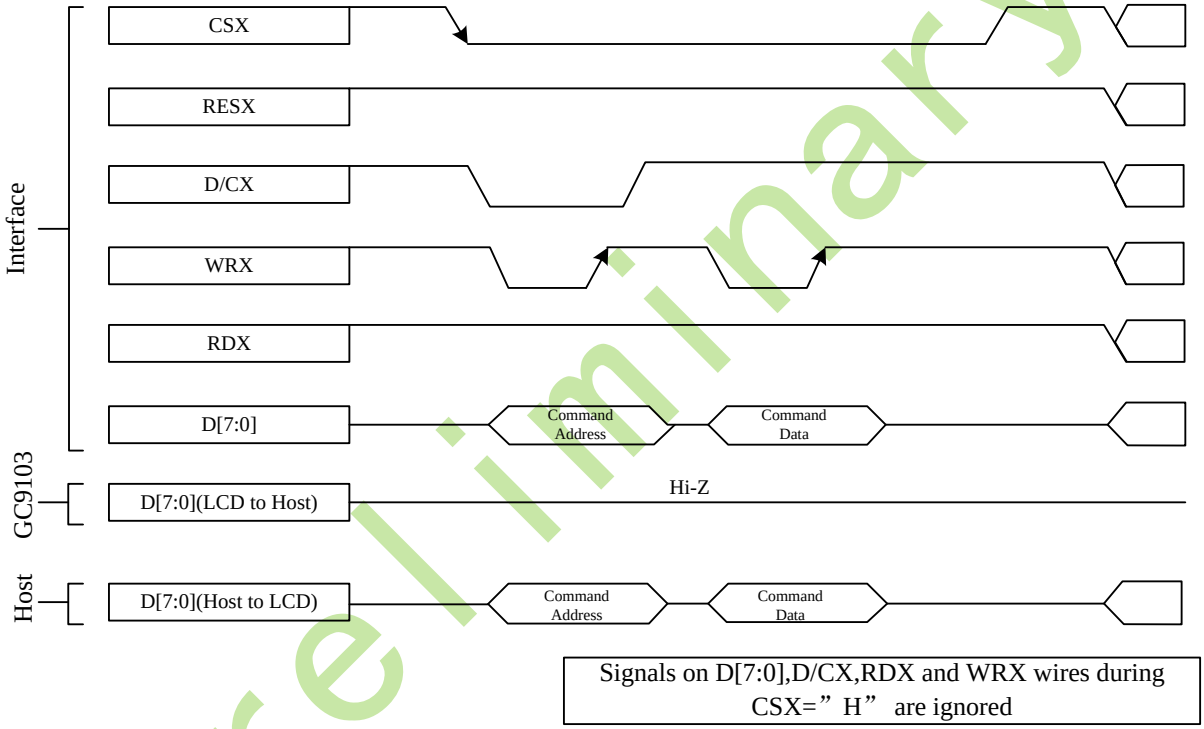


The host assertsD[7:0] lines when there is falling edge of WRX

read D[7:0] lines when there is rising edge of WRX

The host negates D[7:0] lines

Note: WRX is an unsynchronized signal (It can be stopped)

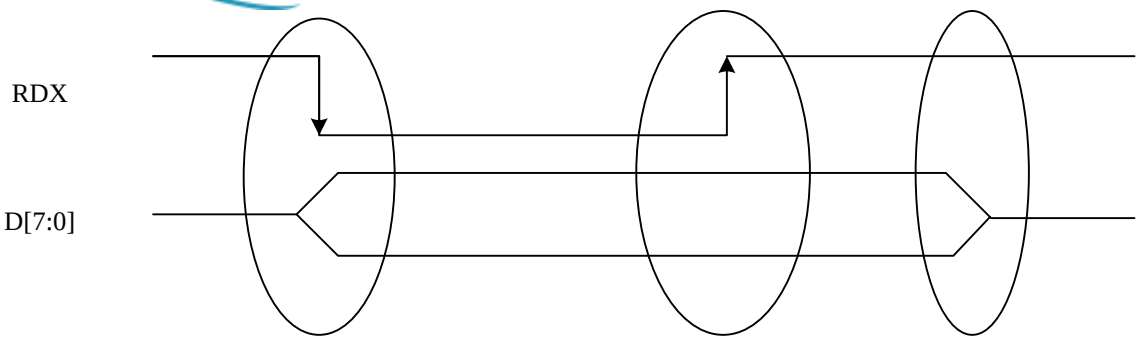


Preliminary

4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.

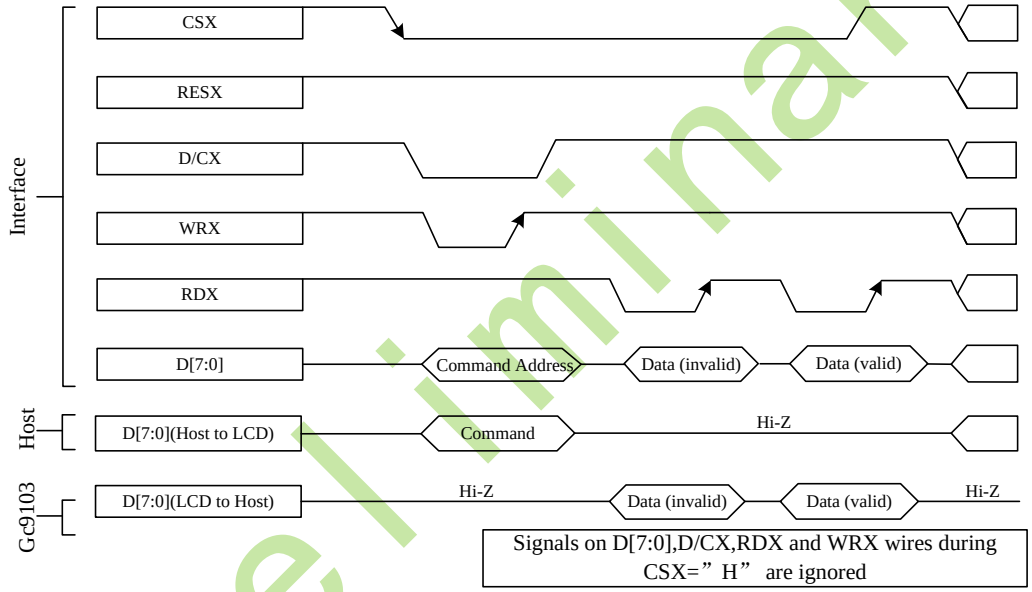


IC assers D[7:0] lines when there is a falling edge of RDX

The host reads D[7:0] lines when there is a rising edge of RDX

IC negates D[7:0] lines

Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

Preliminary

4.1.5. Serial Interface

The selection of interface is done by IM2 bit. Please refer to the Table in the following.

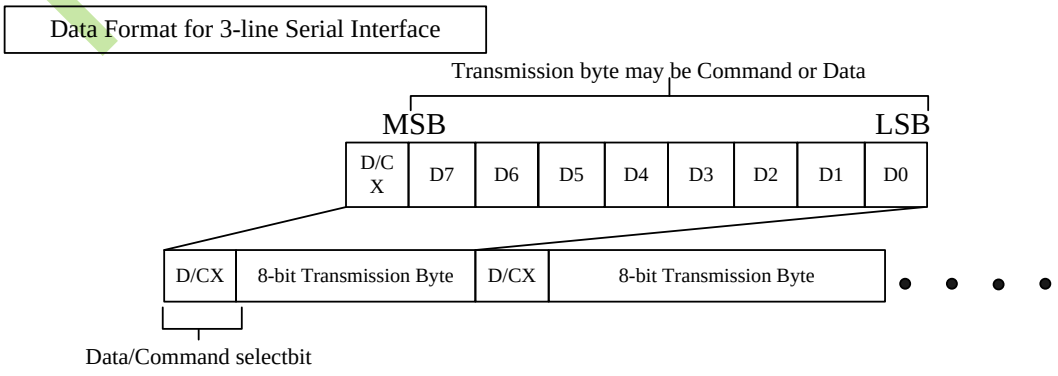
IM2	SPI4W	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	0	3-line serial interface	"L"	-	↑	Read/Write command, parameter or display data.
0	1	4-line serial interface	"L"	"H/L"	↑	Read/Write command, parameter or display data.

GC9106 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9106. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDA) for data transmission. The data bus (D [7:1]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

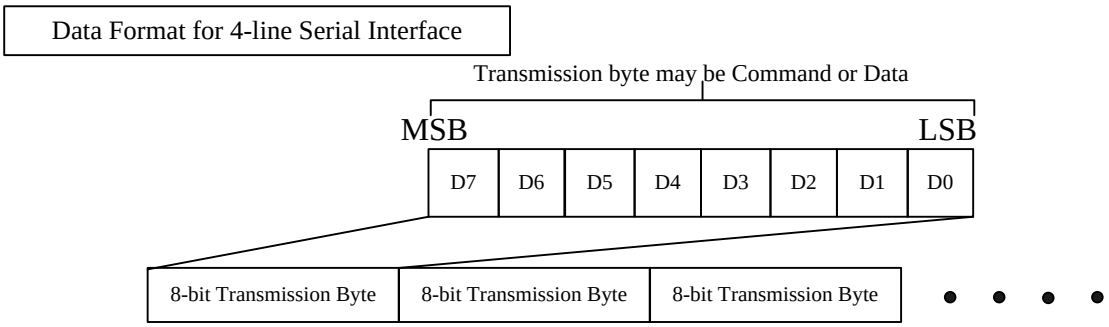
4.1.6. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9106. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command),or command register as parameter.

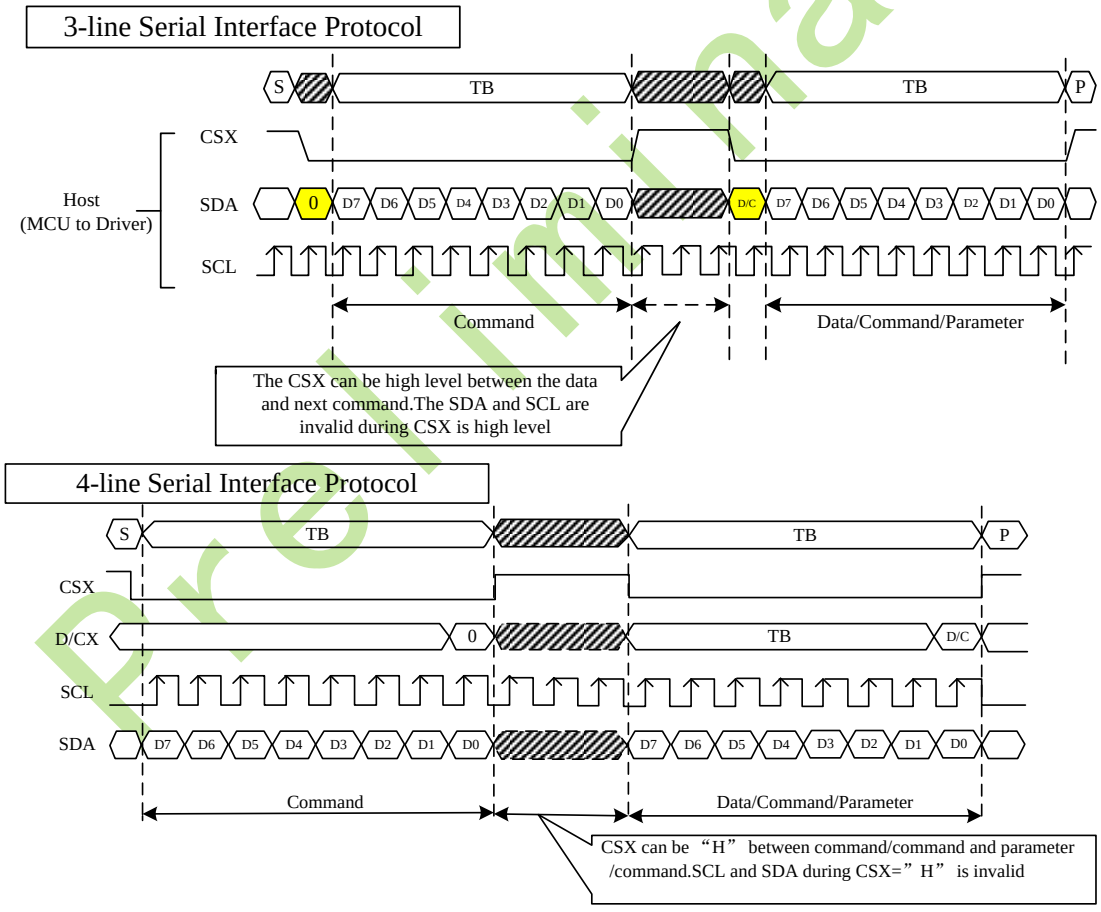
Any instruction can be sent in any order to GC9106 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.



Preliminary



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9106 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



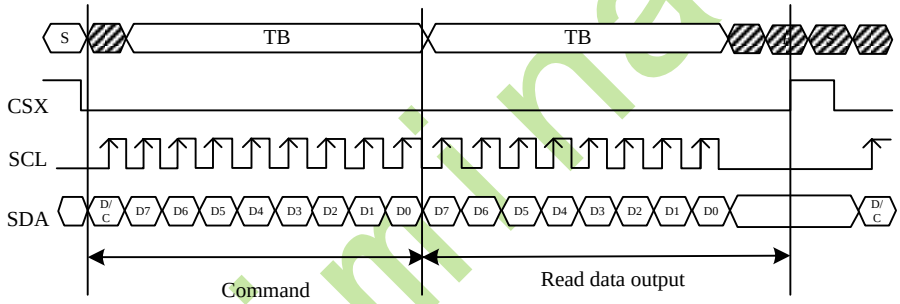
Preliminary

4.1.7. Read Cycle Sequence

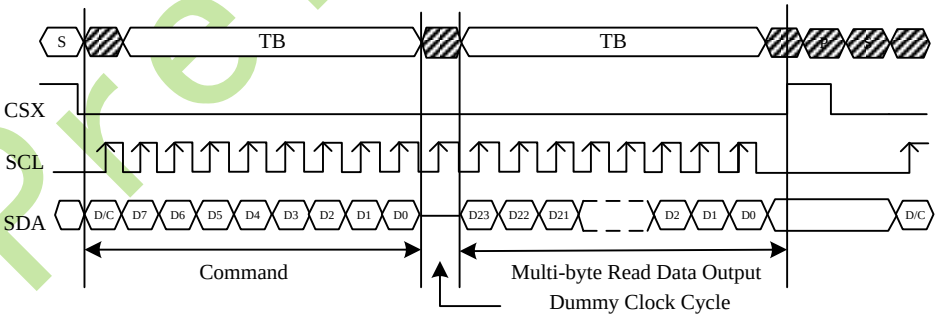
The read mode of interface means that the host reads register's parameter from GC9106. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9106 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)

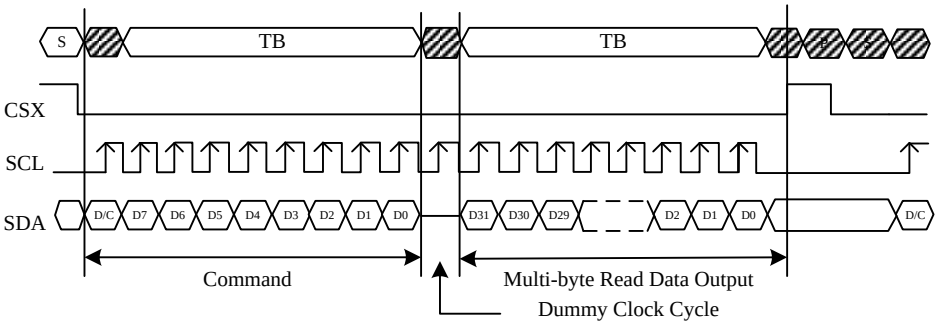


3-wire Serial Protocol (for RDDID command:24-bit read)



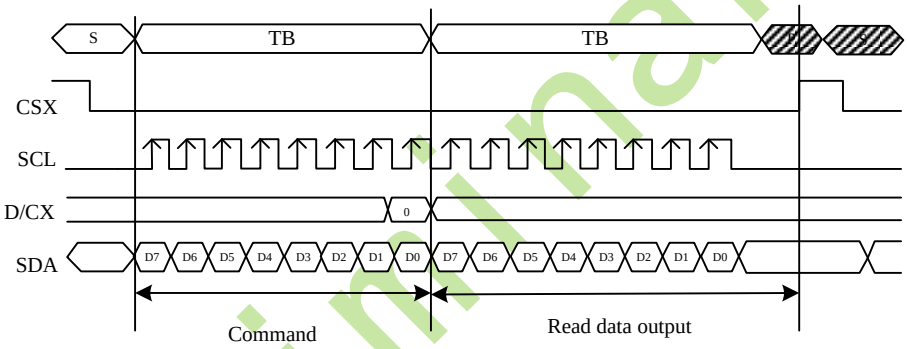
Preliminary

3-wire Serial Protocol (for RDDST command:32-bit read)

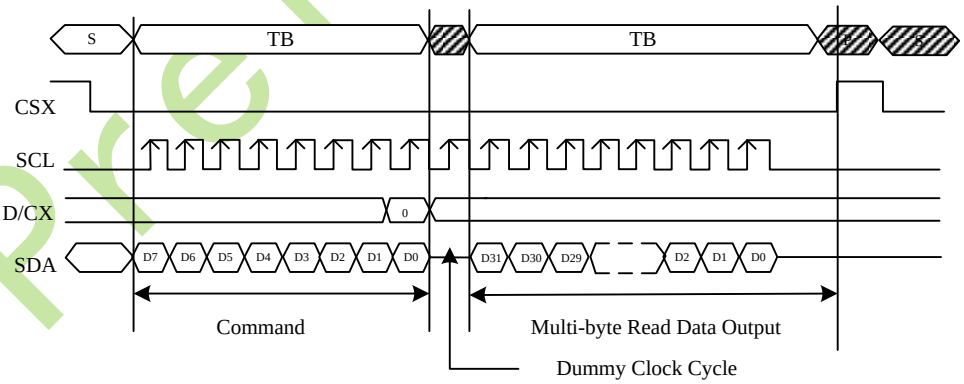


4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



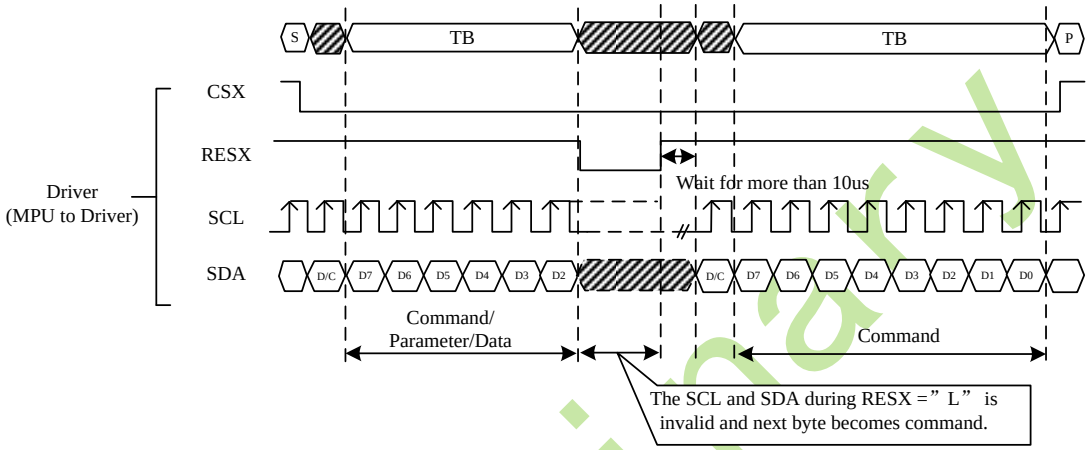
4-wire Serial Protocol (for RDDST command:32-bit read)



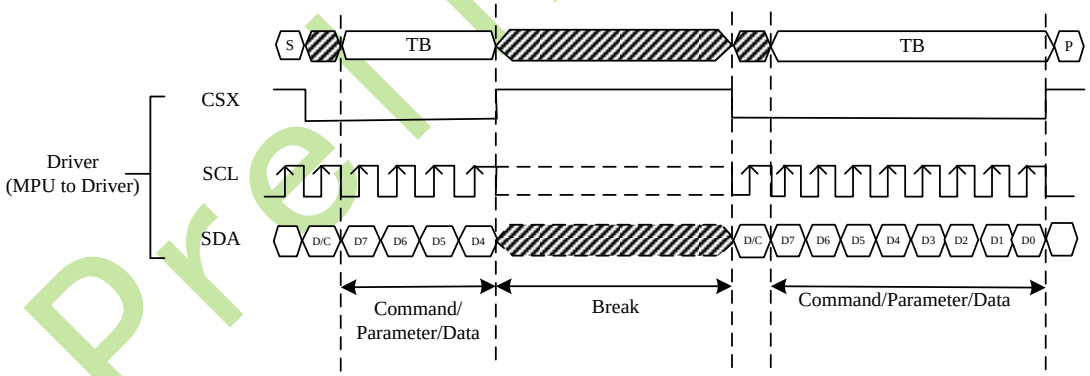
Preliminary

4.1.8. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

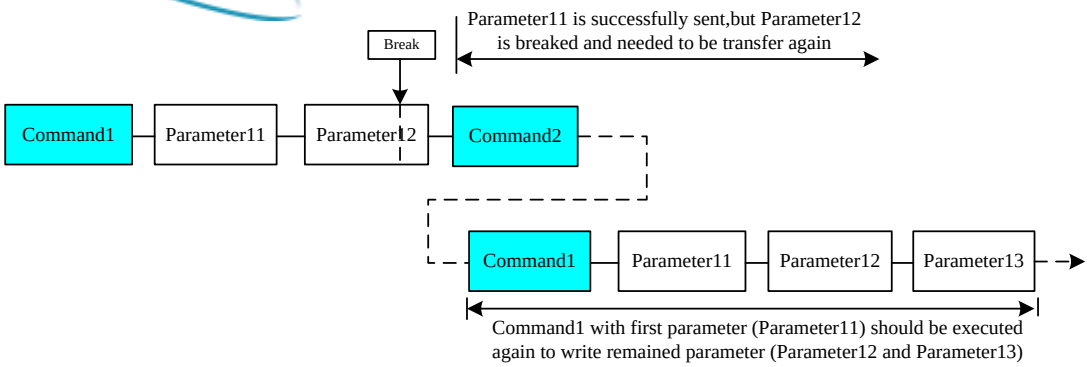


If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

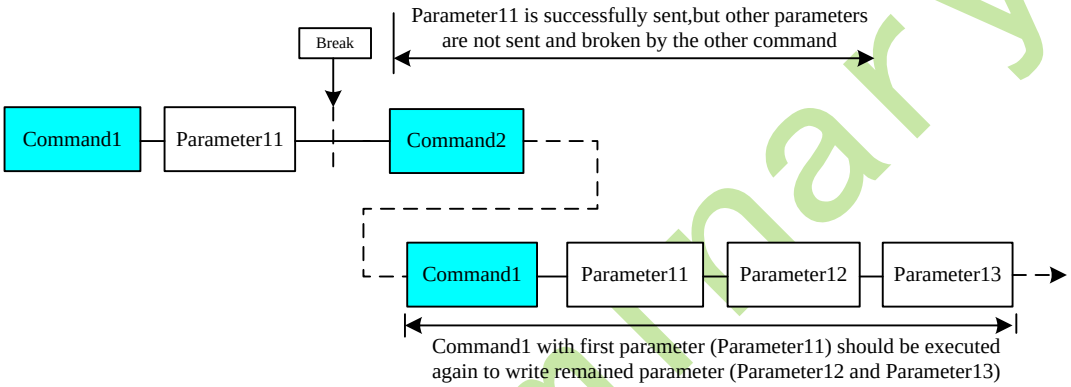


If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Preliminary



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

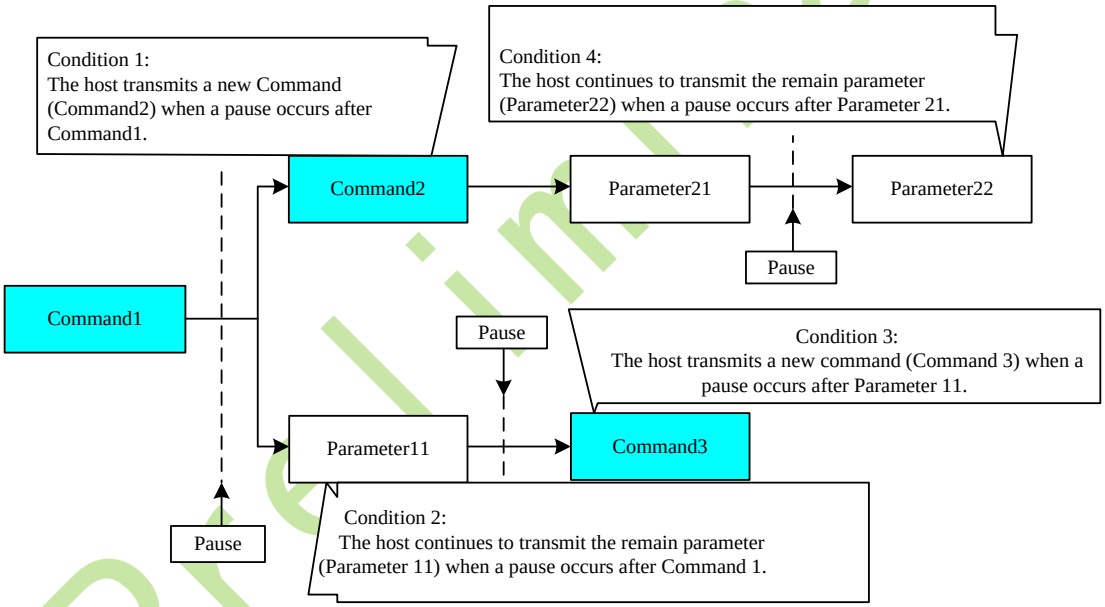


Preliminary

4.1.9. Data Transfer Pause

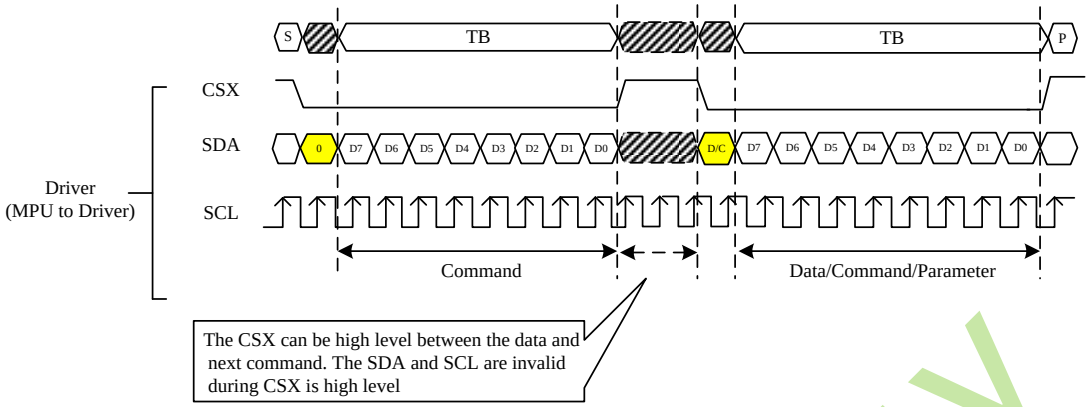
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9106 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

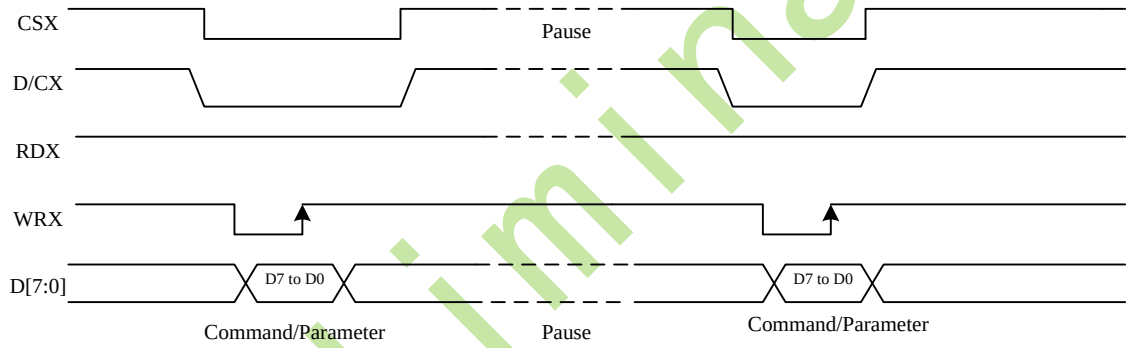


Preliminary

4.1.10. Serial Interface Pause



4.1.11. Parallel Interface Pause

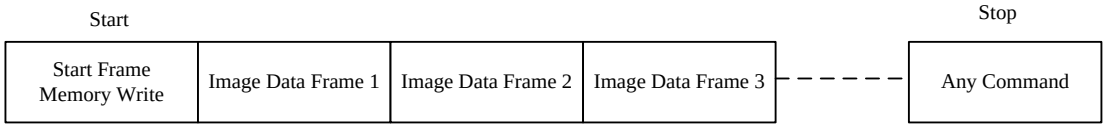


4.1.12. Data Transfer Mode

GC9106 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.13. Data Transfer Method 1

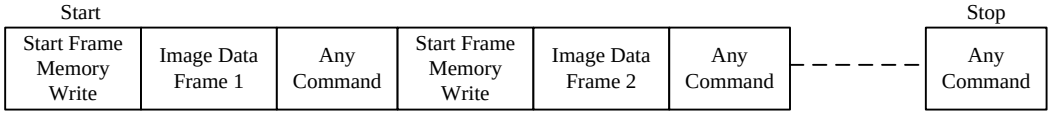
The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



Preliminary

4.1.14. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

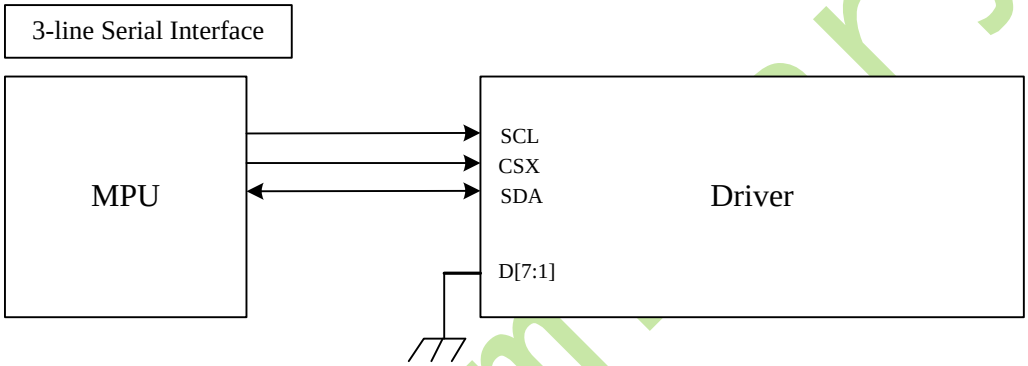
Preliminary

4.2. Display Data Format

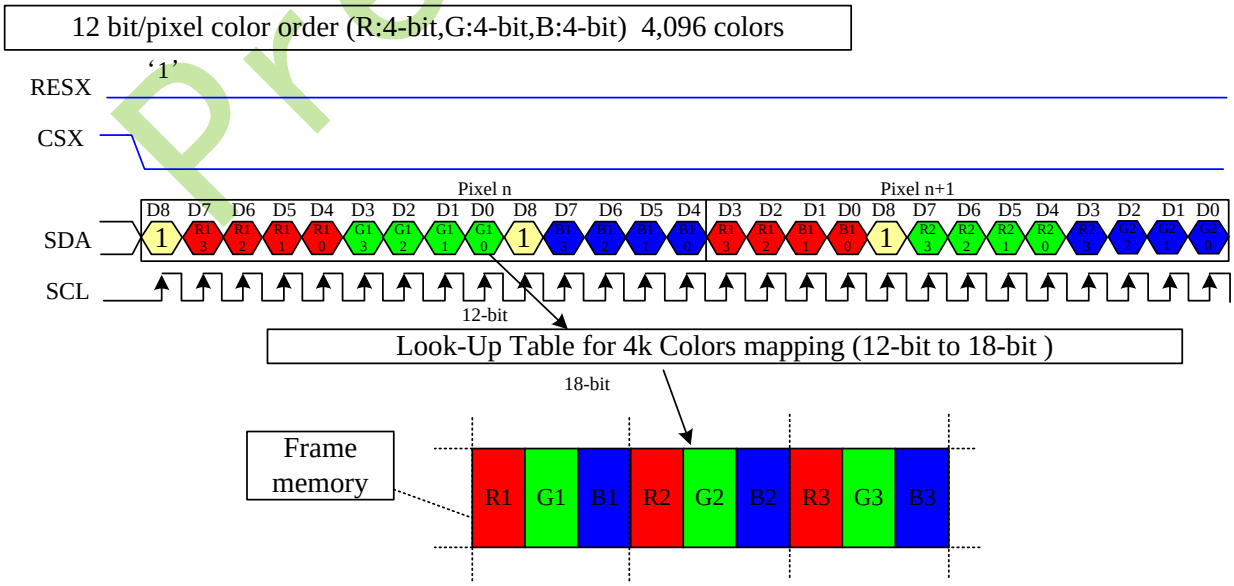
GC9106 supplies 8-bit parallel MCU interface with 8080 series, 3-/4-line serial interface. The parallel MCU interface and serial interface mode can be selected by external pins IM2 and SPI4W.

4.2.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9106 can be used by setting external pin as IM2 to “0” and SPI4W to “0”. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.
-4k color, RGB 4, 4, 4, -bits input
-65k colors, RGB 5, 6, 5 -bits input
-262k colors, RGB 6, 6, 6 -bits input.



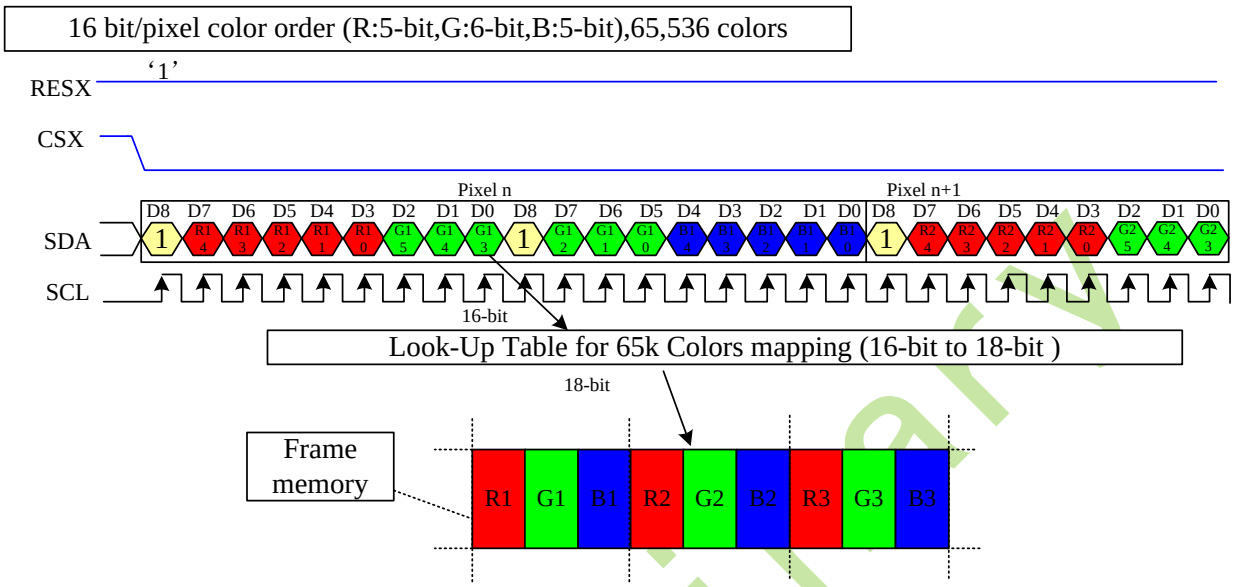
Preliminary

Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

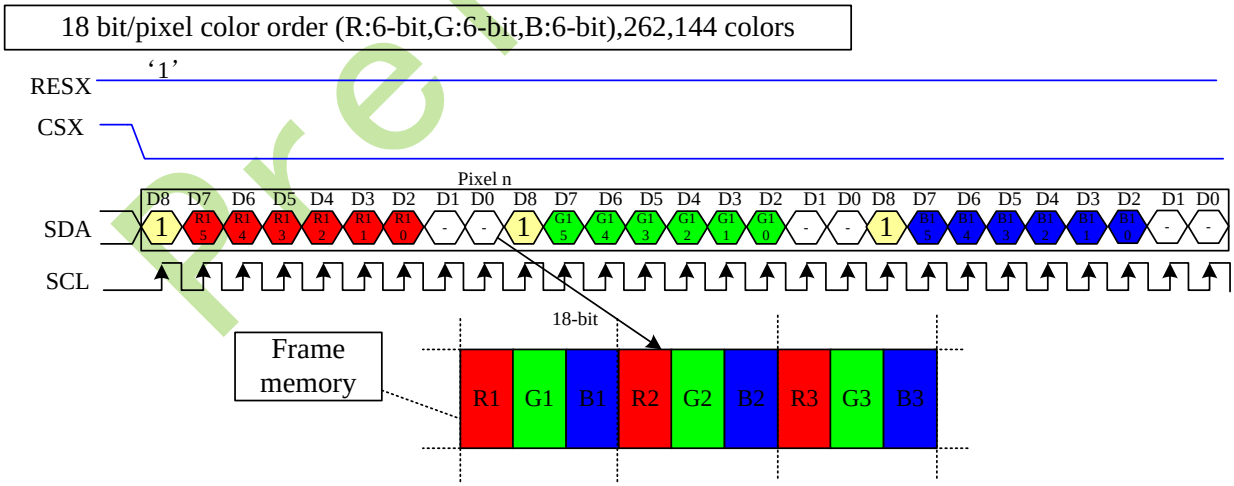


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

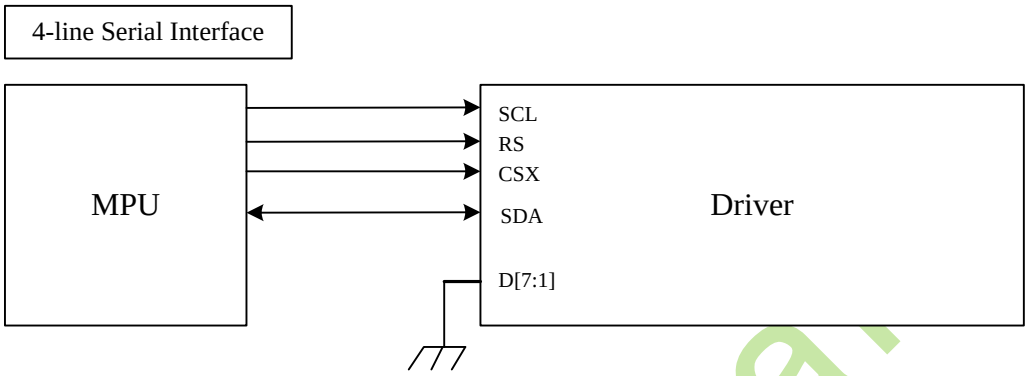
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= don't care - Can be set "0" or "1".

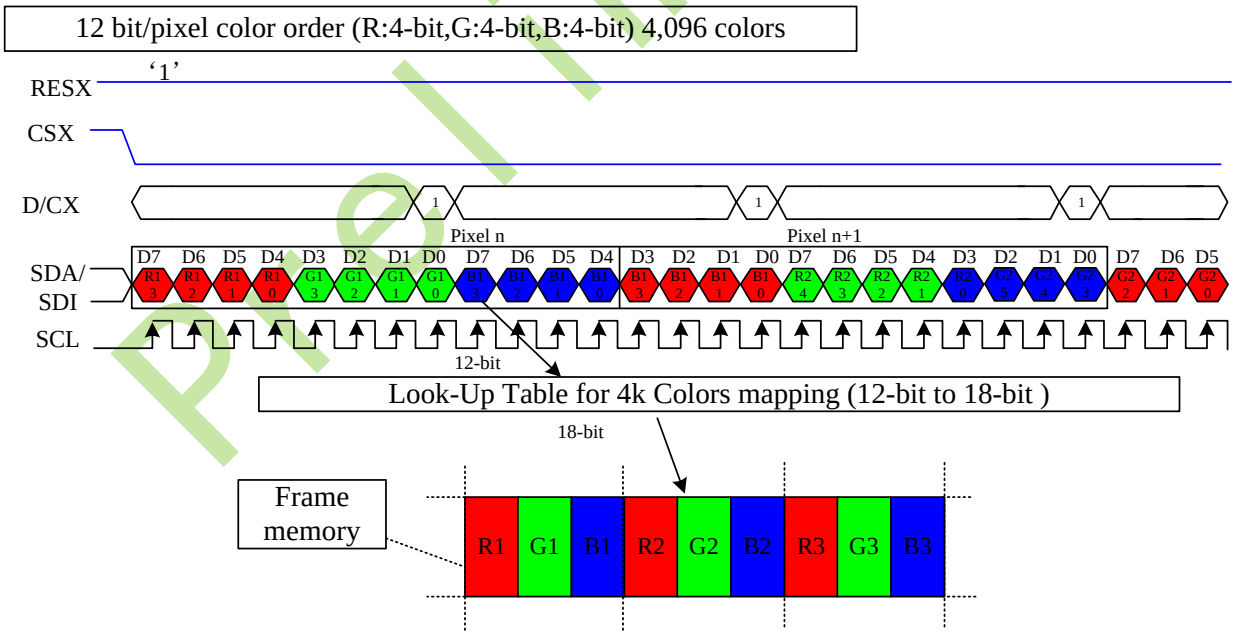
Preliminary

4.2.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9106 can be used by setting external pin as IM2 to “0” and SPI4W to “1”. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.
-4Kk color, RGB 4, 4, 4 -bits input.
-65k colors, RGB 5, 6, 5 -bits input.
-262k colors, RGB 6, 6, 6 -bits input.



Note 1: The pixel data with 12-bit color depth information.

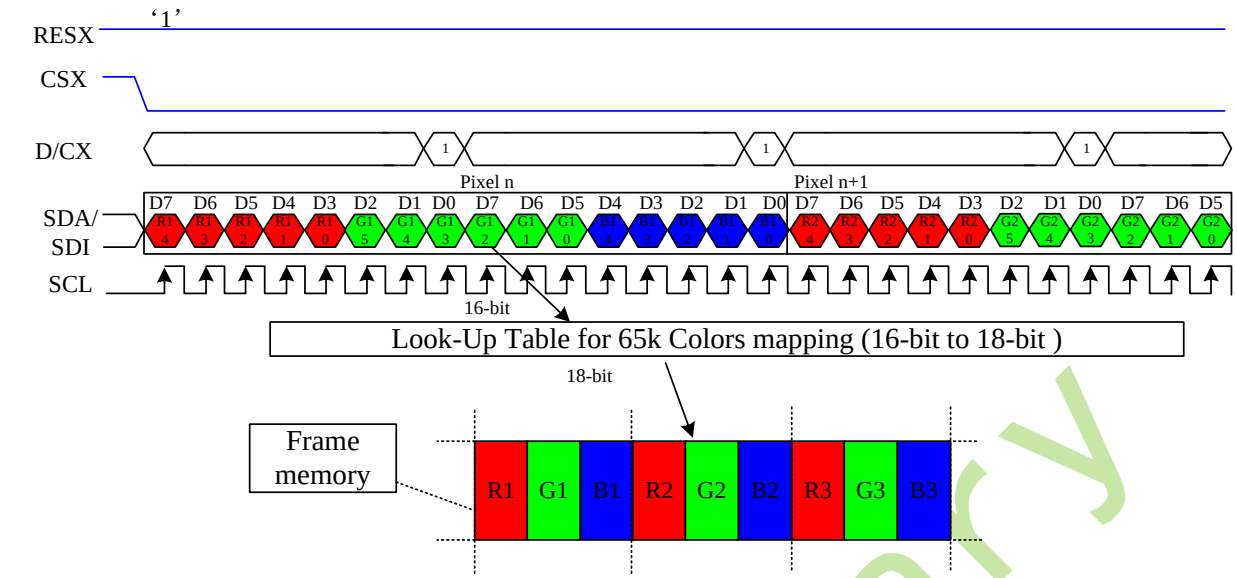
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= don’t care –Can be set “0” or “1”.

Preliminary

16 bit/pixel color order (R:5-bit,G:6-bit,B:5-bit),65,536 colors



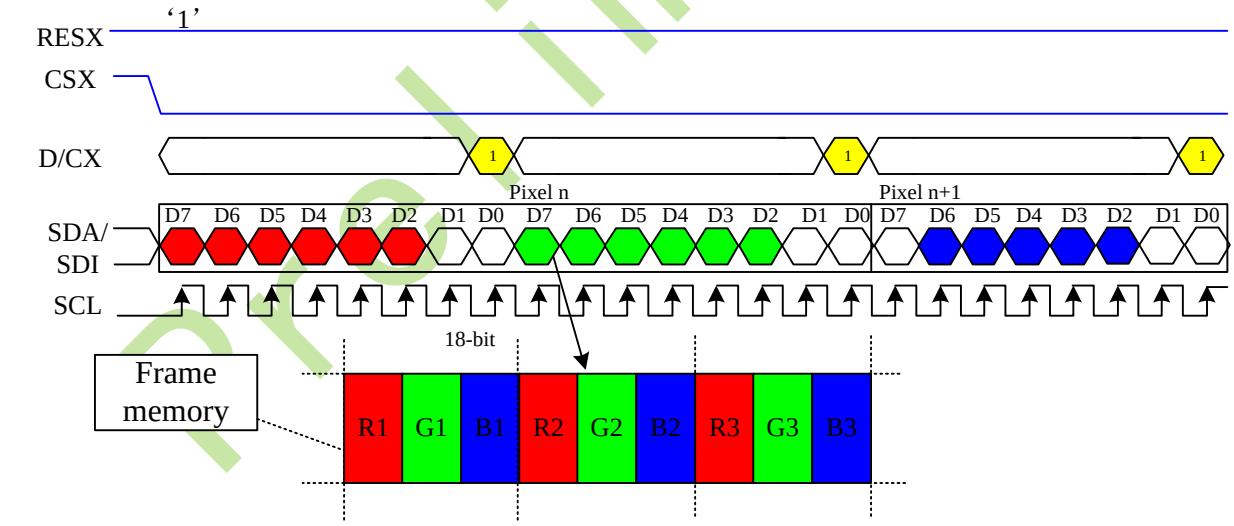
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit,G:6-bit,B:6-bit),65,536 colors



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

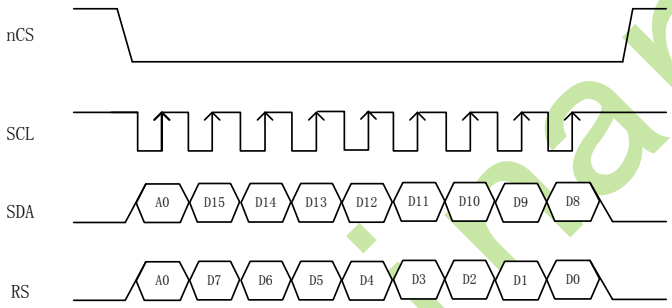
Preliminary

4.2.3. 2-data line mode

This mode is active when 2data_en (A7h[3]) set to “1” in 3-wire. Only frame pixle data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

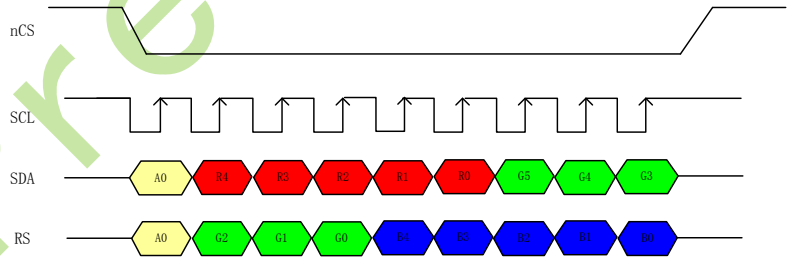
The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and RS are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and RS in the sequence A0, D7 to D0. The GC9106 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.



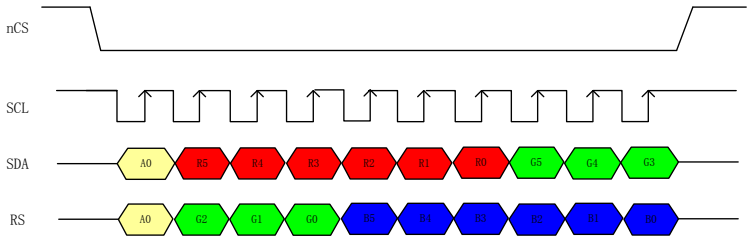
Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (A7h[2:0]) .

RGB565 1pixle/transition (65K color, 2data_mdt[2:0]=“000”)

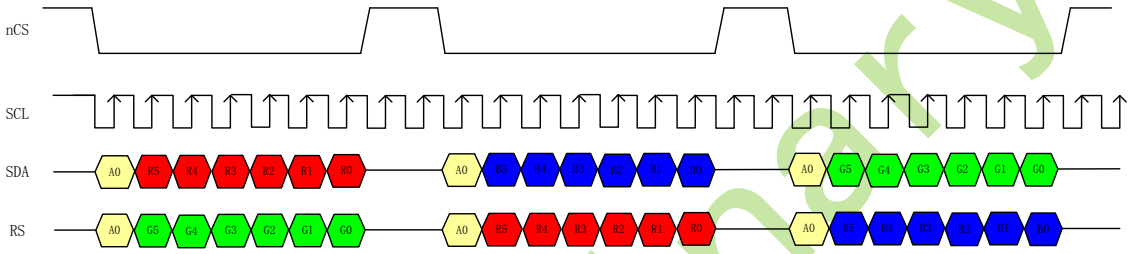


RGB666 1pixle/transition (262K color, 2data_mdt[2:0]=“001”)

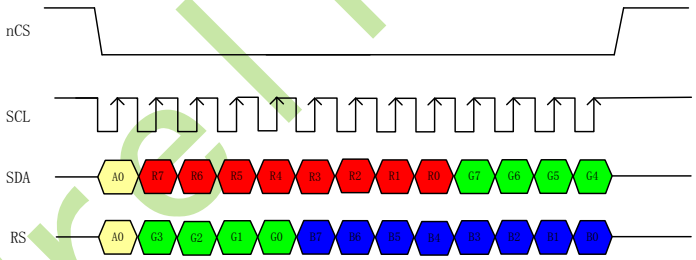
Preliminary



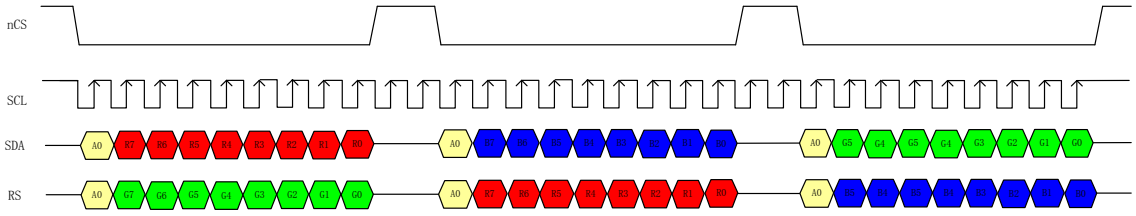
RGB666 2/3pixle/transition (262K color, 2data_mdt[2:0]=“010”)



RGB888 1pixle/transition (4M color, 2data_mdt[2:0]=“100”)



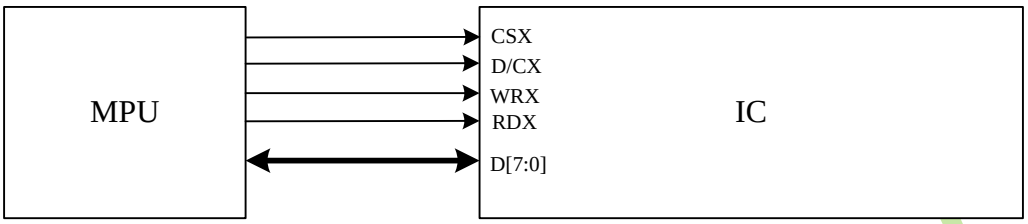
RGB888 2/3pixle/transition (4M color, 2data_mdt[2:0]=“110”)



Preliminary

4.2.4. 8-bit Parallel MCU Interface

The 8-bit parallel bus interface of GC9106 can be used by setting external pin as IM [2:0] to“000”.The following shown figure is the example of interface with 8-bits MCU system interface.



Different display data formats are available for three color depths supported by listed below.
- 4K-Color, RGB 4, 4, 4, -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4K color: 12-bit/pixel (RGB 4-4-4 bits input)

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when IFPF [2:0] bits of 3Ah register are set to “011”.

Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R3	0B3	1G3	2R4	2R3	3G3	…
D6	C6	0R2	0B2	1G2	2R3	2R2	3G2	…
D5	C5	0R1	0B1	1G1	2R2	2R1	3G1	…
D4	C4	0R0	0B0	1G0	2R1	2R0	3G0	…
D3	C3	0G3	1R3	1B3	2G3	3R3	3B3	…
D2	C2	0G2	1R2	1B2	2G2	3R2	3B2	…
D1	C1	0G1	1R1	1B1	2G1	3R1	3B1	…
D0	C0	0G0	1R0	1B0	2G0	3R0	3B0	…

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when IFPF [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…
D/CX	0	1	1	1	1	…
D7	C7	0R4	0G2	1R4	1G2	…
D6	C6	0R3	0G1	1R3	1G1	…
D5	C5	0R2	0G0	1R2	1G0	…

Preliminary

D4	C4	0R1	0B4	1R1	1B4	…
D3	C3	0R0	0B3	1R0	1B3	…
D2	C2	0G5	0B2	1G5	1B2	…
D1	C1	0G4	0B1	1G4	1B1	…
D0	C0	0G3	0B0	1G3	1B0	…

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when IFPF [2:0] bits of 3Ah register are set to “110”.

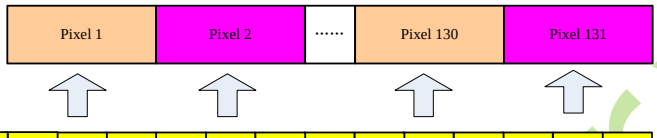
Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R5	0G5	0B5	1R5	1G5	1B5	…
D6	C6	0R4	0G4	0B4	1R4	1G4	1B4	…
D5	C5	0R3	0G3	0B3	1R3	1G3	1B3	…
D4	C4	0R2	0G2	0B2	1R2	1G2	1B2	…
D3	C3	0R1	0G1	0B1	1R1	1G1	1B1	…
D2	C2	0R0	0G0	0B0	1R0	1G0	1B0	…
D1	C1							…
D0	C0							…

Preliminary

5. Function Description

5.1. Display data GRAM mapping

5.1.1. 132RGBx132 resolution (GM = “01”)



Gate Out	Source Out		S1	S2	S3	S4	S5	S6	……	S391	S392	S393	S394	S395	S396		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
1	0	131	R0	G0	B0	R1	G1	B1	……	R130	G130	B130	R131	G131	B131	0	131
2	1	130							……							1	130
3	2	129							……							2	129
4	3	128							……							3	128
5	4	127							……							4	127
6	5	126							……							5	126
7	6	125							……							6	125
8	7	124							……							7	124
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
125	124	7							……							124	7
126	125	6							……							125	6
127	126	5							……							126	5
128	127	4							……							127	4
129	128	3							……							128	3
130	129	2							……							129	2
131	130	1							……							130	1
132	131	0							……							131	0
	CA	MX= ‘0’	0			1			……	130			131				
		MX= ‘1’	131			130			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

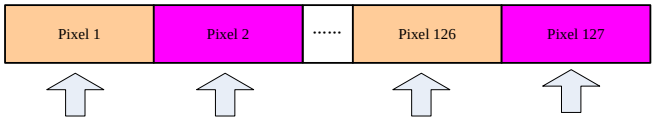
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.1.2. 128RGBx160 resolution (GM = “11”)



Gate Out	Source Out		S7	S8	S9	S10	S11	S12	……	S385	S386	S387	S388	S389	S390		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
2	0	159	R0	G0	B0	R1	G1	B1	……	R126	G126	B126	R127	G127	B127	0	159
3	1	158							……							1	158
4	2	157							……							2	157
5	3	156							……							3	156
6	4	155							……							4	155
7	5	154							……							5	154
8	6	153							……							6	153
9	7	152							……							7	152
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
154	152	7							……							152	7
155	153	6							……							153	6
156	154	5							……							154	5
157	155	4							……							155	4
158	156	3							……							156	3
159	157	2							……							157	2
160	158	1							……							158	1
161	159	0							……							159	0
	CA	MX= ‘0’	0			1			……	126			127				
		MX= ‘1’	127			126			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

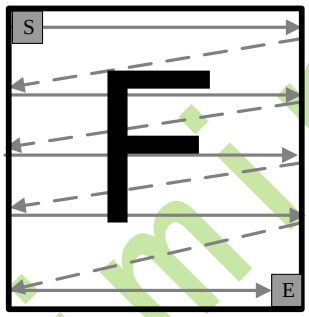
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

Pre

5.2. Address Counter (AC) of GRAM

The GC9106 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

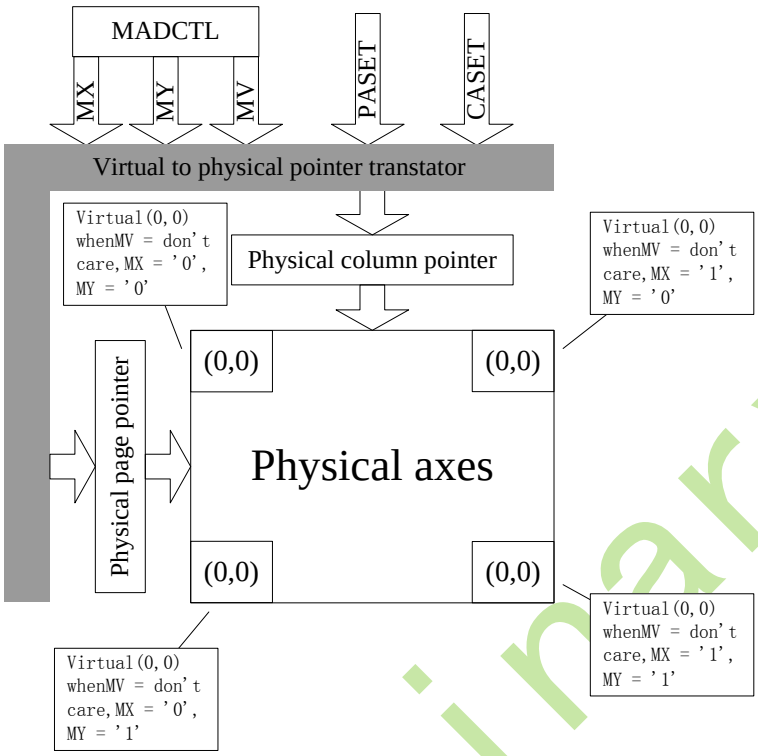
To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.
Image data sending order from host and data stream update as shown in the following figure



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Preliminary

Image data writing control:



For each image orientation, the controls for the column and page counters apply as below:

condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start column"	Return to "Start Page"

Preliminary

5.2.1 128RGBx160 (GM == '11')

CASET and PASET control for physical column/page pointers:

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161 - Physical Page Pointer)
0	1	0	Direct to (131 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (131 - Physical Column Pointer)	Direct to (161 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (131 - Physical Column Pointer)
1	1	1	Direct to (161 - Physical Page Pointer)	Direct to (131 - Physical Column Pointer)

Preliminary

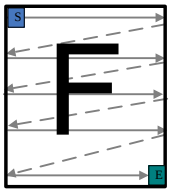
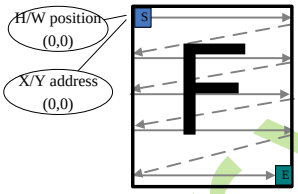
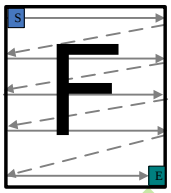
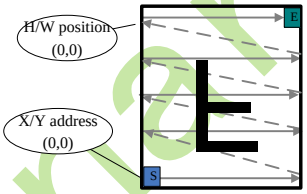
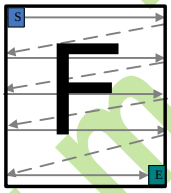
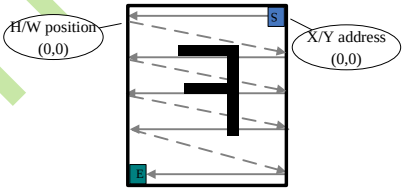
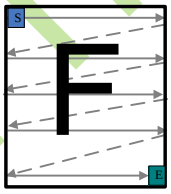
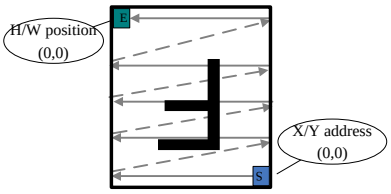
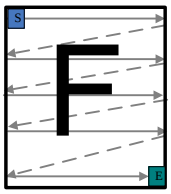
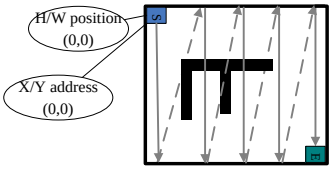
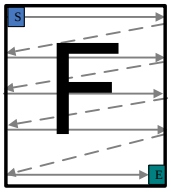
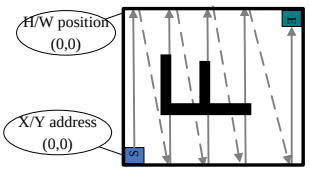
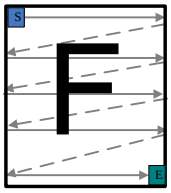
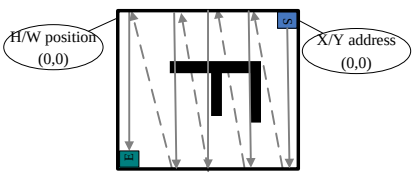
5.2.1. 132RGBx132 (GM == '01')

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (131 - Physical Page Pointer)
0	1	0	Direct to (131 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (131 - Physical Column Pointer)	Direct to (131 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (131 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (131 - Physical Column Pointer)
1	1	1	Direct to (131 - Physical Page Pointer)	Direct to (131 - Physical Column Pointer)

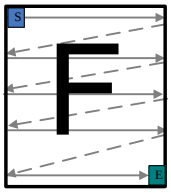
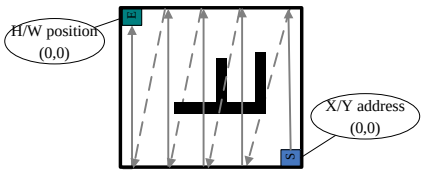
Preliminary

5.2.2. Frame Data Write Direction

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-ivert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-invert	1	0	1		
X-Y exchange X-invert	1	1	0		

Preliminary

X-Y exchange Y-invert X-invert	1	1	1		

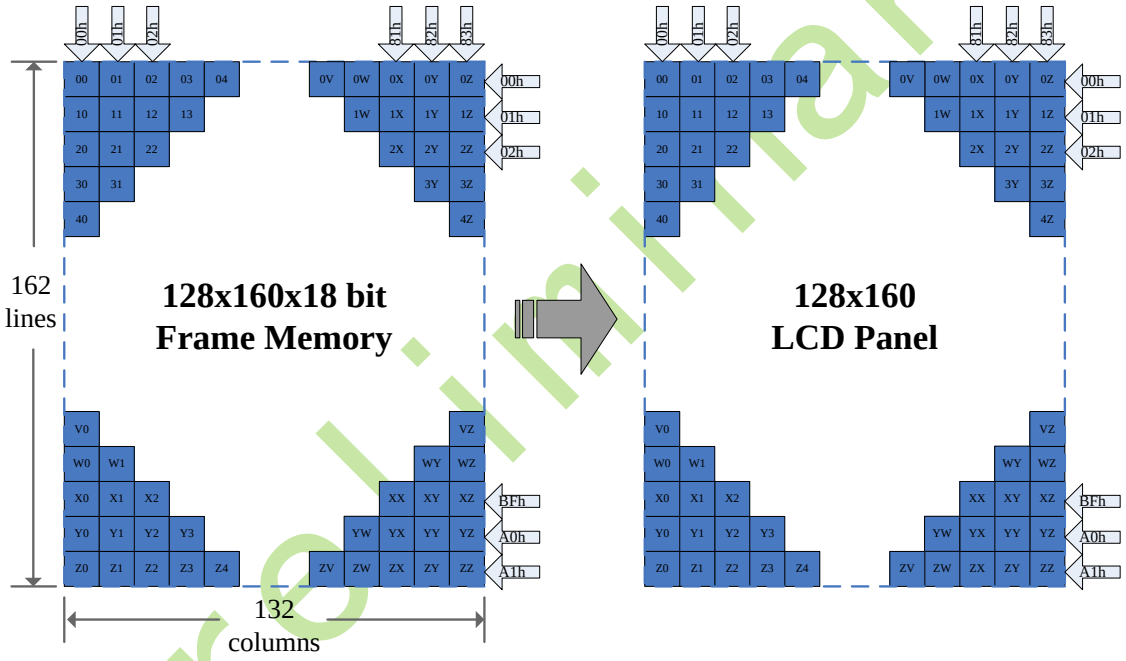
Preliminary

5.3. GRAM to display address mapping

GC9106 supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

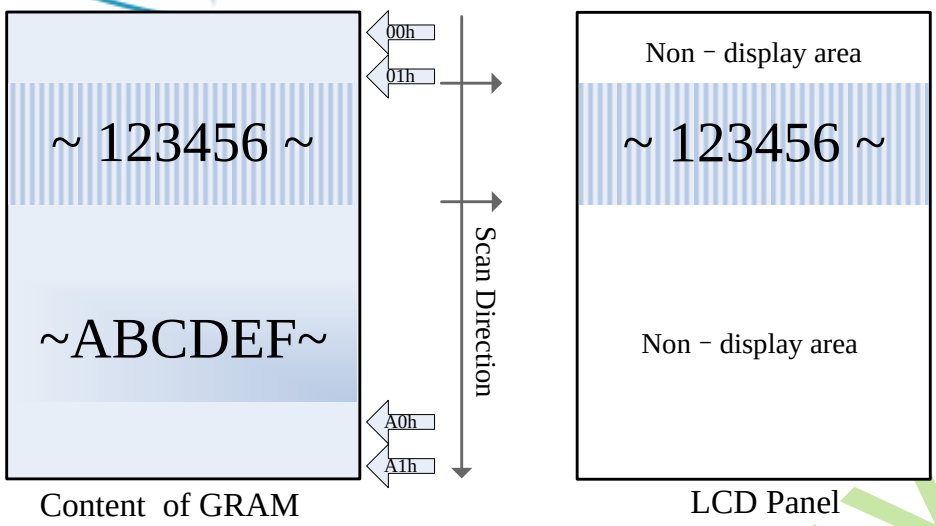
5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 007fh and page pointer is 0000h to 009fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



Example1:
(1) Partial mode on (setting 12h)
(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘0’**.

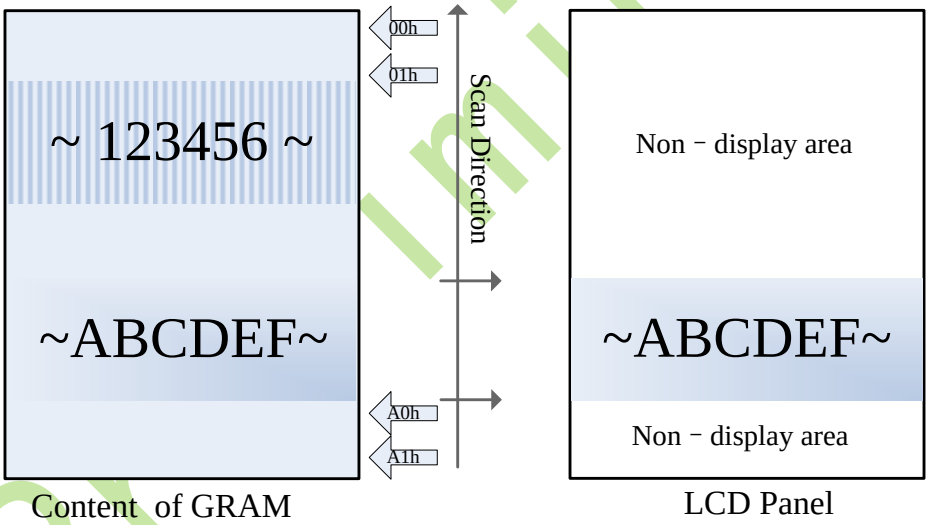
Preliminary



Example2:

(1) Partial mode on (setting 12h)

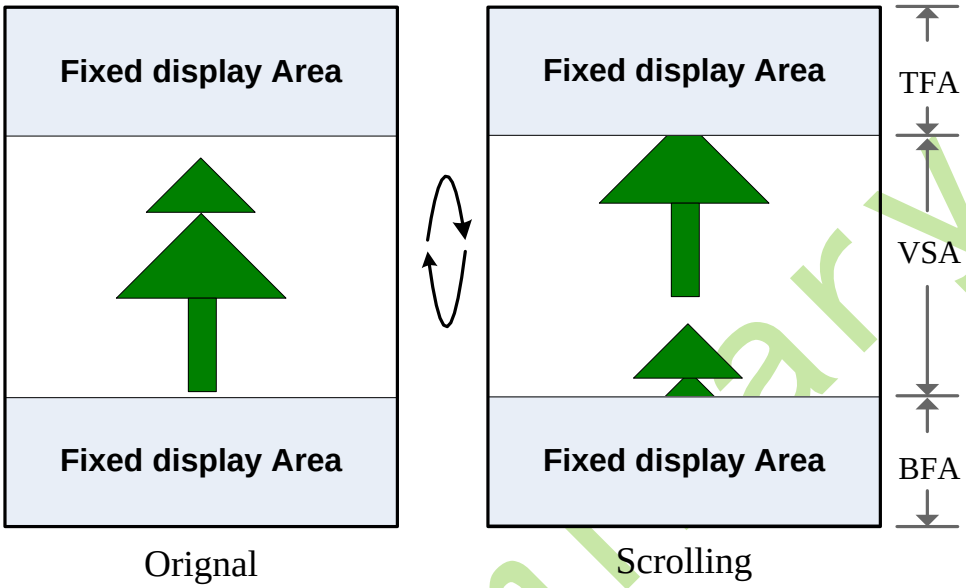
(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘1’**.



Preliminary

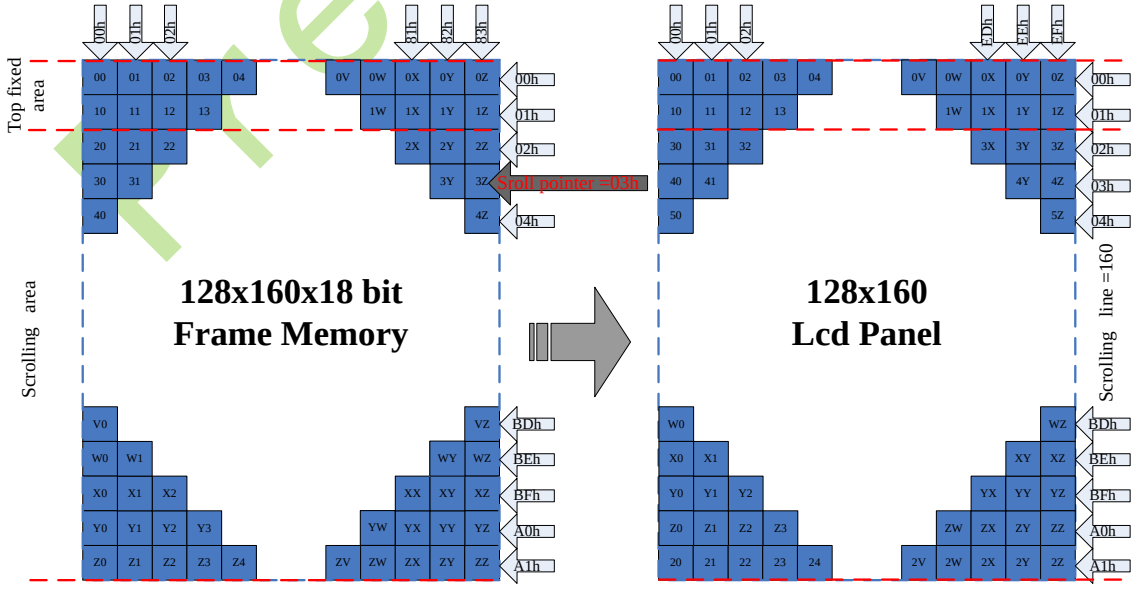
5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).



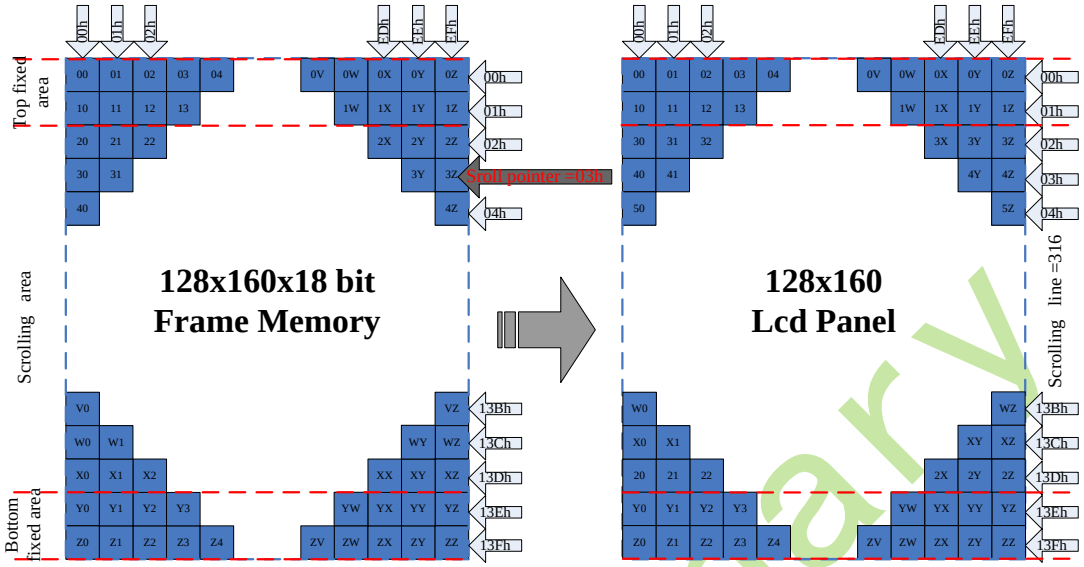
When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =160. In this case, scrolling is applied as shown below.

Example 1 .TFA=’2d’, VSA=’160d’, BFA=’0d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 1:

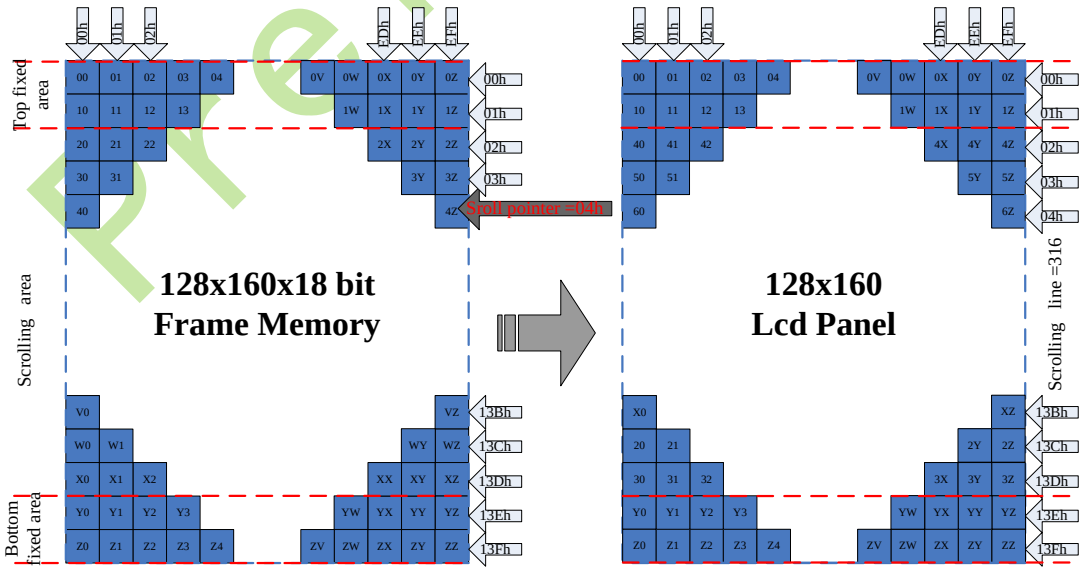


Preliminary

Example 2 .TFA=’2d’, VSA=’158d’, BFA=’2d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 2:



Example 3 .TFA=’2d’, VSA=’158d’, BFA=’2d’, VSP=’4d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 3:



Preliminary

Vertical scroll example

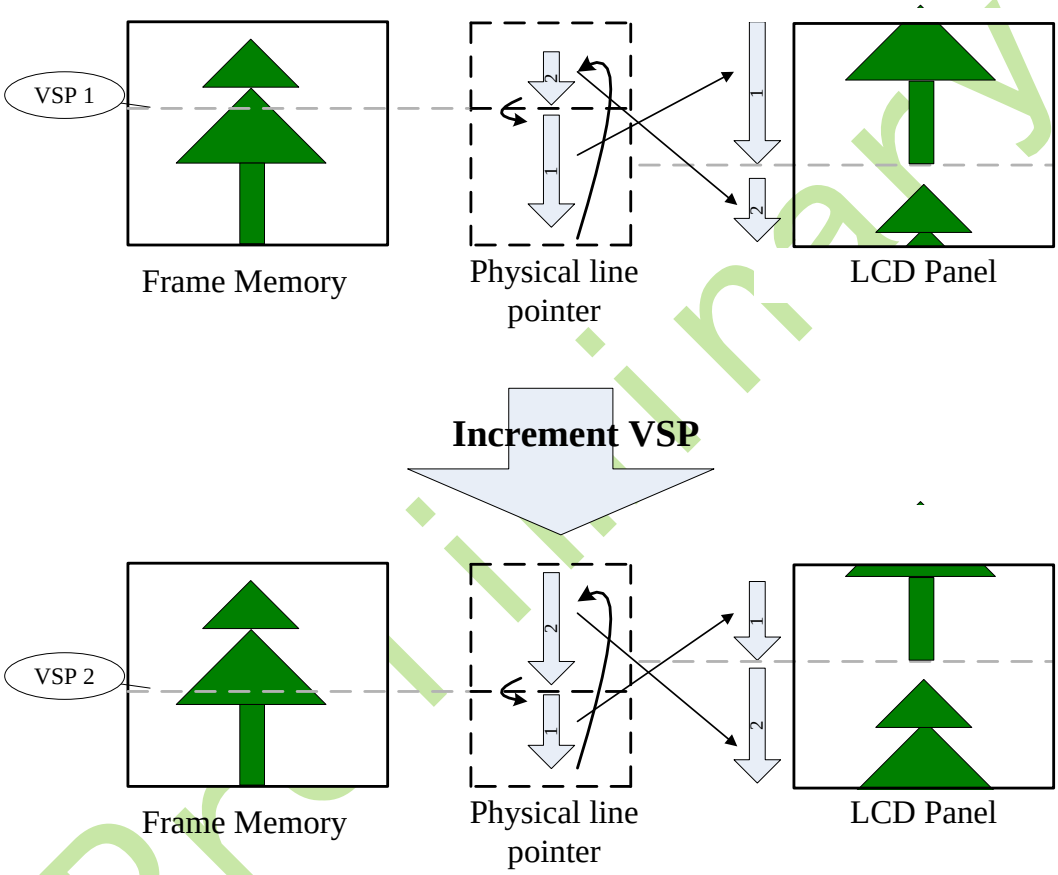
There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **VSP** bits

Case 1: TFA + VSA + BFA ≠ '160d'

N/A: Do not set TFA + VSA + BFA ≠ '160d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '160d' (Scrolling)

Example (1) When TFA='0d', VSA='160d', BFA='0d' and VSP1='40d' & VSP2='100d' (SS ='0', GS='0')



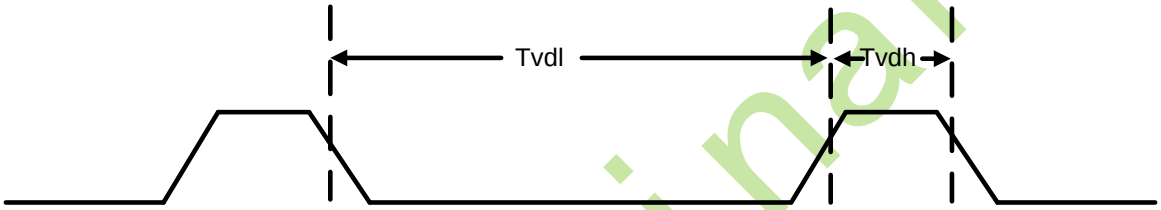
Preliminary

5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory writing when displaying video images.

5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:



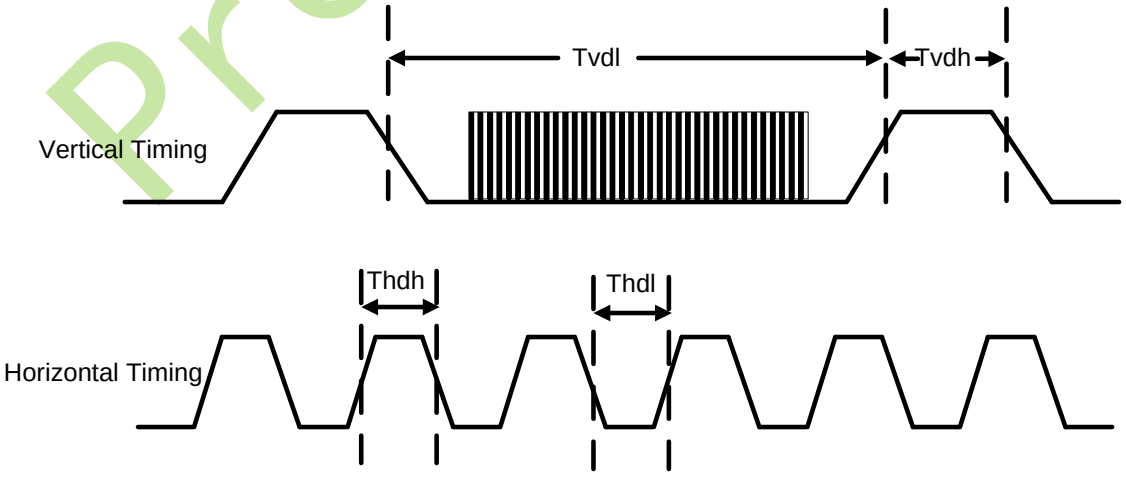
T_{line} is the display time of every line

T_{vdh}=(181-132)*T_{line} when GM[1:0]=01，**T_{vdh}**=(181-160)*T_{line} when GM[1:0]=11.

T_{vdl}=132*T_{line} when GM[1:0]=01，**T_{vdl}**=160*T_{line} when GM[1:0]=11.

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.



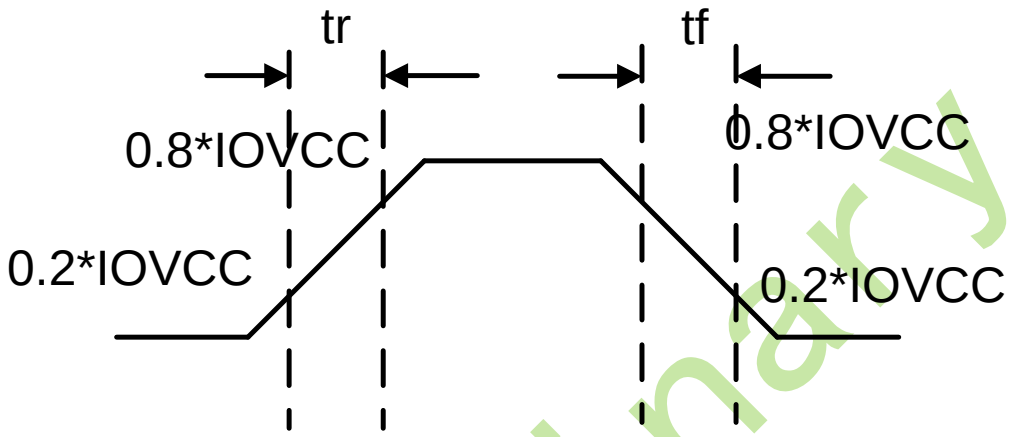
Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.	Description

Preliminary

		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9106 contains a 396 channels of source driver (S1~S396) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 396 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously.
Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

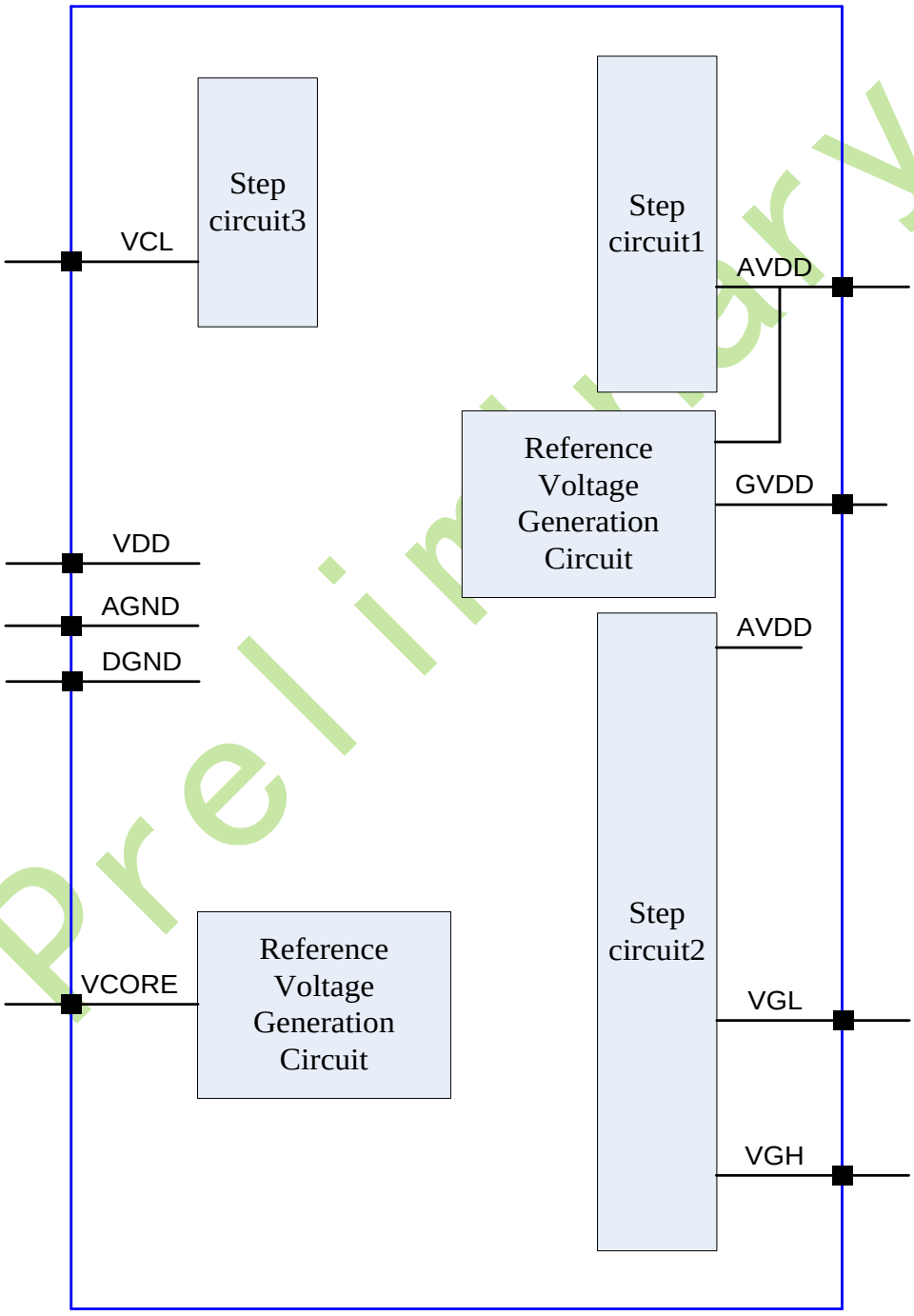
The GC9106 contains a 160 gate channels of gate driver (G1~G160) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

Preliminary

5.7. LCD power generation circuit

5.7.1. Power supply circuit

The power circuit of GC9106 is used to generate supply voltages for LCD panel driving.

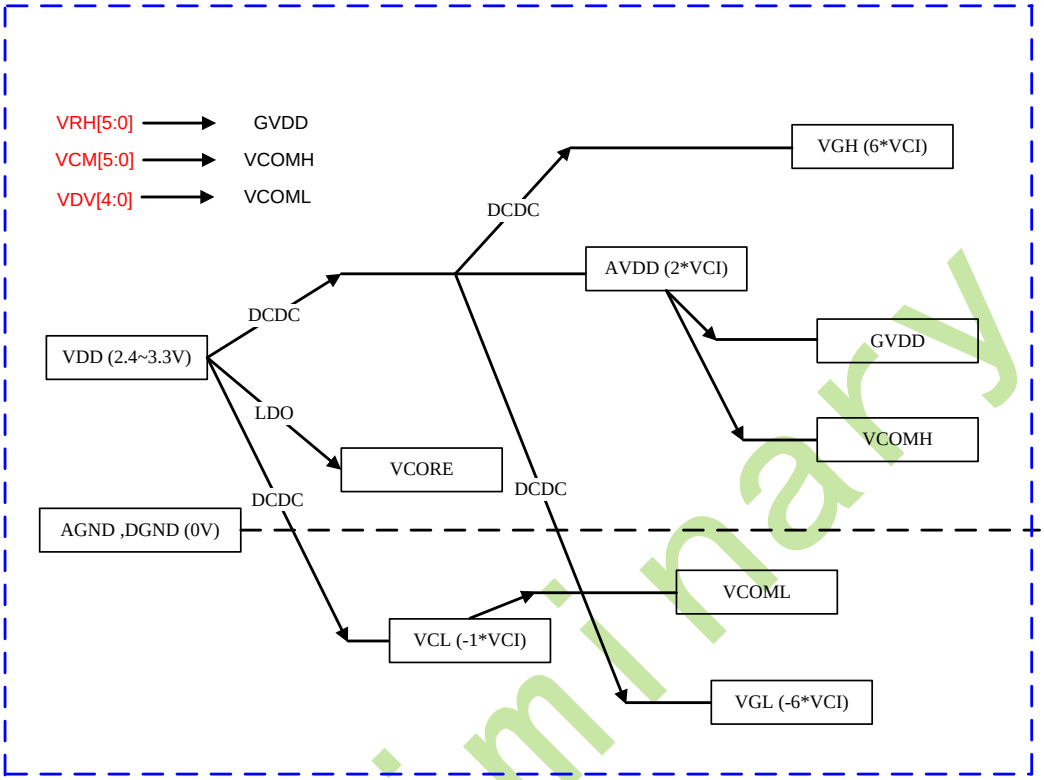


Block diagram of GC9106 power circuit

Preliminary

5.7.2. LCD power generation scheme

The boost voltage generated is shown as below.

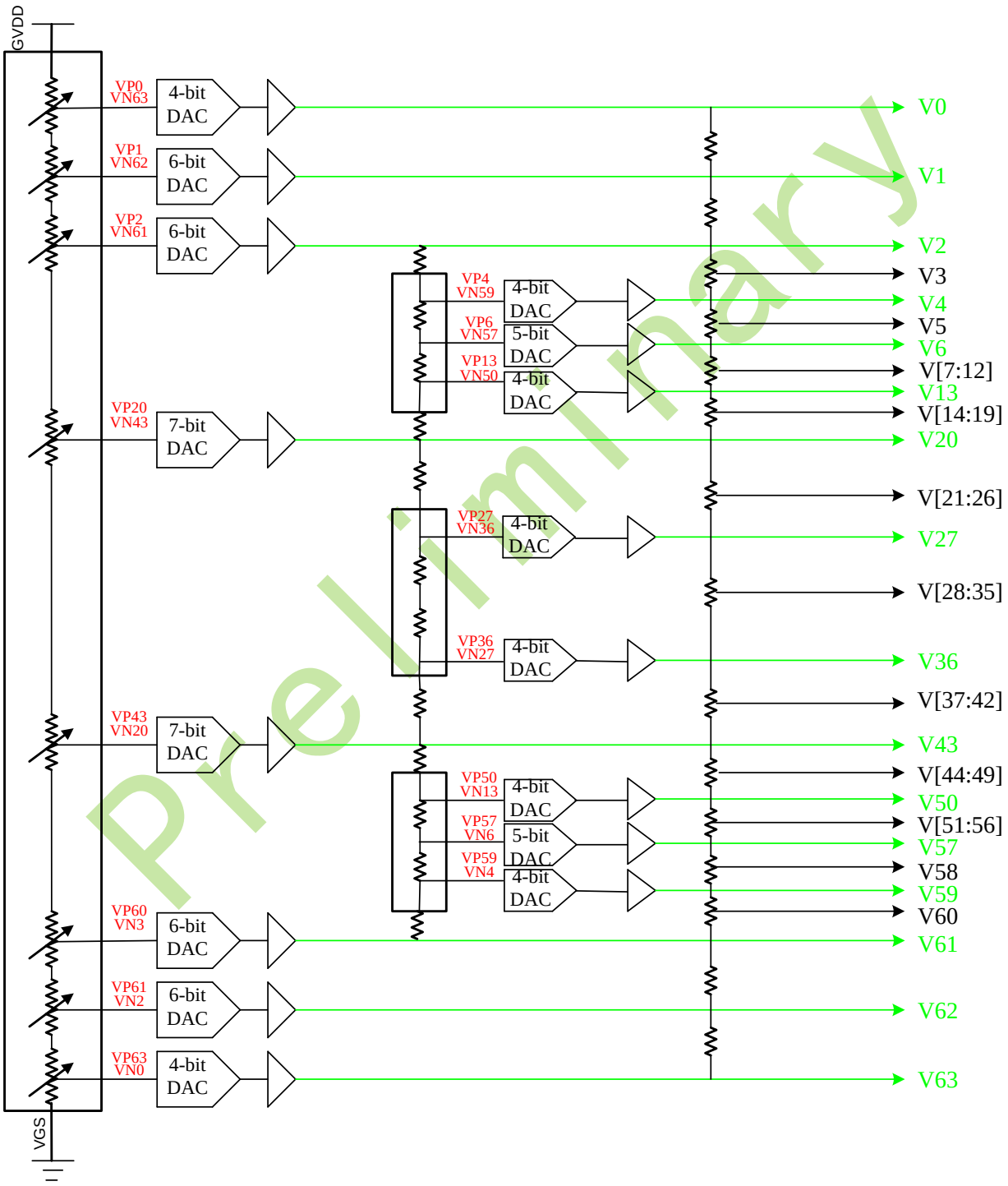


LCD power generation scheme

Preliminary

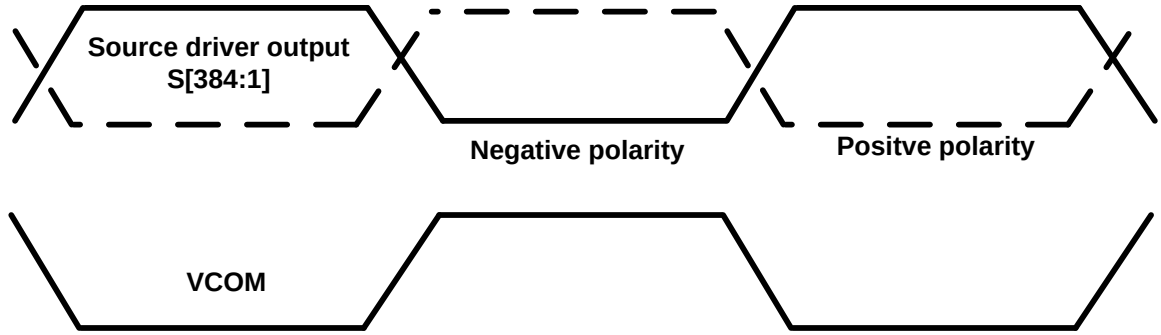
5.8. Gamma Correction

GC9106 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 32 registers determining 16 reference grayscale levels, whitch make GC9106 available with liquid crystal panels of various characteristics.

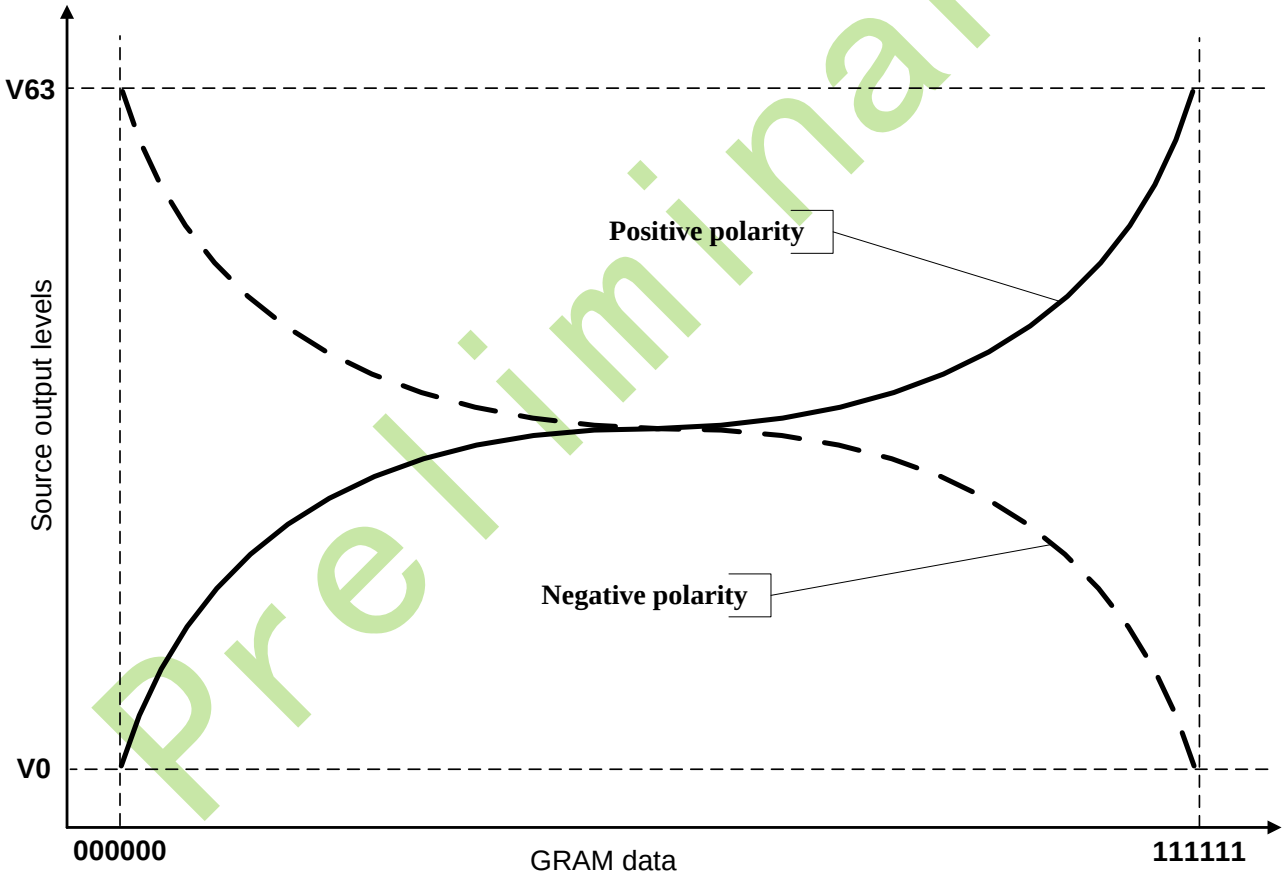


Grayscale Voltage Generation

Preliminary



Relationship between Source Output and VCOM



Preliminary

5.9. Power Level Definition

5.9.1. Power Levels

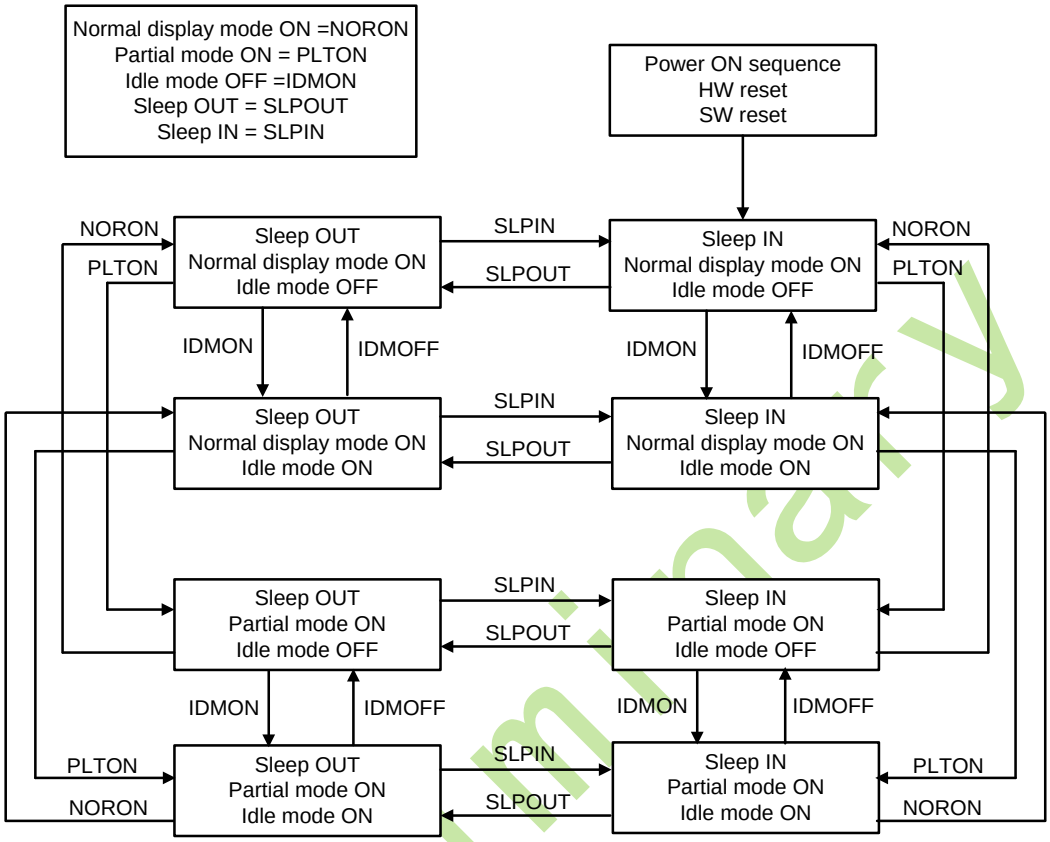
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDD and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

Preliminary

5.9.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

Preliminary

6. Command

6.1. Command List

USER REG

Regulative Command Set													
Command Function	**D/CX**	**RDX**	**WRX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Read Display Identification	0	1	↑	XX	0	0	0	0	0	0	0	0	00
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1_1[7:0]								00
	1	↑	1	XX	ID1_2[7:0]								91
	1	↑	1	XX	ID1_3[7:0]								04
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01
Read Manufactory Programming Identification	0	1	↑	XX	0	0	0	0	0	1	0	0	04
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Man_ID1_1[7:0]								00
	1	↑	1	XX	Man_ID1_2[7:0]								91
	1	↑	1	XX	Man_ID1_3[7:0]								06
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	BSTON	MY	MX	MV	ML	RGB	0	0	00
	1	↑	1	XX	0	IFPF[2:0]			IDMON	PTLON	SLPOUT	NORON	61
	1	↑	1	XX	0	0	INVON	0	0	DISON	TEON	0	00
	1	↑	1	XX	0	0	TEM	0	0	0	0	0	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0A
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	BSTON	IDMON	PTLON	SLPON	NORON	DISON	0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0B
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	MY	MX	MV	ML	RGB	0	0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0C
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	IFPF [2:0]			06

Preliminary

Read Display Image Form	0	1	↑	XX	0	0	0	0	1	1	0	1	0D
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	VSSON	0	INVON	0	0	0	0	0	00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0E
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	TEON	TEM	0	0	0	0	0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0F
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	1	1	1	1	0	0	0	0	F0
Sleep In	0	1	↑	XX	0	0	0	1	0	0	0	0	10
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2A
	1	1	↑	XX	SC[15:8]								-
	1	1	↑	XX	SC[7:0]								-
	1	1	↑	XX	EC[15:8]								-
	1	1	↑	XX	EC[7:0]								-
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2B
	1	1	↑	XX	SP[15:8]								-
	1	1	↑	XX	SP[7:0]								-
	1	1	↑	XX	EP[15:8]								-
	1	1	↑	XX	EP[7:0]								-
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2C
	1	1	↑	D[17:0]									-
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								00
	1	1	↑	XX	ER[7:0]								A0
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								00

Preliminary

	1	1	↑	XX	VSA[7:0]								A0
	1	1	↑	XX	BFA[15:8]								00
	1	1	↑	XX	BFA[7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35
	1	1	↑	XX	0	0	0	0	0	0	0	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36
	1	1	↑	XX	MY	MX	MV	ML	BGR	0	0	0	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3A
	1	1	↑	XX	0	0	0	0	0	IFPF[2:0]			06
TEST Scanline Set	0	1	↑	XX	0	1	0	0	0	1	0	0	44
	1	1	↑	XX	SCNL[7:0]								00
TEST Scanline Get	0	1	↑	XX	0	1	0	0	0	1	0	1	45
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	SCNL[7:0]								--
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4
	1	1	↑	XX	0	0	bgr_comp	0	0	inv_ctl[2:0]			20
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DA
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Man_ID1_1[7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DB
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Man_ID1_2[7:0]								91
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DC
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Man_ID1_3[7:0]								06
Majority en	0	1	↑	XX	1	1	1	1	1	1	0	1	FD
	1	1	↑	XX	maj_en[15:8]								00
	1	1	↑	XX	maj_en[7:0]								00

Preliminary

INTER REG

Internal Command Set													
Command Function	**D/CX**	**RDX**	**WRX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FE
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EF
AVDD_CLK	0	1	↑	XX	1	1	0	0	0	0	0	0	C0
	1	↑	1	XX	1	1	0	AVDD_CLKAD[1:0]		0	1	1	CB
AVEE_CLK	0	1	↑	XX	1	1	0	0	0	0	0	1	C1
	1	↑	1	XX	1	1	0	AVEE_CLKAD[1:0]		0	1	1	CB
VGH_CLK	0	1	↑	XX	1	1	0	0	0	0	1	0	C2
	1	↑	1	XX	0	1	0	0	VGH_CLKAD[3:0]				48
VGL_CLK	0	1	↑	XX	1	1	0	0	0	0	1	1	C3
	1	↑	1	XX	0	1	0	0	VGL_CLKAD[3:0]				48
CHP_SOU_CLK	0	1	↑	XX	1	1	0	0	0	1	1	0	C6
	1	↑	1	XX	0	0	0	1	1	CHP_SOU_CLKAD[2:0]			1A
	1	↑	1	XX	0	0	0	0	0	0	0	0	00
FRS	0	1	↑	XX	1	0	1	0	0	0	1	1	A3
	1	↑	1	XX	0	RTN[6:0]							16
SPI-2line	0	1	↑	XX	1	0	1	0	1	0	1	0	AA
	1	↑	1	XX	0	0	0	0	SPI2_EN	SPI_2DATA_MDT[2:0]			00
VREG1 CTL	0	1	↑	XX	1	1	1	0	0	1	1	0	E6
	1	↑	1	XX	0	VREG1A_AD[6:0]							50
	1	↑	1	XX	0	VREG1B_AD[6:0]							43
VREG2 CTL	0	1	↑	XX	1	1	1	0	0	1	1	1	E7
	1	↑	1	XX	0	VREG2A_AD[6:0]							38
	1	↑	1	XX	0	VREG2B_AD[6:0]							43
CHP CLAMP CTL1	0	1	↑	XX	1	1	1	0	1	0	1	0	EA
	1	↑	1	XX	0	VGH_AD[2:0]			0	VGL_AD[2:0]			24
	1	↑	1	XX	0	0	0	0	0	1	1	1	07
CHP CLAMP CTL2	0	1	↑	XX	1	1	1	0	1	0	1	1	EB
	1	↑	1	XX	0	AVEE_AD[2:0]			0	AVDD_AD[2:0]			33
	1	↑	1	XX	0	BVEE_AD[2:0]			0	BVDD_AD[2:0]			66

Preliminary

Command Function	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SET_GAMMA0	0	1	↑	1	1	1	1	0	0	0	0	F0
	1	1	↑	X	X	X	X	VP0[3:0]				0F
	1	1	↑	X	X	VP1[5:0]						3F
	1	1	↑	X	X	VP2[5:0]						3F
	1	1	↑	X	X	X	X	VP4[3:0]				0F
	1	1	↑	X	X	X	X	VP6[4:0]				1A
	1	1	↑	X				VP13[4:0]				0F
	1	1	↑	X	VP20[6:0]							5A
	1	1	↑	VP36[3:0]				VP27[3:0]				64
	1	1	↑	X	VP43[6:0]							30
	1	1	↑	X	X	X		VP50[3:0]				0A
	1	1	↑	X	X	X	VP57[4:0]					15
	1	1	↑	X	X	X	X	VP59[3:0]				05
	1	1	↑	X	X	VP61[5:0]						19
	1	1	↑	X	X	VP62[5:0]						19
	1	1	↑	X	X	X	X	VP63[3:0]				02
SET_GAMMA1	0	1	↑	1	1	1	1	0	0	0	0	F1
	1	1	↑	X	X	X	X	VN0[3:0]				0F
	1	1	↑	X	X	VN1[5:0]						3F
	1	1	↑	X	X	VN2[5:0]						2F
	1	1	↑	X	X	X	X	VN4[3:0]				0F
	1	1	↑	X	X	X	X	VN6[4:0]				15
	1	1	↑	X				VN13[4:0]				0B
	1	1	↑	X	VN20[6:0]							30
	1	1	↑	VN36[3:0]				VN27[3:0]				87
	1	1	↑	X	VN43[6:0]							2F
	1	1	↑	X	X	X		VN50[3:0]				0A
	1	1	↑	X	X	X	VN57[4:0]					15
	1	1	↑	X	X	X	X	VN59[3:0]				0F
	1	1	↑	X	X	VN61[5:0]						1E
	1	1	↑	X	X	VN62[5:0]						18
	1	1	↑	X	X	X	X	VN63[3:0]				02

Preliminary

6.2. Description of User Command

6.2.1. Read Display Identification (00h)

<table>
<tr><td>00h</td><td colspan="13">Read display identification information 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_2[7:0]</td><td>91</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_3[7:0]</td><td>04</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID1_1 [7:0]): module/driver ID.
The 3rd parameter (ID1_2 [7:0]): LCD module/driver ID.
The 4th parameter (ID1_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13">The value of 00h is not changed by OTP writing.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009104h</td></tr><tr><td>SW Reset</td><td>24’h009104h</td></tr><tr><td>HW Reset</td><td>24’h009104h</td></tr></table></td></tr>
</table>

Preliminary

6.2.2. Software Reset (01h)

01h	Software Reset												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01
Parameter	No Parameter												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	No Parameter
SW Reset	No Parameter
HW Reset	No Parameter

Preliminary

6.2.3. Read display identification information 2 (04h)

04h	Read display identification information 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	Man_ID1_1 [7:0]								00
3rd Parameter	1	↑	1	XX	Man_ID1_2 [7:0]								91
4th Parameter	1	↑	1	XX	Man_ID1_3[7:0]								06
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (Man_ID1_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (Man_ID1_2 [7:0]): LCD module's manufacturer ID. The 4th parameter (Man_ID1_3 [7:0]): LCD module's manufacturer ID.												
Restriction	The value of 04h *is changed* by OTP writing if OTP enable. When the OTP disable, the value of 04h is 0x009106. When the OTP enable, the value of 04h is the same as the OTP writing.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes												
Default	Status / Default Value Power On Sequence / 24'h009106 SW Reset / 24'h009106 HW Reset / 24'h009106												

Preliminary

6.2.4. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	BSTON	MY	MX	MV	ML	RGB	0	0	00
3rd Parameter	1	↑	1	XX	0	IFPF[2:0]			IDMON	PTLON	SLPOUT	NORON	61
4th Parameter	1	↑	1	XX	0	0	INVON	0	0	DISON	TEON	0	00
5th Parameter	1	↑	1	XX	0	0	TEM	0	0	0	0	0	00

Preliminary

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
BSTON	Booster voltage status	0	Booster OFF
		1	Booster ON
MY	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
MX	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
MV	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
ML	Vertical refresh	0	LCD Refresh Top to bottom (When MADCTL B4='0')
		1	LCD Refresh bottom to Top (When MADCTL B4='1').
RGB	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
IFPF	Interface color pixel format definition	011	12-bit/pixel
		101	16-bit/pixel
		110	18-bit/pixel
IDMON	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
PTLON	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON
SLPOUT	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode
NORON	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
INVON	Inversion status	0	Inversion off
		1	Inversion on
DISON	Display ON/OFF	0	Display is OFF
		1	Display is ON
TEON	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
TEM	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking

- = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

Default

Status	Default Value
Power On Sequence	24'h006100
SW Reset	24'h006100
HW Reset	24'h006100

Preliminary

6.2.5. Read Display Power Mode (0Ah)

<table>
<tr><td>0Ah</td><td colspan="13">Read Display Power Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>BSTON</td><td>IDMON</td><td>PTLON</td><td>SLPON</td><td>NORON</td><td>DISON</td><td>0</td><td>0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>alue</th></tr>
<tr><td rowspan="2">BSTON</td><td>Booster Off or has a fault.</td><td>0</td></tr>
<tr><td>Booster On and working OK.</td><td>1</td></tr>
<tr><td rowspan="2">IDMON</td><td>Idle Mode Off.</td><td>0</td></tr>
<tr><td>Idle Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">PTLON</td><td>Partial Mode Off.</td><td>0</td></tr>
<tr><td>Partial Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">SLPON</td><td>Sleep In Mode</td><td>0</td></tr>
<tr><td>Sleep Out Mode</td><td>1</td></tr>
<tr><td rowspan="2">NORON</td><td>Display Normal Mode Off.</td><td>0</td></tr>
<tr><td>Display Normal Mode On</td><td>1</td></tr>
<tr><td rowspan="2">DISON</td><td>Display is Off.</td><td>0</td></tr>
<tr><td>Display is On</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>SW Reset</td><td>8’h08</td></tr>
<tr><td>HW Reset</td><td>8’h08</td></tr>
</table></td></tr>
</table>

Preliminary

6.2.6. Read Display MADCTL (0Bh)

<table>
<tr><td>0Bh</td><td colspan="13">Read Display MADCTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>RGB</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">MY</td><td>Top to ttom (When MADCTL B7=’0’).</td><td>0</td></tr>
<tr><td>Bottom to Top(When MADCTL B7=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">MX</td><td>Left to Right (When MADCTL B6=’0’)</td><td>0</td></tr>
<tr><td>Right to Left (When MADCTL B6=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">MV</td><td>Normal Mode (When MADCTL B5=’0’)</td><td>0</td></tr>
<tr><td>Reverse Mode (When MADCTL B5=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">ML</td><td>LCD Refresh Top to Bottom (When MADCTL B4=’0’)</td><td>0</td></tr>
<tr><td>LCD Refresh Bottom to Top (When MADCTL B4=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">RGB</td><td>RGB (When MADCTL B3=’0’)</td><td>0</td></tr>
<tr><td>BGR (When MADCTL B3=’1’).</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Preliminary

6.2.7. Read Display Pixel Format (0Ch)

<table>
<tr><td>0Ch</td><td colspan="13">Read Display Pixel Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>06</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>IFPF [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>010</td><td>12 bits / pixle</td></tr>
<tr><td>101</td><td>16 bits / pixel</td></tr>
<tr><td>110</td><td>18 bits / pixel</td></tr>
<tr><td>others</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>IFPF [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Chang</td></tr>
<tr><td>HW Reset</td><td>3’b110</td></tr>
</table></td></tr>
</table>

Preliminary

6.2.8. Read Display Image Format (0Dh)

<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0D</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>VSSON</td><td>0</td><td>INVON</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">VSSON</td><td>Vertical mode off</td><td>0</td></tr>
<tr><td>Vertical mode on</td><td>1</td></tr>
<tr><td rowspan="3">INVON</td><td>Inversion off</td><td>0</td></tr>
<tr><td>Inversion on</td><td>1</td></tr>
<tr><td>other</td><td>Not define</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’b00</td></tr>
<tr><td>SW Reset</td><td>8’b00</td></tr>
<tr><td>HW Reset</td><td>8’b00</td></tr>
</table></td></tr>
</table>

Preliminary

6.2.9. Read Display Signal Mode (0Eh)

<table>
<tr><td>0Eh</td><td colspan="13">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>TEON</td><td>TEM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">TEON</td><td>0</td><td>Tearing effect line OFF</td></tr>
<tr><td>1</td><td>Tearing effect line ON</td></tr>
<tr><td rowspan="2">TEM</td><td>0</td><td>Tearing effect line mode 1</td></tr>
<tr><td>1</td><td>Tearing effect line mode 2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Preliminary

6.2.10. Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><td>0Fh</td><td colspan="13">Read Display Self-Diagnostic Result</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F</td><td>1</td><td>0F</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0</td></tr>
<tr><td>Description</td><td colspan="13">In sleep-in state, the value of 0fh is 0xF0. In sleep out state, the value of 0fh is 0xF0 or 0x00 alternately.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’hF0</td></tr><tr><td>SW Reset</td><td>8’hF0</td></tr><tr><td>HW Reset</td><td>8’hF0</td></tr></table></td></tr>
</table>

Preliminary

6.2.11. Sleep In (10h)

10h	Enter Sleep Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped MCU interface and memory are still working and the memory keeps its contents.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

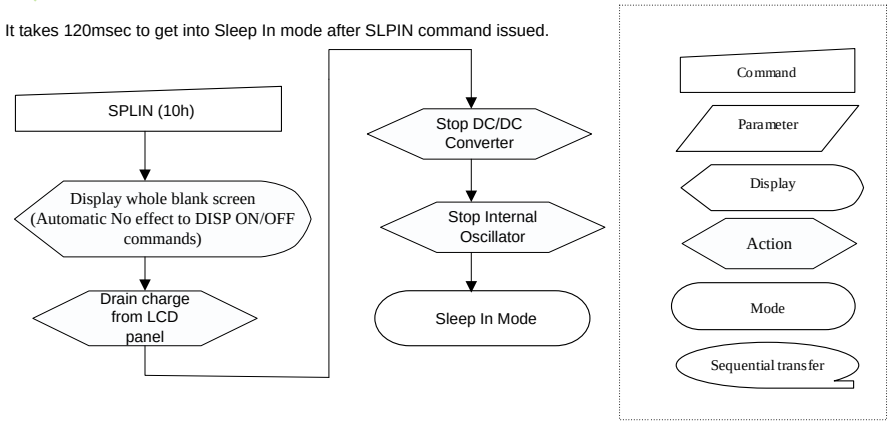
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart



Preliminary

6.2.12. Sleep Out (11h)

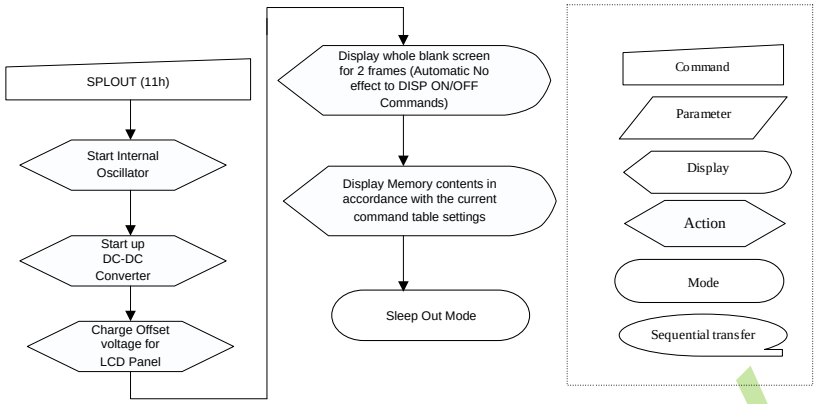
11h	Sleep Out Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	This command turns off sleep mode. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Preliminary

Flow Chart	

Preliminary

6.2.13. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

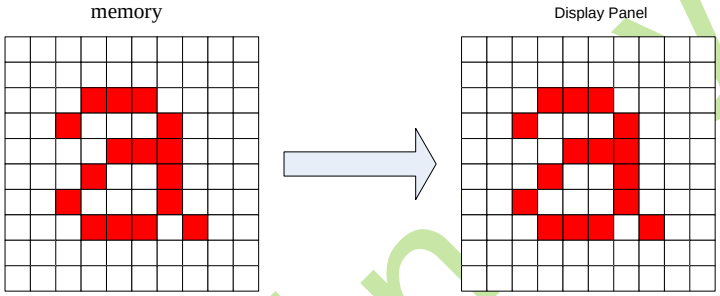
Preliminary

6.2.14. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

Preliminary

6.2.15. Display Inversion OFF (20h)

20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. 												
Restriction	This command has no effect when module already is inversion OFF mode.												

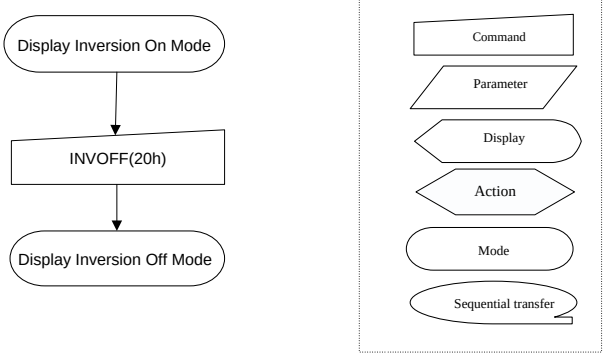
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

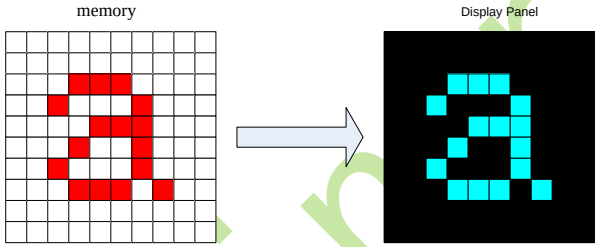
Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



Preliminary

6.2.16. Display Inversion ON (21h)

21h	Display Inversion ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.. 												
Restriction	This command has no effect when module already is inversion ON mode.												

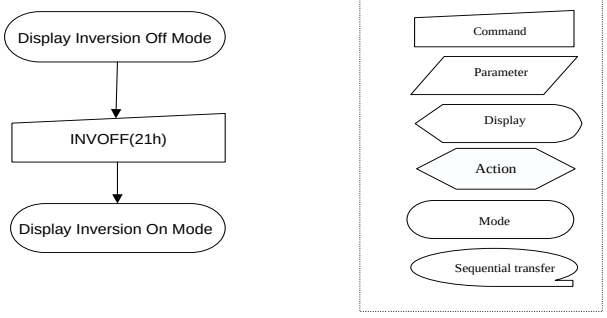
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

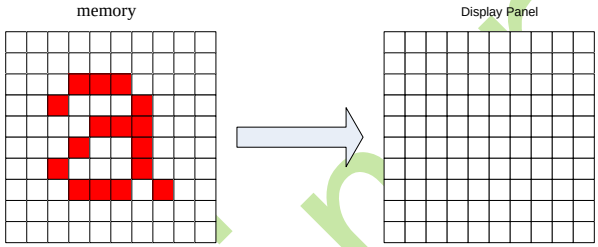
Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



Preliminary

6.2.17. Display OFF (28h)

28h	Display OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. 												
Restriction	This command has no effect when module is already in display off mode.												

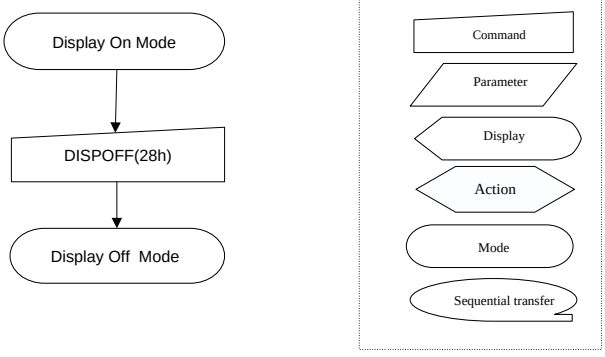
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

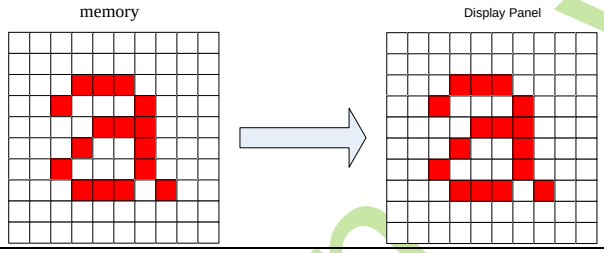
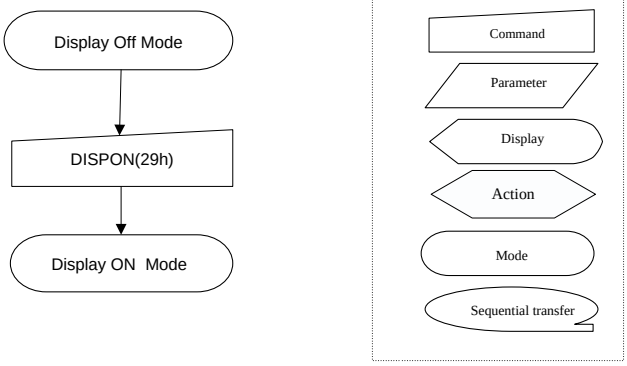
Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



Preliminary

6.2.18. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

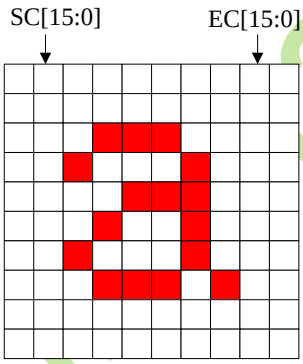
Preliminary

6.2.19. Column Address Set (2Ah)

2Ah	Column Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2A
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	--
2nd Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	--
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	--
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	--

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

SC [15:0] always must be equal to or less than EC [15:0].

When SC [15:0] or EC [15:0] is greater than maximum address like below, data of out of range will be ignored

1. 132X132 memory base (GM = '01')

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 131 (0083h)): MV="0")

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 131 (0083h)): MV="1")

2. 128X160 memory base (GM = '11')

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 127 (007Fh)): MV="0")

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 159 (009Fh)): MV="1")

Register Availability

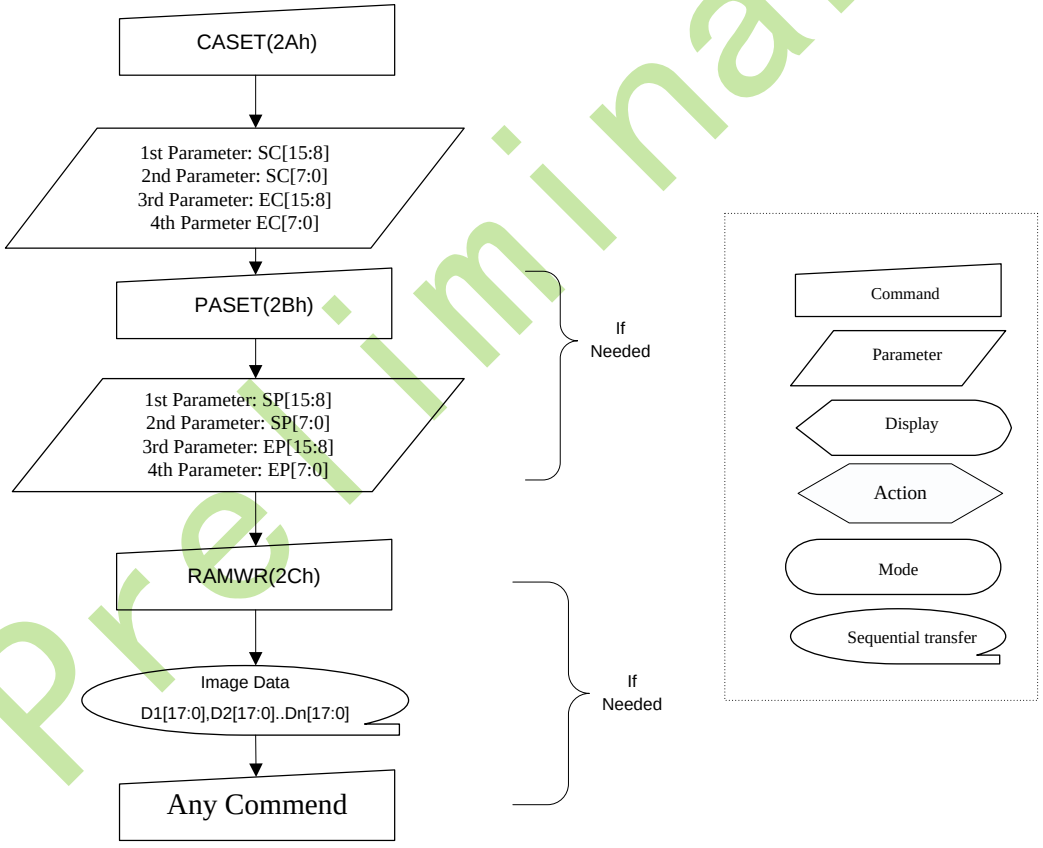
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sl p Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

Default

GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= '01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	SW Reset	0000h	0083h (131)	0083h (131)
	HW Reset	0000h	0083h (131)	
GM= '11' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)	
	SW Reset	0000h	007Fh (127)	009Fh (159)
	HW Reset	0000h	007Fh (127)	

Flow Chart



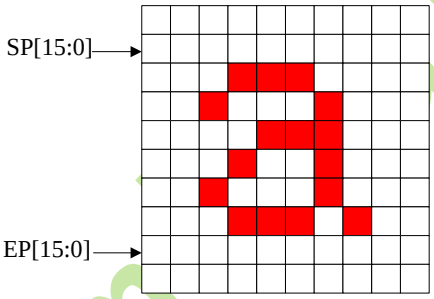
Preliminary

6.2.20. Row Address Set (2Bh)

2Bh	Row Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2B
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	--
2nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	--
3rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	--
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	--

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

SP [15:0] always must be equal to or less than EP [15:0].

When SP [15:0] or EP [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 132X132 memory base (GM = '01')

(Parameter range: 0 < SP [15:0] < EP [15:0] < 131 (00A1h)): MV="0"

(Parameter range: 0 < SP [15:0] < EP [15:0] < 131 (0083h)): MV="1"

2. 128X160 memory base (GM = '11')

(Parameter range: 0 < SP [15:0] < EP [15:0] < 159 (009Fh)): MV="0"

(Parameter range: 0 < SP [15:0] < EP [15:0] < 127 (007Fh)): MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

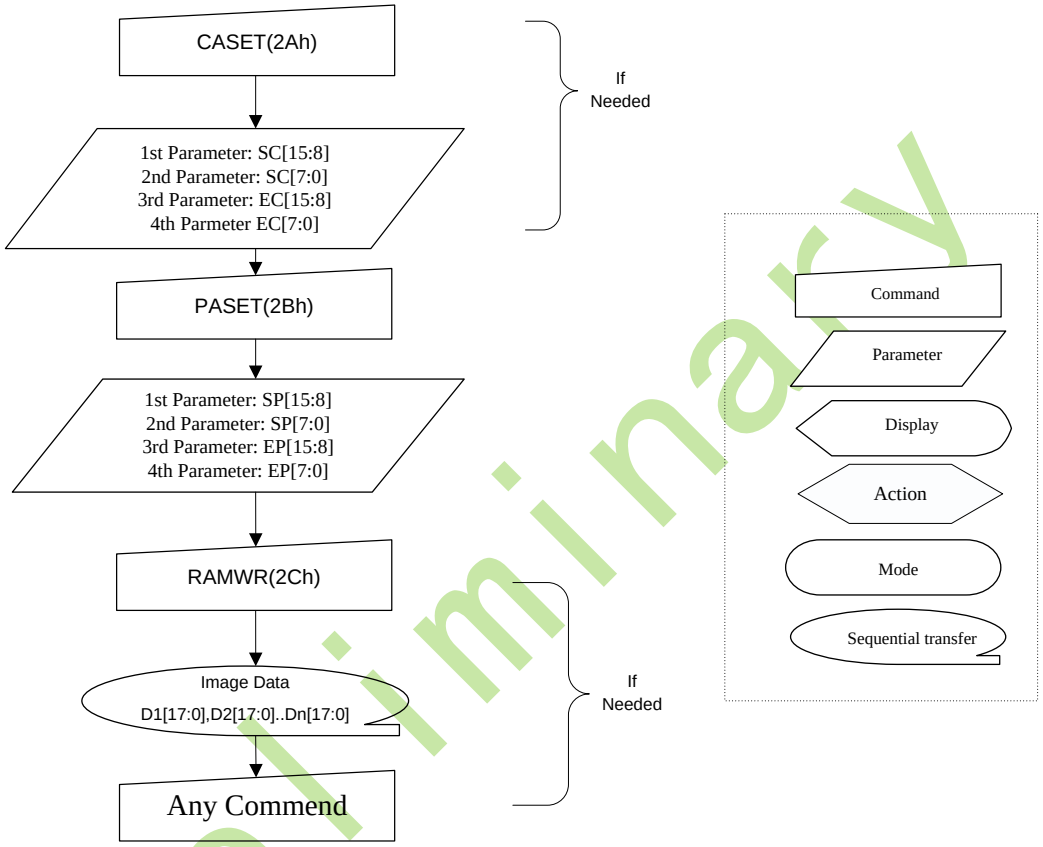
Default

GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= '01' (132x132	Power On Sequence	0000h	0083h (131)	
	SW Reset	0000h	0083h (131)	0083h (131)

Preliminary

Memory Base)	HW Reset	0000h	0083h (131)		
GM= ‘11’ (128x160 memory base)	Power On Sequence	0000h	009Fh (159)		
	SW Reset	0000h	009Fh (159)	007Fh (127)	
	HW Reset	0000h	009Fh (159)		

Flow Chart

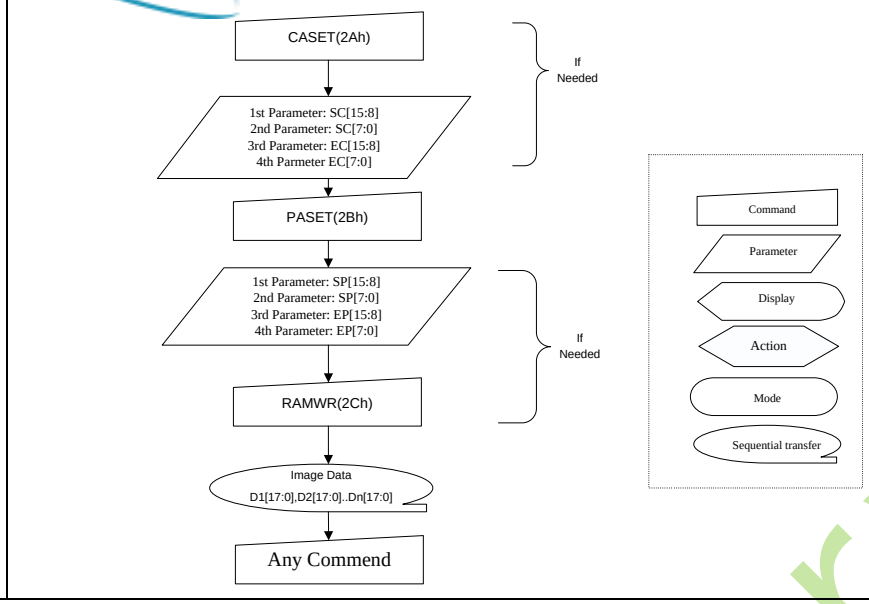


Preliminary

6.2.21. Memory Write (2Ch)

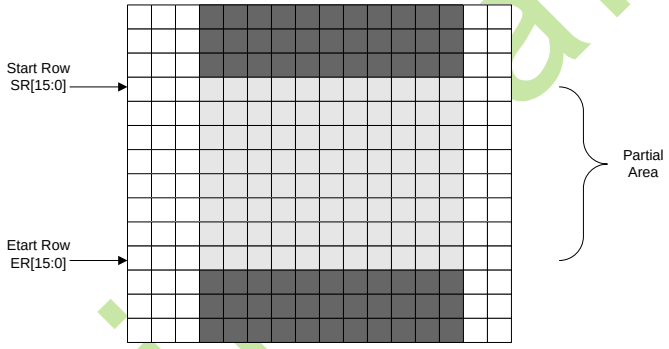
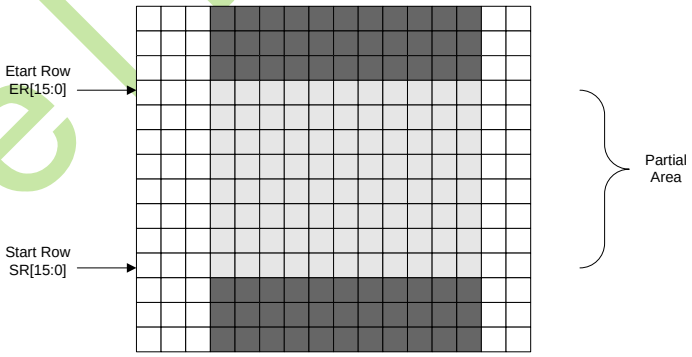
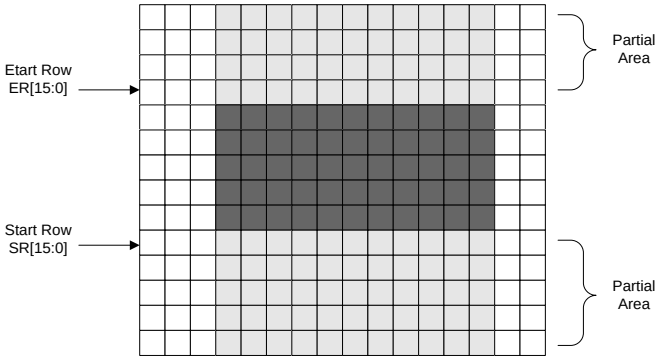
<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td rowspan="2"></td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Preliminary

Flow Chart	

Preliminary

6.2.22. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	-
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when ML=0:  If End Row>Start Row when ML=1:  If End Row<Start Row when ML =0:  												

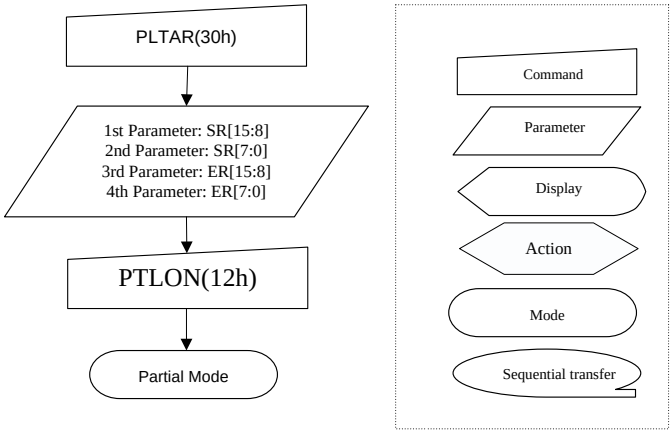
Preliminary

<table>
<tr><td></td><td>If End Row = Start Row then the Partial Area will be one row deep.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>SR [15:0]</th><th colspan="2">ER [15:0]</th></tr>
<tr><td>GM[1:0]</td><td>xx</td><td>GM = ‘01’</td><td>GM = ‘11’</td></tr>
<tr><td>Power On Sequence</td><td>16’h0000</td><td>16’h0083</td><td>16’h009F</td></tr>
<tr><td>SW Reset</td><td>16’h0000</td><td>16’h0083</td><td>16’h009F</td></tr>
<tr><td>HW Reset</td><td>16’h0000</td><td>16’h0083</td><td>16’h009F</td></tr>
</table>
</td></tr>
</table>

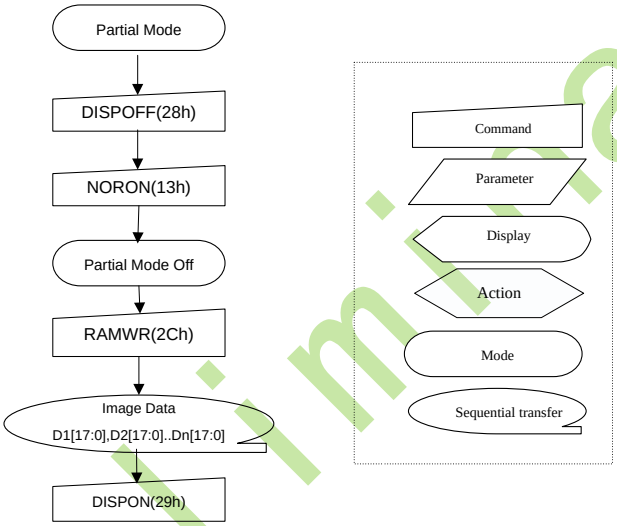
Preliminary

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



Preliminary

6.2.23. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								00
4th Parameter	1	1	↑	XX	VSA [7:0]								A0
5th Parameter	1	1	↑	XX	BFA [15:8]								00
6th Parameter	1	1	↑	XX	BFA [7:0]								00

Description

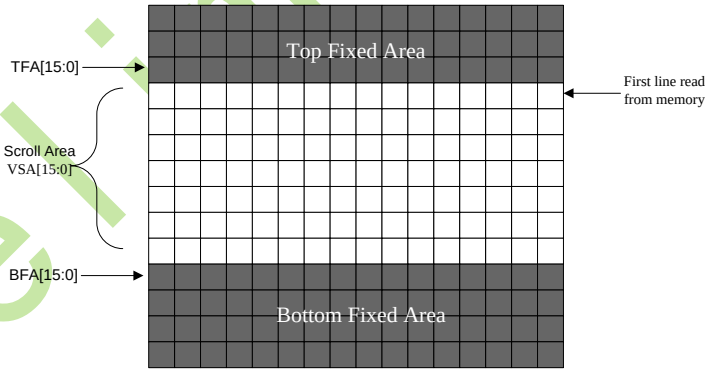
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



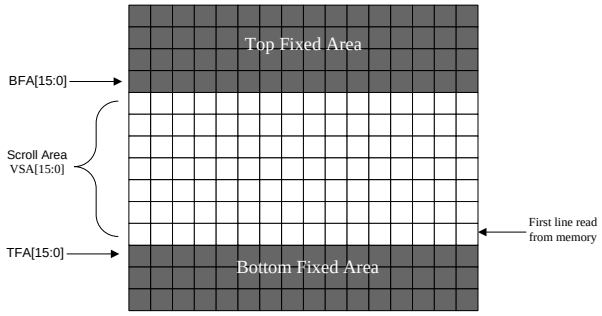
When MADCTL B4=1

The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).

Preliminary



X = Don't care.

Restriction

The condition is (TFA+VSA+BFA)=132 in 132RGBx132 (GM="01")

The condition is (TFA+VSA+BFA)=160 in 128RGBx160 (GM="11")

Otherwise Scrolling mode is undefined.

In Vertical Scroll Mode, MADCTR parameter MV should be set to '0', this only affects the Frame Memory Write.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

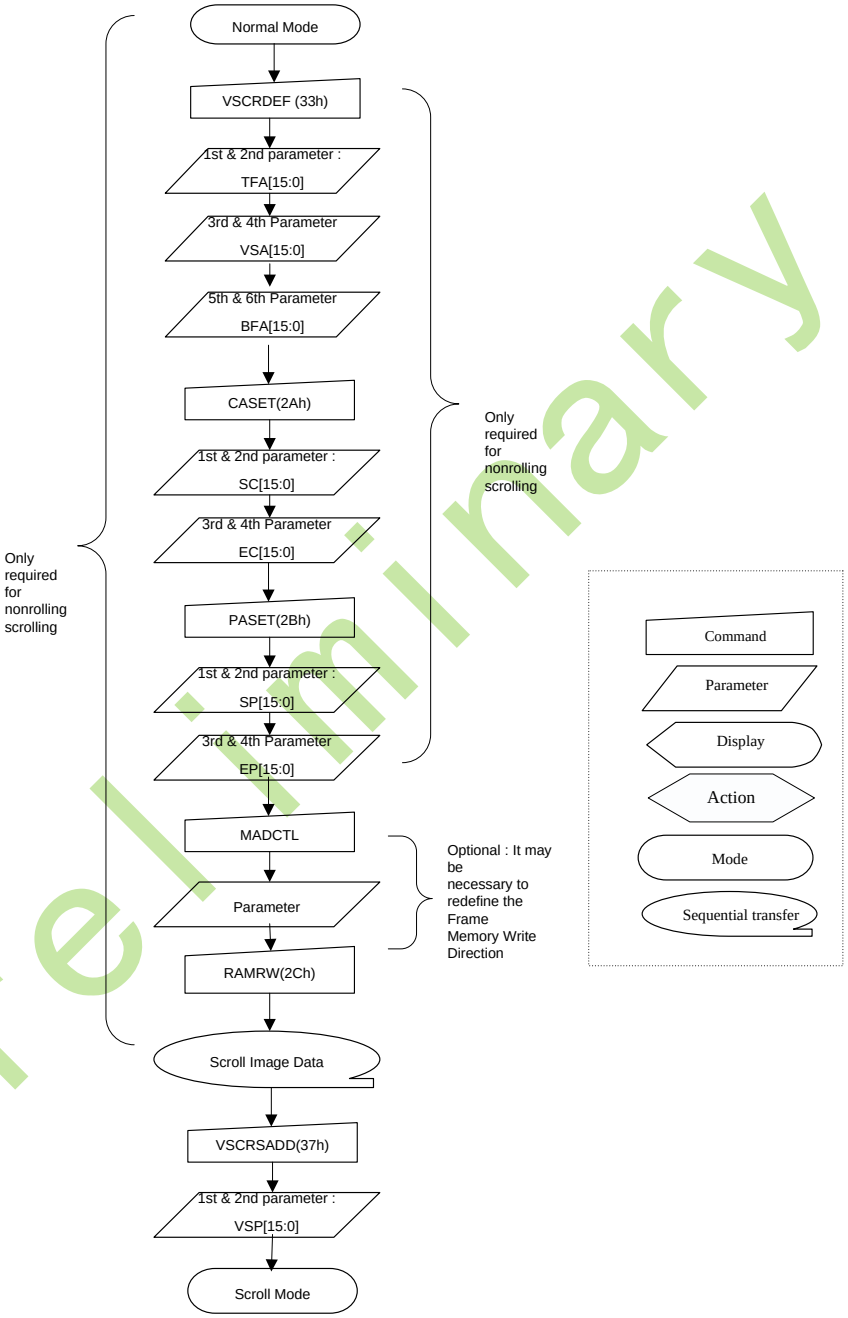
Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16'h0000	16'h00A0
SW Reset	16'h0000	16'h00A0
HW Reset	16'h0000	16'h00A0

Preliminary

Flow Chart

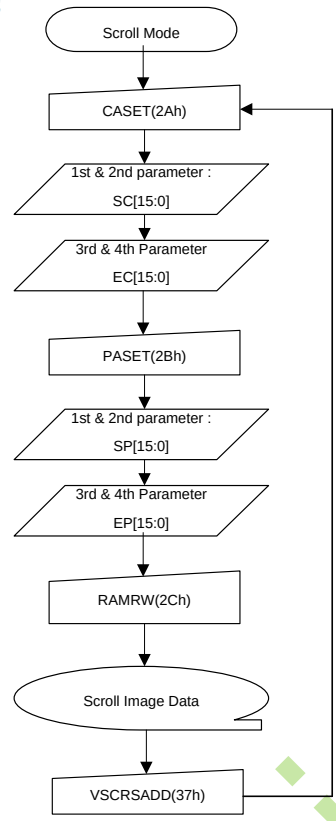
1. To enter Vertical Scroll Mode :

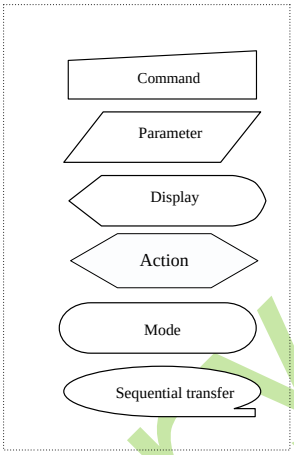


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

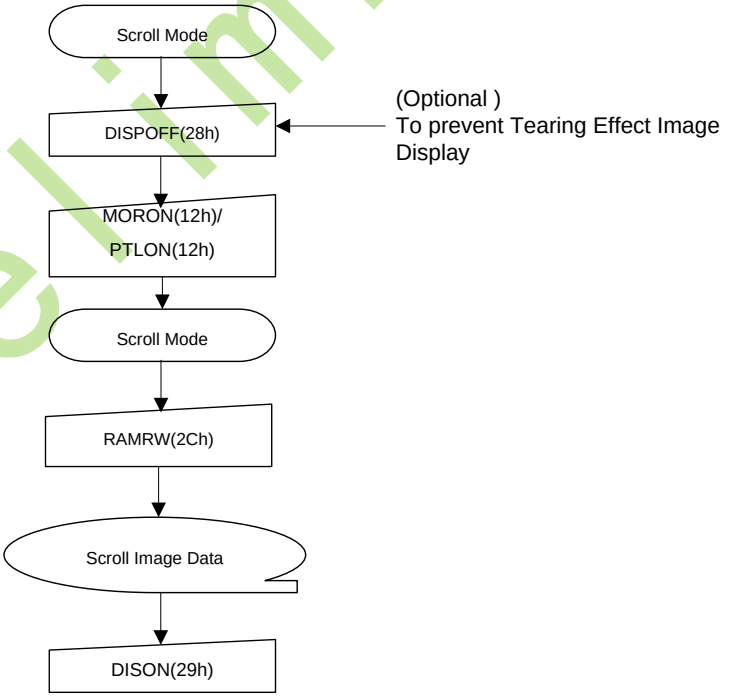
2.Continuous Scroll :

Preliminary





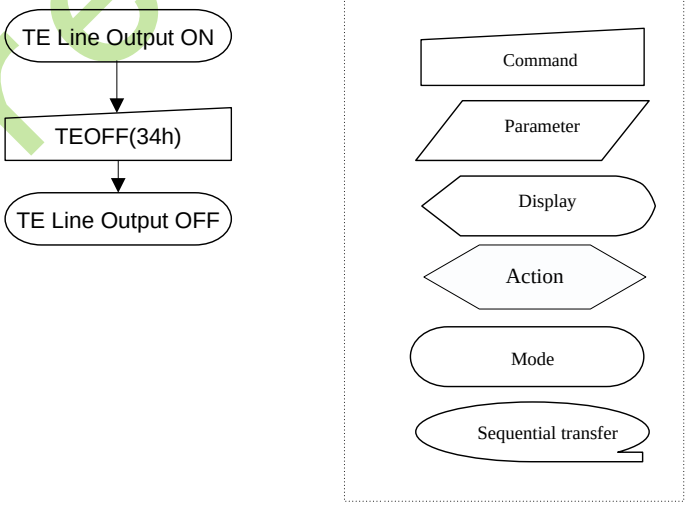
3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

Preliminary

6.2.24. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">
</td></tr>
</table>

Preliminary

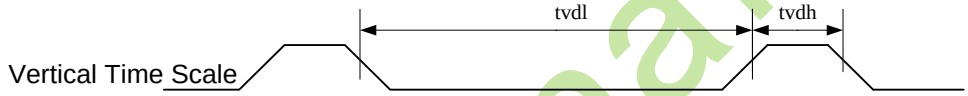
6.2.25. Tearing Effect Line ON (35h)

35h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00

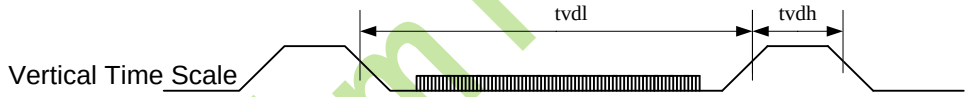
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:
The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don't care.

Restriction

This command has no effect when Tearing Effect output is already ON

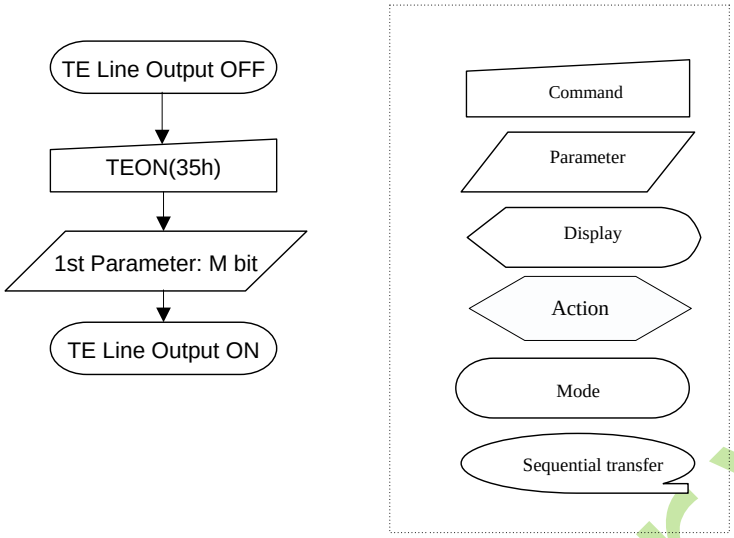
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Preliminary

Flow Chart	

Preliminary

6.2.26. Memory Access Ctrl (36h)

36h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

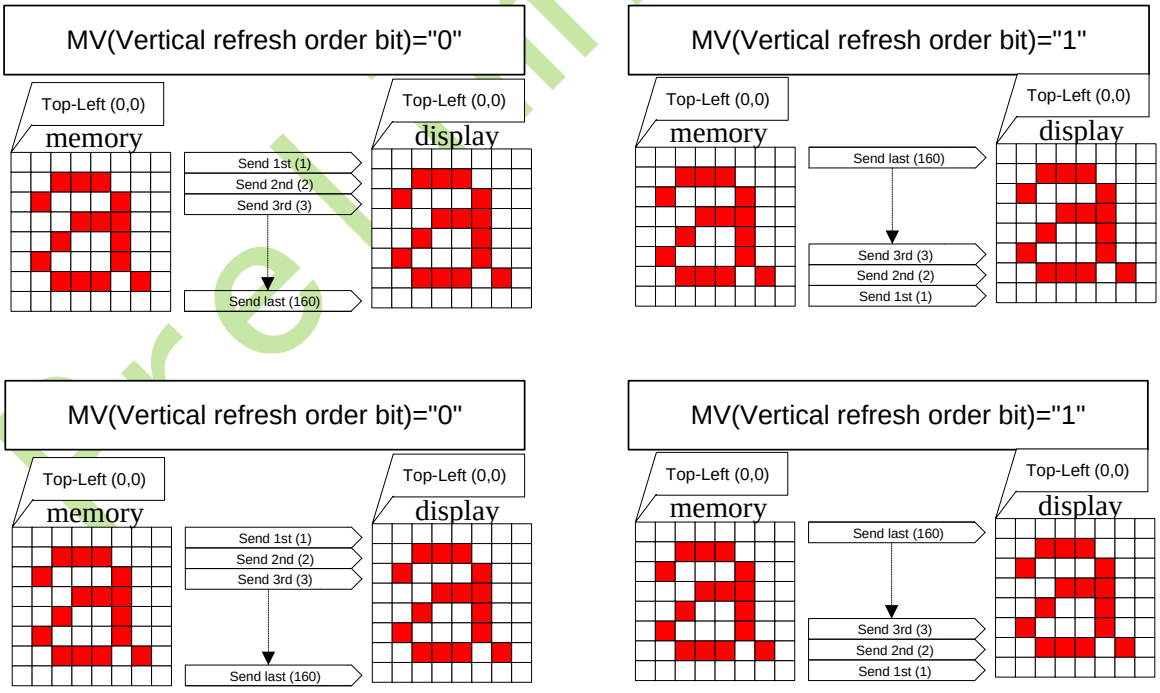
This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

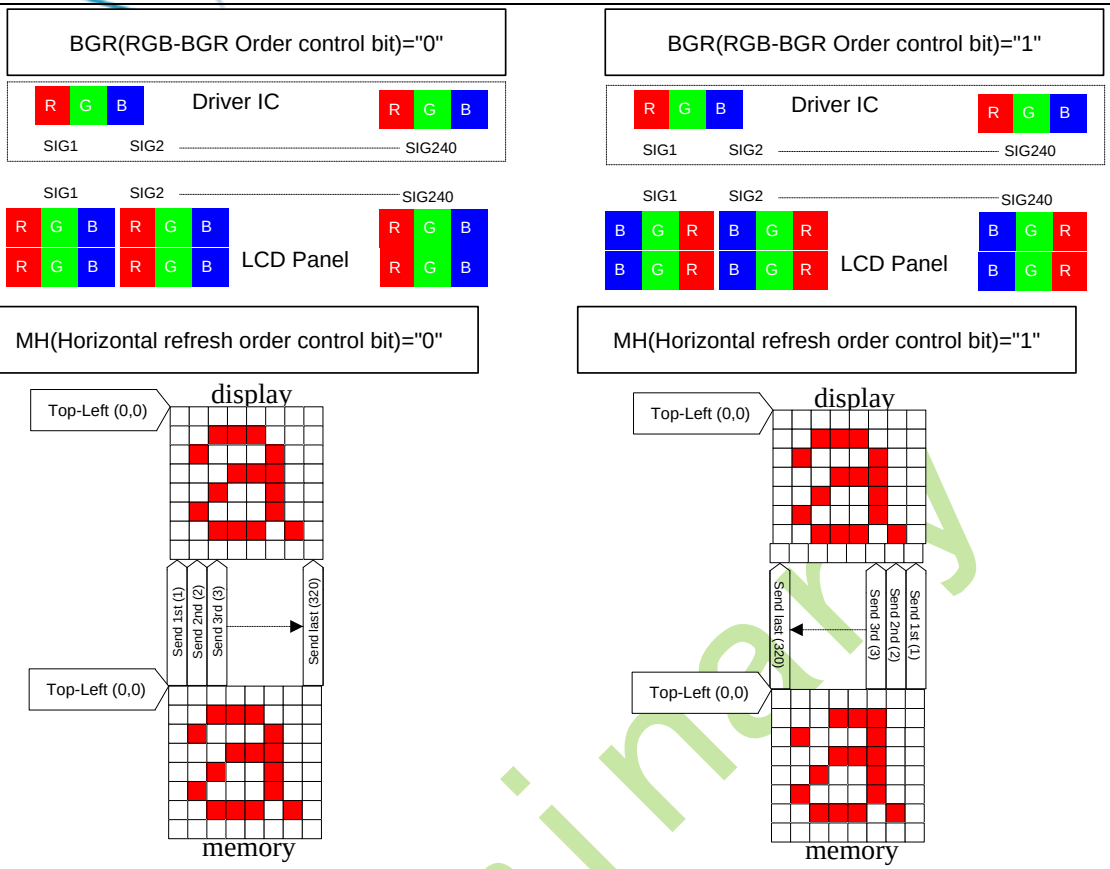
Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.

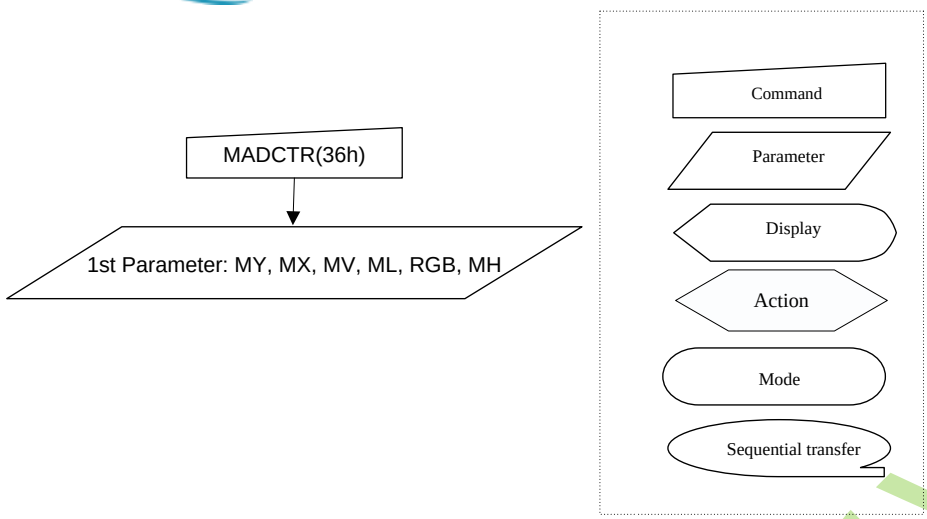


Preliminary

<table>
<tr><td></td><td>


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
</table>

Preliminary

Flow Chart	

Preliminary

6.2.27. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37
1st Parameter	1	1	↑	XX	00								00
2nd Parameter	1	1	↑	XX	SSA [7:0]								00

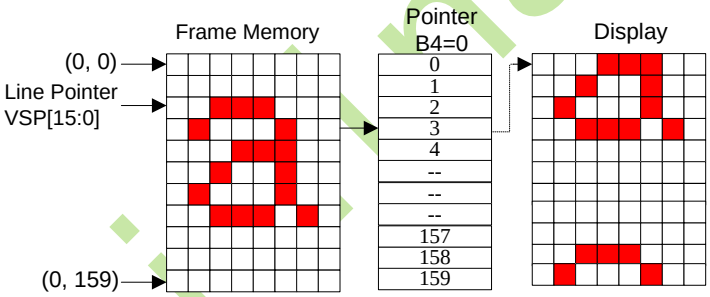
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When MADCTL B4=0

Example:

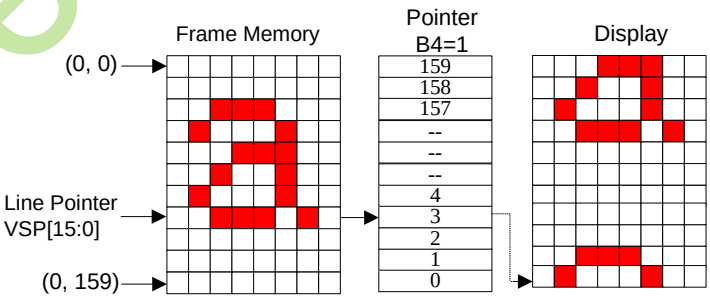
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and VSP='3'.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the GC9106 enters Partial mode.

X = Don't care

Restriction	This command has no effect when Tearing Effect output is already ON

Preliminary

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [7:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

Preliminary

6.2.28. Idle Mode OFF (38h)

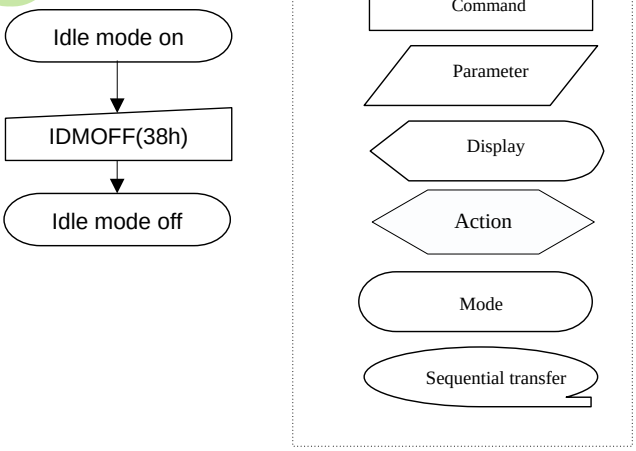
38h	Idle Mode OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

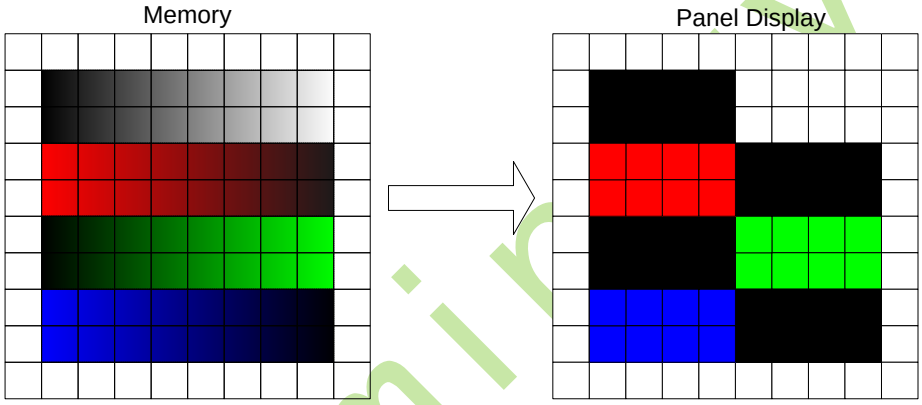
Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



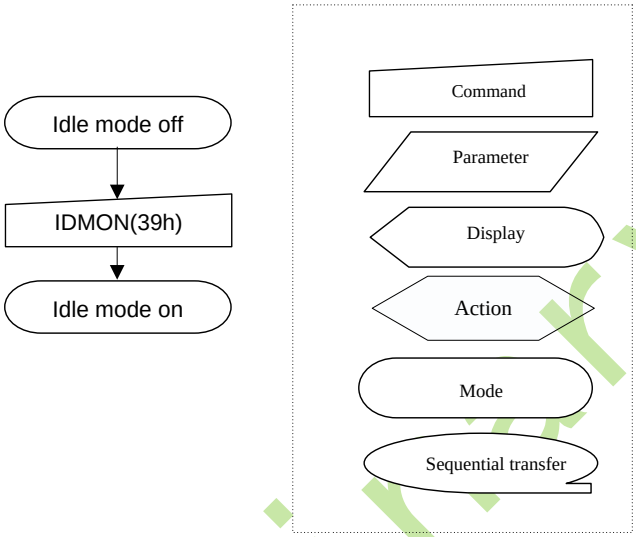
Preliminary

6.2.29. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.


<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XX XX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

Preliminary

	Status / Default Value
	Power On Sequence: Idle mode OFF
	SW Reset: Idle mode OFF
	HW Reset: Idle mode OFF
Flow Chart	

Preliminary

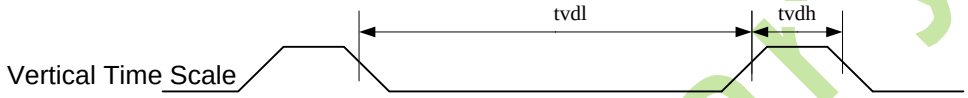
6.2.30. COLMOD: Pixel Format Set (3Ah)

<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">IFPF [2:0]</td><td>06</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. IFPF [2:0] is the pixel format of MCU interface. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">IFPF [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td colspan="3">others</td><td>Reserved</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>IFPF [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

Preliminary

6.2.31. Scan line set (44h)

<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">SCNL[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">SCNL[7:0]: When setting the SCNL[7:0] value, the following conditions shall be met: SCNL [7:0]≤160

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of SCNL [7:0]


Note:that set_tear_scanline with STS is equivalent to set_tear_on with 5+GateN(N=1、2、3...220)
eg:when the SCNL [7:0]=6,the TE will output at the position of Gate1.
when the SCNL [7:0]=7,the TE will output at the position of Gate2.
when the SCNL [7:0]=8,the TE will output at the position of Gate3.
…….</td></tr>
<tr><td>Restriction</td><td colspan="13">The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

Preliminary

6.2.32. Scan line Get (45h)

3Ah	Pixel Format Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	0	1	45
Parameter	1	1	↑	XX	SCNL[7:0]								--
Description	This command indicates the current status of CMD 44h(SCNL[7:0])												
Restriction	The Tearing Effect Output line shall be active low when the display module is in Sleep mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
SW Reset	8'h00
HW Reset	8'h00

Preliminary

6.2.33. Display Inversion Control (B4h)

<table>
<tr><td>B4h</td><td colspan="13">Frame Rate and Display Inversion Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>B4</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>bgr_comp</td><td>0</td><td>0</td><td colspan="3">inv_ctl[2:0]</td><td>20</td></tr>
<tr><td>Description</td><td colspan="13">Display inversion mode set
inv_ctl[2:0]: Inversion setting in full colors normal mode(Normal mode on)
<table><tr><th>inv_ctl[2:0]</th><th>Inversion</th></tr><tr><td>0</td><td>Column inversion</td></tr><tr><td>1</td><td>1 dot inversion</td></tr><tr><td>2</td><td>2 dot inversion</td></tr><tr><td>3</td><td>4 dot inversion</td></tr><tr><td>4</td><td>8 dot inversion</td></tr></table>bgr_comp:
<table><tr><th>bgr_comp</th><th>Description</th></tr><tr><td>0</td><td>Fix 0</td></tr><tr><td>1</td><td>Fix high value</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h20</td></tr><tr><td>SW Reset</td><td>8’h20</td></tr><tr><td>HW Reset</td><td>8’h20</td></tr></table></td></tr>
</table>

Preliminary

6.2.34. Read ID1 (DAh)

DAh	Read ID1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DA
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								00
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. The ID2 can be programmed by MTP function. X = Don't care												
Restriction	None												

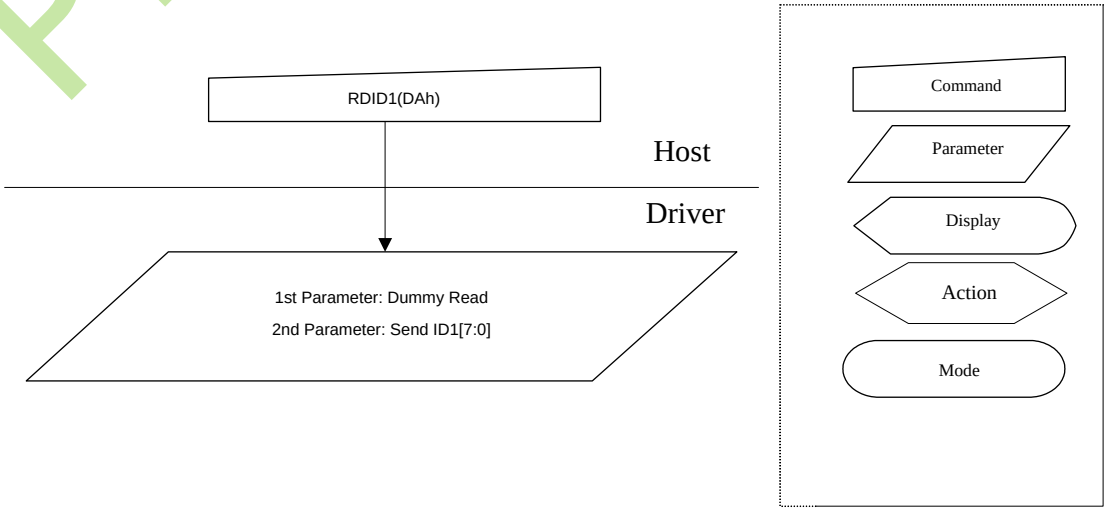
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00	8'h00
SW Reset	8'h00	8'h00
HW Reset	8'h00	8'h00

Flow Chart



Preliminary

6.2.35. Read ID2 (DBh)

DBh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DB
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2 [7:0]								91
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction	None												

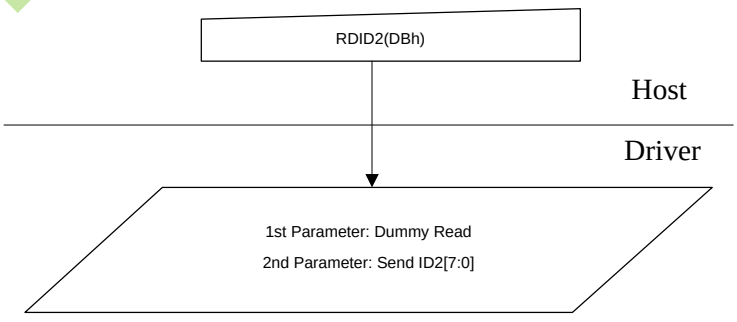
Register Availability

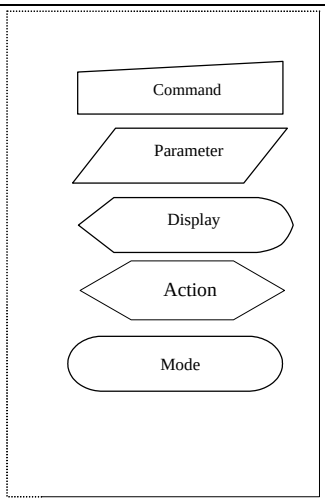
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h91	8'h91
SW Reset	8'h91	8'h91
HW Reset	8'h91	8'h91

Flow Chart





Preliminary

6.2.36. Read ID3 (DCh)

DCh	Read ID3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DC
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								06
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

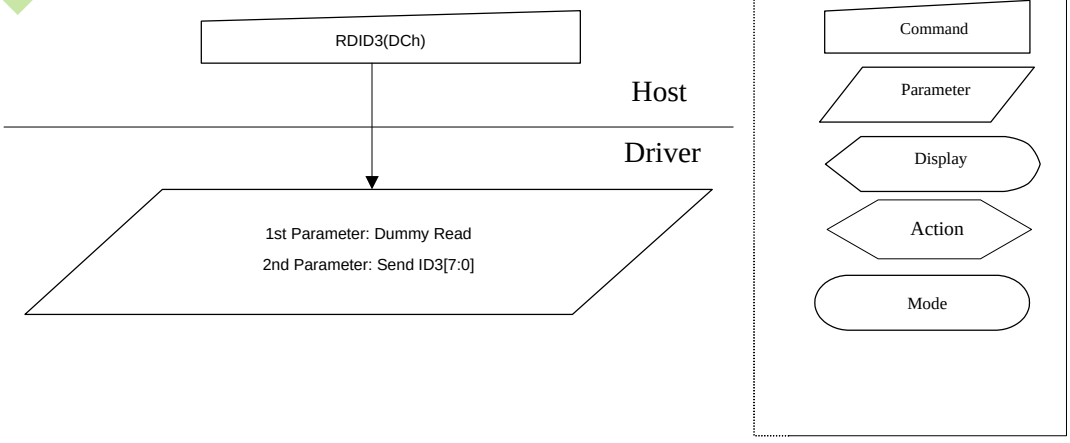
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h04	8'h06
SW Reset	8'h04	8'h06
HW Reset	8'h04	8'h06

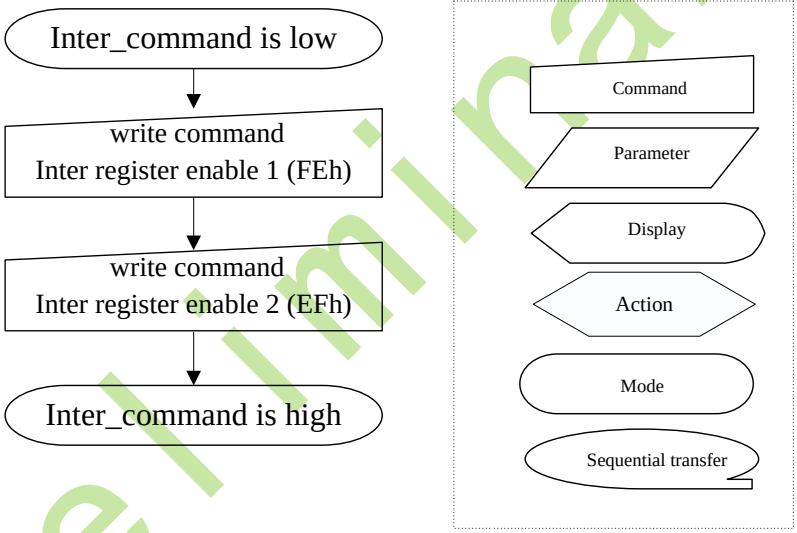
Flow Chart



Preliminary

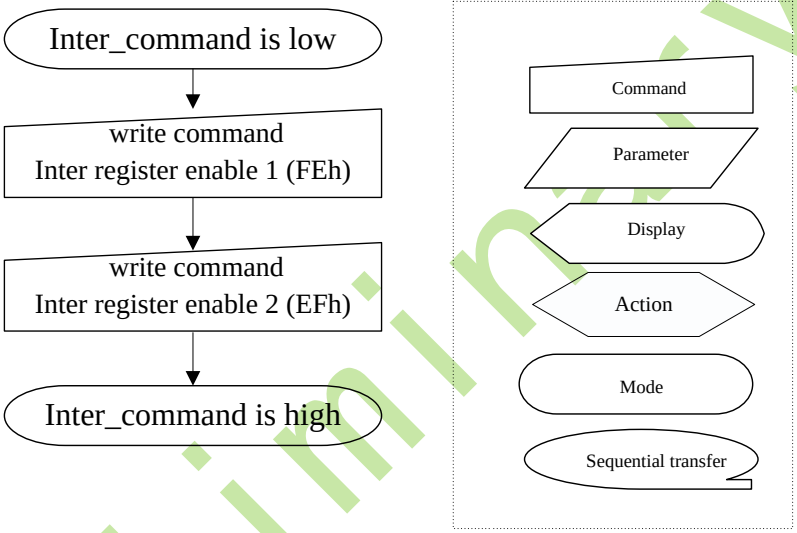
6.3. Description of Internal Command

6.3.1. Inter register enable 1 (FEh)

FEh	Inter register enable 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability	Status	Availability
---	---	---
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

6.3.2. Inter register enable 2 (EFh)

EFh	Inter register enable 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

6.3.3. Frame Rate Set(A3h)

A3h	Frame Rate set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	0	1	1	A3
1st Parameter	1	1	↑	XX	0	RTN1 [6:0]							16

Description

To have access to "A3h" , bit [0] of "B6h" need be set to 1

Frame Rate=18MHz/190/（4*(128*(rtn1[6:4]+2)+8*rtn1[3:0])）

Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)
0x00	91.8	0x10	61.2	0x20	45.9	0x30	36.7	0x40	30.6	0x50	26.2	0x60	22.9	0x70	20.4
0x01	89.0	0x11	59.9	0x21	45.2	0x31	36.2	0x41	30.2	0x51	26.0	0x61	22.7	0x71	20.2
0x02	86.4	0x12	58.7	0x22	44.5	0x32	35.8	0x42	29.9	0x52	25.7	0x62	22.6	0x72	20.1
0x03	83.9	0x13	57.6	0x23	43.8	0x33	35.4	0x43	29.6	0x53	25.5	0x63	22.4	0x73	19.9
0x04	81.6	0x14	56.5	0x24	43.2	0x34	34.9	0x44	29.3	0x54	25.3	0x64	22.2	0x74	19.8
0x05	79.4	0x15	55.4	0x25	42.6	0x35	34.5	0x45	29.0	0x55	25.1	0x65	22.0	0x75	19.7
0x06	77.3	0x16	54.3	0x26	42.0	0x36	34.1	0x46	28.8	0x56	24.8	0x66	21.9	0x76	19.6
0x07	75.3	0x17	53.4	0x27	41.4	0x37	33.7	0x47	28.5	0x57	24.6	0x67	21.7	0x77	19.4
0x08	73.4	0x18	52.4	0x28	40.8	0x38	33.3	0x48	28.2	0x58	24.4	0x68	21.6	0x78	19.3
0x09	71.6	0x19	51.5	0x29	40.2	0x39	33.0	0x49	27.9	0x59	24.2	0x69	21.4	0x79	19.2
0x0a	69.9	0x1a	50.6	0x2a	39.7	0x3a	32.6	0x4a	27.7	0x5a	24.0	0x6a	21.2	0x7a	19.0
0x0b	68.3	0x1b	49.7	0x2b	39.1	0x3b	32.2	0x4b	27.4	0x5b	23.8	0x6b	21.1	0x7b	18.9
0x0c	66.7	0x1c	48.9	0x2c	38.6	0x3c	31.9	0x4c	27.2	0x5c	23.7	0x6c	20.9	0x7c	18.8
0x0d	65.2	0x1d	48.1	0x2d	38.1	0x3d	31.6	0x4d	26.9	0x5d	23.5	0x6d	20.8	0x7d	18.7
0x0e	63.8	0x1e	47.4	0x2e	37.6	0x3e	31.2	0x4e	26.7	0x5e	23.3	0x6e	20.7	0x7e	18.6
0x0f	62.5	0x1f	46.6	0x2f	37.2	0x3f	30.9	0x4f	26.4	0x5f	23.1	0x6f	20.5	0x7f	18.4

Restriction: Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h16

Preliminary

		SW Reset	8’h16
		HW Reset	8’h16

Preliminary

6.3.4. SPI 2 DATA(AAh)

<table>
<tr><td>A3h</td><td colspan="13">Frame Rate set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>AA</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SPI2_EN</td><td colspan="3">SPI_2DATA_MDT[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “AAh”, bit [2] of “B6h” need be set to 1

2DATA_EN Set 2_data_line mode in 3-wire SPI.

2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

<table>
<tr><th>2DATA_MDT[2:0]</th><th>Data Format</th></tr>
<tr><td>000</td><td>65K color 1pixle/transition</td></tr>
<tr><td>001</td><td>262K color 1pixle/transition</td></tr>
<tr><td>010</td><td>262K color 2/3pixle/transition</td></tr>
<tr><td>100</td><td>4M color 1pixle/transition</td></tr>
<tr><td>110</td><td>4M color 2/3pixle/transition</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

Preliminary

6.3.5. AVDD_CLK (C0h)

<table>
<tr><td>A3h</td><td colspan="13">AVDD_CLK</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C0</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>1</td><td>1</td><td>0</td><td colspan="2">AVDD_CLK AD[1:0]</td><td>0</td><td>1</td><td>1</td><td>CB</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “C0h”, bit [0] of “B0h” need be set to 1

AVDD_CLKAD[1:0]:
<table>
<tr><th>AVDD_CLK_AD</th><th>AVDD (V)</th><th>AVDD Operation (MHZ)</th></tr>
<tr><td>0</td><td>7.42</td><td>8</td></tr>
<tr><td>1</td><td>7.31</td><td>6</td></tr>
<tr><td>2</td><td>7.21</td><td>4.8</td></tr>
<tr><td>3</td><td>7.09</td><td>4</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’Hcb</td></tr>
<tr><td>SW Reset</td><td>8’Hcb</td></tr>
<tr><td>HW Reset</td><td>8’Hcb</td></tr>
</table></td></tr>
</table>

Preliminary

6.3.6. AVEE_CLK (C1h)

<table>
<tr><td>A3h</td><td colspan="13">AVEE_CLK</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>1</td><td>1</td><td>0</td><td colspan="2">AVEE_CLK AD[1:0]</td><td>0</td><td>1</td><td>1</td><td>CB</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “C1h”, bit [1] of “B0h” need be set to 1

AVEE_CLKAD[1:0]:
<table>
<tr><th>AVEE_CLK_AD</th><th>AVEE (V)</th><th>AVEE Operation (MHZ)</th></tr>
<tr><td>0</td><td>-5.06</td><td>8</td></tr>
<tr><td>1</td><td>-5.04</td><td>6</td></tr>
<tr><td>2</td><td>-5.03</td><td>4.8</td></tr>
<tr><td>3</td><td>-4.99</td><td>4</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’Hcb</td></tr>
<tr><td>SW Reset</td><td>8’Hcb</td></tr>
<tr><td>HW Reset</td><td>8’Hcb</td></tr>
</table></td></tr>
</table>

Preliminary

6.3.7. VGH_CLK (C2h)

A3h	VGH_CLK												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	0	C2
1st Parameter	1	↑	1	XX	0	1	0	0	VGH_CLKAD[3:0]				48

Description

To have access to "C2h", bit [2] of "B0h" need be set to 1

VGH_CLKAD[3:0]:

VGH_CLK_AD	VGH (V)	VGH Operation (MHZ)	VGH_CLK_AD	VGH (V)	VGH Operation (MHZ)
0	8.98	6	**8**	13.38	1
1	9.73	4.8	**9**	13.51	0.8
2	10.34	4	**10**	13.78	0.6
3	11.12	3	**11**	13.78	0.5
4	11.73	2.4	**12**	13.87	0.4
5	12.21	2	**13**	13.99	0.3
6	12.57	1.6	**14**	13.81	0.2
7	13.10	1.2	**15**	13.06	0.1

Restriction: Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'H48
SW Reset	8'H48
HW Reset	8'H48

Preliminary

6.3.8. VGL_CLK (C3h)

A3h	VGL_CLK												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3
1st Parameter	1	↑	1	XX	0	1	0	0	VGL_CLKAD[3:0]				48

Description

To have access to "C3h", bit [3] of "B0h" need be set to 1

VGL_CLKAD[3:0]:

VGL_CLK_AD	VGL (V)	VGL Operation (MHZ)	VGL_CLK_AD	VGL (V)	VGL Operation (MHZ)
0	-11.71	6	**8**	-13.08	1
1	-12.04	4.8	**9**	-13.08	0.8
2	-12.25	4	**10**	-13.12	0.6
3	-12.59	3	**11**	-13.11	0.5
4	-12.68	2.4	**12**	-13.07	0.4
5	-12.77	2	**13**	-13.02	0.3
6	-12.90	1.6	**14**	-12.85	0.2
7	-12.98	1.2	**15**	-12.35	0.1

Restriction: Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'H48
SW Reset	8'H48
HW Reset	8'H48

Preliminary

6.3.9. CHP_SOU_CLK (C6h)

<table>
<tr><td>A3h</td><td colspan="13">CHP_SOU_CLK</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>C6</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td colspan="3">CHP_SOU_CLKAD[2:0]</td><td>1A</td></tr>
<tr><td>2ed Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “C6h”, bit [6] of “B0h” need be set to 1

CHP_SOU_CLKAD[3:0]:
<table>
<tr><th>CHP_SOU_CLK_AD</th><th>BVDD (V)</th><th>BVEE(V)</th><th>CHP_SOU_CLK Operation (MHZ)</th></tr>
<tr><td>0</td><td>7.31</td><td>-4.76</td><td>12</td></tr>
<tr><td>1</td><td>7.58</td><td>-5.10</td><td>6</td></tr>
<tr><td>2</td><td>7.60</td><td>-5.14</td><td>4</td></tr>
<tr><td>3</td><td>7.60</td><td>-5.15</td><td>3</td></tr>
<tr><td>4</td><td>7.58</td><td>-5.14</td><td>2.4</td></tr>
<tr><td>5</td><td>7. 57</td><td>-5.14</td><td>2</td></tr>
<tr><td>6</td><td>7.56</td><td>-5.13</td><td>1.714</td></tr>
<tr><td>7</td><td>7.54</td><td>-5.13</td><td>1.5</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’H00</td></tr>
<tr><td>SW Reset</td><td>8’H00</td></tr>
<tr><td>HW Reset</td><td>8’H00</td></tr>
</table></td></tr>
</table>

Preliminary

6.3.10. VREG1_CTL (E6h)

<table>
<tr><td>A3h</td><td colspan="13">VREG1_CTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>E6</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="8">VREG1A_AD[6:0]</td><td>50</td></tr>
<tr><td>2ed Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="8">VREG1B_AD[6:0]</td><td>43</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “E6h”, bit [6] of “B1h” need be set to 1

VREG1A_AD[6:0]:

<table>
<tr><th>VREG1A_AD</th><th>VREG1A</th></tr>
<tr><td>0</td><td>4.5V</td></tr>
<tr><td>...</td><td>25mV/STEP</td></tr>
<tr><td>40</td><td>5.5V</td></tr>
<tr><td>...</td><td>12.5mV/STEP</td></tr>
<tr><td>80</td><td>6V</td></tr>
<tr><td>...</td><td>12.5mV/STEP</td></tr>
<tr><td>102</td><td>6.275V</td></tr>
<tr><td>...</td><td>25mV/STEP</td></tr>
<tr><td>127</td><td>6.9V</td></tr>
</table>

VREG1B_AD[6:0]:

<table>
<tr><th>VREG1B_AD</th><th>VREG1B</th></tr>
<tr><td>0</td><td>0.57V</td></tr>
<tr><td>...</td><td>20mV/STEP</td></tr>
<tr><td>26</td><td>1.09V</td></tr>
<tr><td>...</td><td>10mV/STEP</td></tr>
<tr><td>67</td><td>1.5V</td></tr>
<tr><td>...</td><td>10mV/STEP</td></tr>
<tr><td>103</td><td>1.86V</td></tr>
<tr><td>...</td><td>20mV/STEP</td></tr>
<tr><td>127</td><td>2.34V</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register</td><td></td><td colspan="9">Status</td><td colspan="2">Availability</td><td></td></tr>
</table>

Preliminary

Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default		Status	Default Value
		Power On Sequence	16'H5043
		SW Reset	16'H5043
		HW Reset	16'H5043

Preliminary

6.3.11. VREG2_CTL (E7h)

<table>
<tr><td>A3h</td><td colspan="13">VREG2_CTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>E7</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="8">VREG2A_AD[6:0]</td><td>38</td></tr>
<tr><td>2ed Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="8">VREG2B_AD[6:0]</td><td>43</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “E7h”, bit [7] of “B1h” need be set to 1

VREG2A_AD[6:0]:

<table>
<tr><th>VREG2A_AD</th><th>VREG2A</th></tr>
<tr><td>0</td><td>-2V</td></tr>
<tr><td>...</td><td>25mV/STEP</td></tr>
<tr><td>24</td><td>-2.6V</td></tr>
<tr><td>...</td><td>12.5mV/STEP</td></tr>
<tr><td>56</td><td>-3V</td></tr>
<tr><td>...</td><td>12.5mV/STEP</td></tr>
<tr><td>86</td><td>-3.375V</td></tr>
<tr><td>...</td><td>25mV/STEP</td></tr>
<tr><td>127</td><td>-4.4V</td></tr>
</table>

VREG2B_AD[6:0]:

<table>
<tr><th>VREG1B_AD</th><th>VREG2B</th></tr>
<tr><td>0</td><td>0.57V</td></tr>
<tr><td>...</td><td>20mV/STEP</td></tr>
<tr><td>26</td><td>1.09V</td></tr>
<tr><td>...</td><td>10mV/STEP</td></tr>
<tr><td>67</td><td>1.5V</td></tr>
<tr><td>...</td><td>10mV/STEP</td></tr>
<tr><td>103</td><td>1.86V</td></tr>
<tr><td>...</td><td>20mV/STEP</td></tr>
<tr><td>127</td><td>2.34V</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availabi ity</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
</table></td></tr>
</table>

Preliminary

		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default		Status	Default Value
		Power On Sequence	16'H3843
		SW Reset	16' H3843
		HW Reset	16' H3843

Preliminary

6.3.12. CHP_CLAMP_CTL1 (EAh)

<table>
<tr><td>A3h</td><td colspan="13">CHP_CLAMP_CTL1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>EA</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">VGH_AD[2:0]</td><td>0</td><td colspan="3">VGL_AD[2:0]</td><td>24</td></tr>
<tr><td>2ed Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>07</td></tr>
<tr><td>Description</td><td colspan="13">To have access to “EAh”, bit [2] of “B2h” need be set to 1

VGH_AD[2:0]:
<table><tr><th>VGH_AD</th><th>VGH (V)</th><th>VGH _AD</th><th>VGH (V)</th></tr><tr><td>0</td><td>9</td><td>4</td><td>11</td></tr><tr><td>1</td><td>9.5</td><td>5</td><td>11.5</td></tr><tr><td>2</td><td>10</td><td>6</td><td>12</td></tr><tr><td>3</td><td>10.5</td><td>7</td><td>12.5</td></tr></table>VGL_AD[2:0]:
<table><tr><th>VGL_AD</th><th>VGL (V)</th><th>VGL_AD</th><th>VGL (V)</th></tr><tr><td>0</td><td>-8</td><td>4</td><td>-10</td></tr><tr><td>1</td><td>-8.5</td><td>5</td><td>-10.5</td></tr><tr><td>2</td><td>-9</td><td>6</td><td>-11</td></tr><tr><td>3</td><td>-9.5</td><td>7</td><td>-11.5</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availabili y</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>16’H2407</td></tr><tr><td>SW Reset</td><td>16’ H2407</td></tr><tr><td>HW Reset</td><td>16’ H2407</td></tr></table></td></tr>
</table>

Preliminary

6.3.13. CHP_CLAMP_CTL2 (EBh)

<table>
<tr><td>A3h</td><td colspan="13">CHP_CLAMP_CTL2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>EB</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">AVEE_AD[2:0]</td><td>0</td><td colspan="3">AVDD_AD[2:0]</td><td>33</td></tr>
<tr><td>2ed Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">BVEE_AD[2:0]</td><td>0</td><td colspan="3">BVDD_AD[2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">
To have access to “EBh”, bit [3] of “B2h” need be set to 1

AVEE_AD[2:0]:
<table>
<tr><th>AVEE_AD</th><th>AVEE (V)</th><th>AVEE _AD</th><th>AVEE (V)</th></tr>
<tr><td>0</td><td>-4.88</td><td>4</td><td>-4.4</td></tr>
<tr><td>1</td><td>-4.76</td><td>5</td><td>-4.28</td></tr>
<tr><td>2</td><td>-4.64</td><td>6</td><td>-4.16</td></tr>
<tr><td>3</td><td>-4.52</td><td>7</td><td>-4.04</td></tr>
</table>
AVDD_AD[2:0]:
<table>
<tr><th>AVDD_AD</th><th>AVDD (V)</th><th>AVDD_AD</th><th>AVDD (V)</th></tr>
<tr><td>0</td><td>6.92</td><td>4</td><td>6.44</td></tr>
<tr><td>1</td><td>6.8</td><td>5</td><td>6.32</td></tr>
<tr><td>2</td><td>6.68</td><td>6</td><td>6.2</td></tr>
<tr><td>3</td><td>6.56</td><td>7</td><td>6.08</td></tr>
</table>
BVEE_AD[2:0]:
<table>
<tr><th>BVEE_AD</th><th>BVEE (V)</th><th>BVEE _AD</th><th>BVEE (V)</th></tr>
<tr><td>0</td><td>-5.1</td><td>4</td><td>-4.7</td></tr>
<tr><td>1</td><td>-5.0</td><td>5</td><td>-4.6</td></tr>
<tr><td>2</td><td>-4.9</td><td>6</td><td>-4.5</td></tr>
<tr><td>3</td><td>-4.8</td><td>7</td><td>-4.4</td></tr>
</table>
BVDD_AD[2:0]:
<table>
<tr><th>BVDD_AD</th><th>BVDD (V)</th><th>BVDD_AD</th><th>BVDD (V)</th></tr>
<tr><td>0</td><td>7.1</td><td>4</td><td>6.7</td></tr>
<tr><td>1</td><td>7.0</td><td>5</td><td>6.6</td></tr>
<tr><td>2</td><td>6.9</td><td>6</td><td>6.5</td></tr>
<tr><td>3</td><td>6.8</td><td>7</td><td>6.4</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availabili y</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Preliminary

		Sleep In	Yes	
Default		Status	Default Value	
		Power On Sequence	16’H3366	
		SW Reset	16’H3366	
		HW Reset	16’H3366	

Preliminary

6.3.14. SET_GAMMA1 (F0h)

F0h	SET_GAMMA1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	0	F0
1st Parameter	1	1	↑	XX					VP0[3:0]				0F
2nd Parameter	1	1	↑	XX			VP1[5:0]						3F
3rd Parameter	1	1	↑	XX			VP2[5:0]						3F
4th Parameter	1	1	↑	XX					VP4[3:0]				0F
5th Parameter	1	1	↑	XX				VP6[4:0]					1A
6th Parameter	1	1	↑	XX					VP13[3:0]				0F
7th Parameter	1	1	↑	XX		VP20[6:0]							5A
8th Parameter	1	1	↑	XX	VP36[3:0]				VP27[3:0]				64
9th Parameter	1	1	↑	XX		VP43[6:0]							30
10th Parameter	1	1	↑	XX					VP50[3:0]				0A
11th Parameter	1	1	↑	XX				VP57[4:0]					15
12th Parameter	1	1	↑	XX					VP59[3:0]				05
13th Parameter	1	1	↑	XX			VP61[5:0]						19
14th Parameter	1	1	↑	XX			VP62[5:0]						19
15th Parameter	1	1	↑	XX					VP63[3:0]				02
Description	***To have access to "F0h" , bit [0] of "B3h" need be set to 1*** Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Inter command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

6.3.15. SET_GAMMA2 (F1h)

F1h	SET_GAMMA1												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1
1st Parameter	1	1	↑	XX					VN0[3:0]				0F
2nd Parameter	1	1	↑	XX			VN1[5:0]						3F
3rd Parameter	1	1	↑	XX			VN2[5:0]						2F
4th Parameter	1	1	↑	XX					VN4[3:0]				0F
5th Parameter	1	1	↑	XX				VN6[4:0]					15
6th Parameter	1	1	↑	XX					VN13[3:0]				0B
7th Parameter	1	1	↑	XX		VN20[6:0]							3A
8th Parameter	1	1	↑	XX	VN36[3:0]				VN27[3:0]				87
9th Parameter	1	1	↑	XX		VN43[6:0]							2F
10th Parameter	1	1	↑	XX					VN50[3:0]				0A
11th Parameter	1	1	↑	XX				VN57[4:0]					15
12th Parameter	1	1	↑	XX					VN59[3:0]				0F
13th Parameter	1	1	↑	XX			VN61[5:0]						1E
14th Parameter	1	1	↑	XX			VN62[5:0]						18
15th Parameter	1	1	↑	XX					VN63[3:0]				02

Description

To have access to "F1h" , bit [1] of "B3h" need be set to 1

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.

Restriction

Inter_command should be set high to enable this command

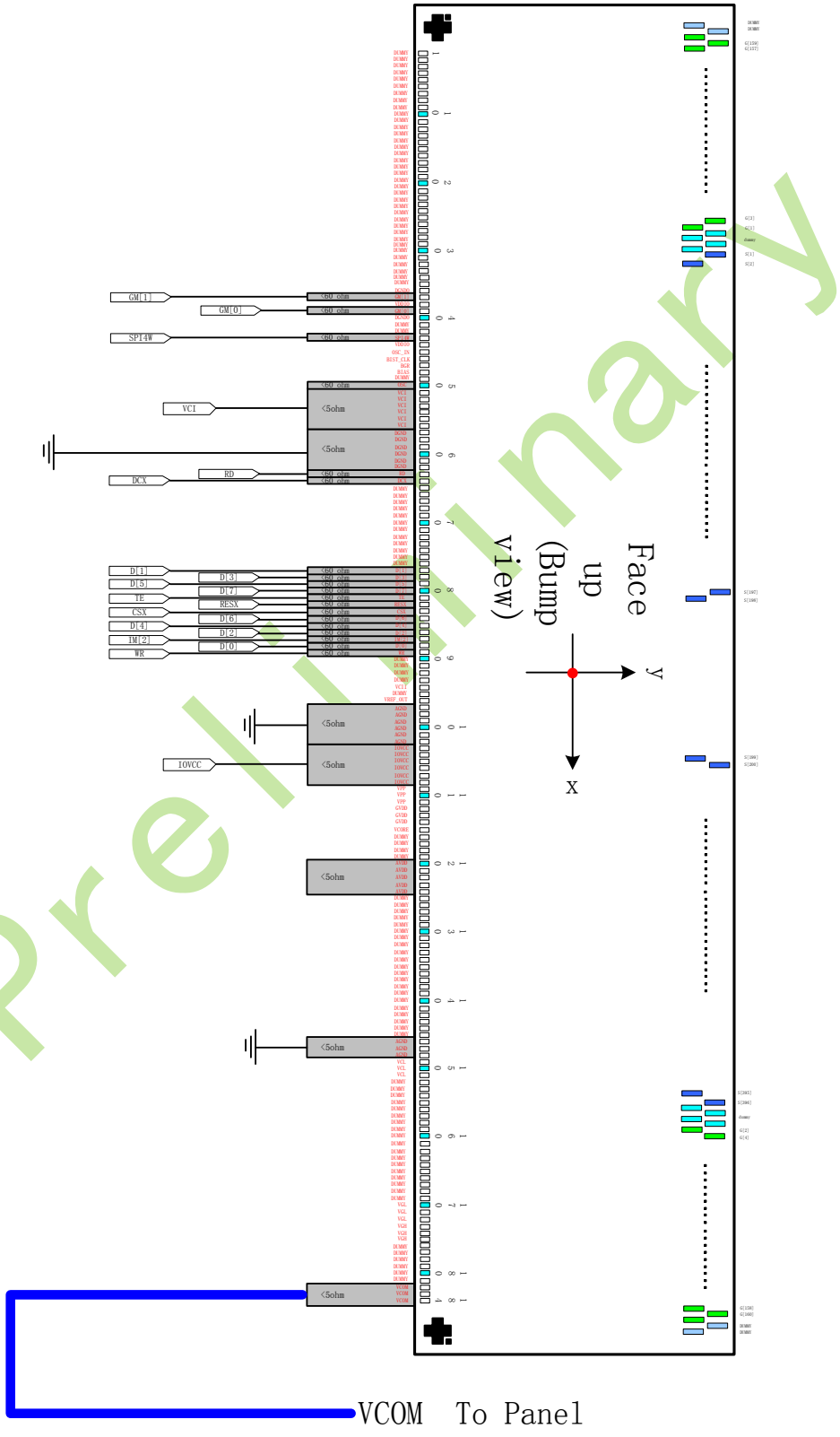
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Preliminary

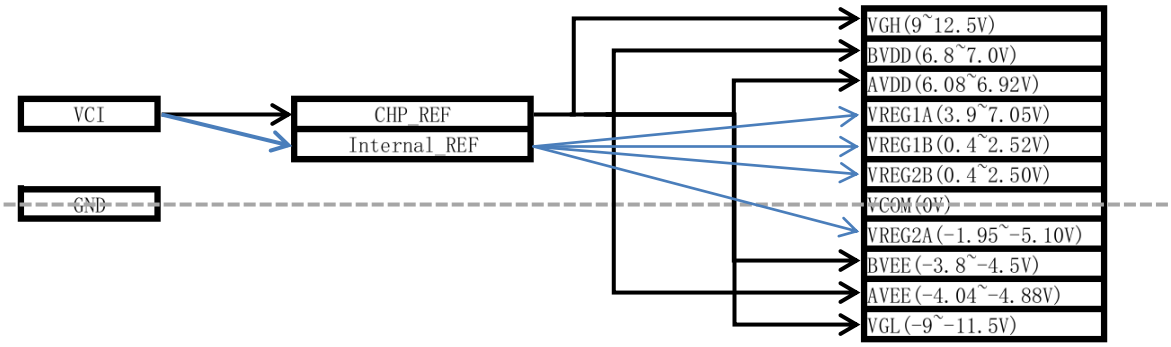
7. Application

7.1 APPLICATION CIRCUIT



Preliminary

7.2 Voltage Generation



Preliminary

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9106 is used out of the absolute maximum ratings, GC9106 may be permanently damaged. To use GC9106 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9106 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+85
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Preliminary

8.2. DC Characteristics

General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.8	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or DGND	-0.1	-	+0.1	Note1,2,3
Source Driver							
Source Output Range	Vsout	V	-	BVEE+0.1	-	BVDD -0.1	Note4
Gamma Reference Voltage	VREG1A	V	Operating voltage	4.5	-	6.9	
	VREG1B	V	Operating voltage	0.57		2.34	
	VREG2	V	Operating voltage	-4.4		-2	

Preliminary

	A						
	VREG2B	V	Operating voltage	0.57		2.34	

Note 1: VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDD voltage.

Note3 When the measurements are performed with LCD module. Measurement Points are like Note3.

Note4 VDD=2.6V

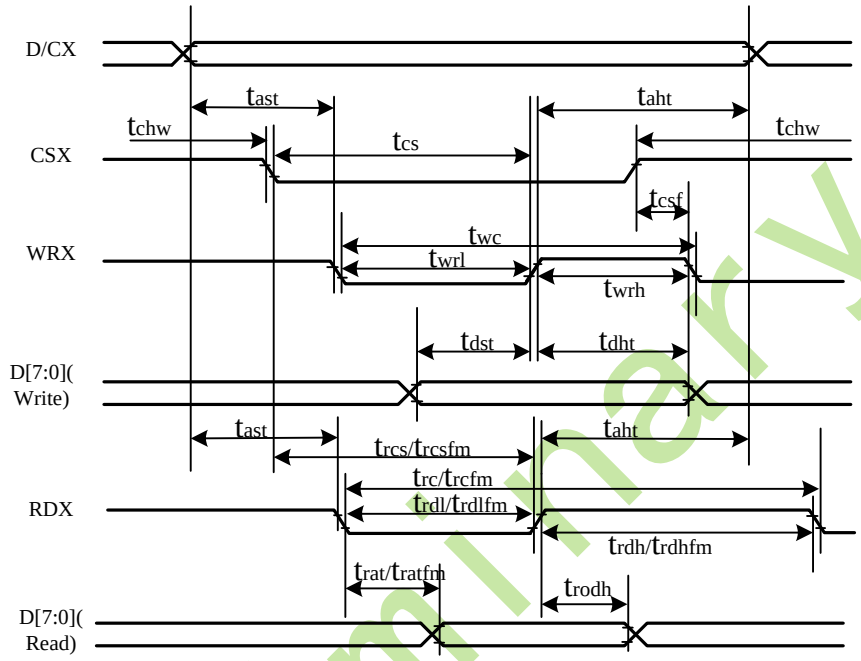
Note5 VDD=3.3V

Note6 The Max. Value is between with Note 4 measure point and Gamma setting value

Preliminary

8.3. AC Characteristics

8.3.1. Display Parallel 8-bit Interface Timing Characteristics (8080)

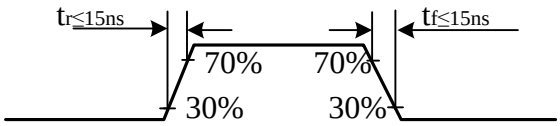


Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	45	-	ns	
D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	

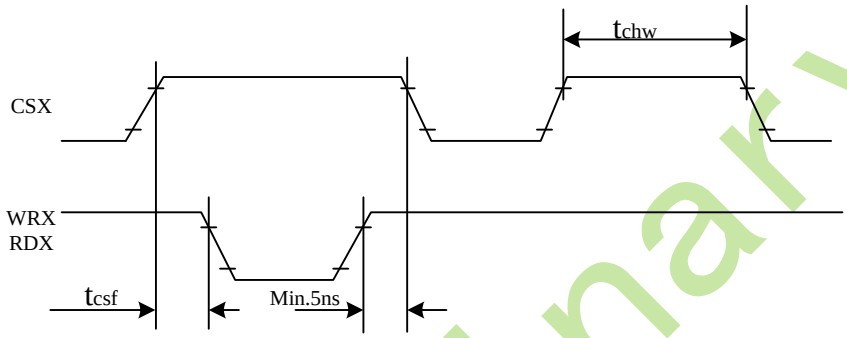
Preliminary

	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, DGND=0V

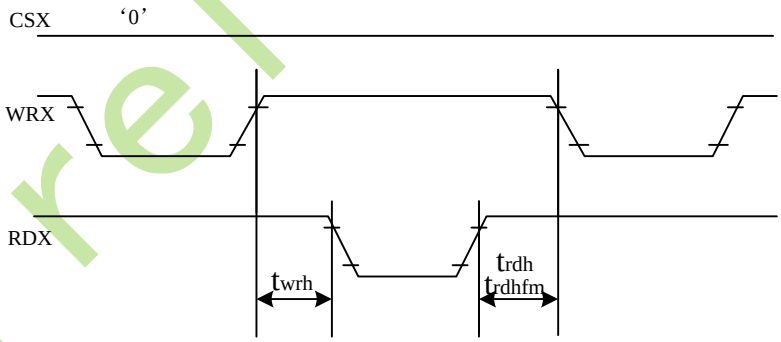


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

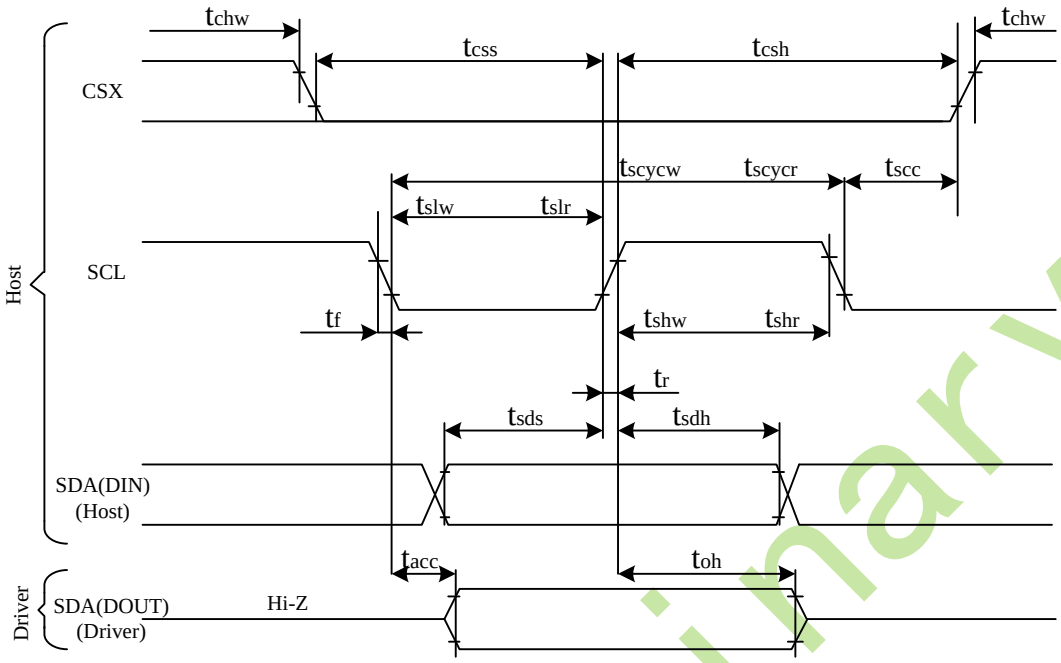
Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

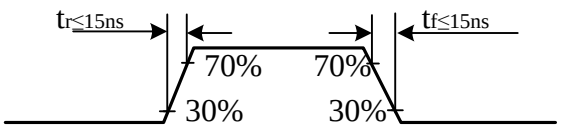
Preliminary

8.3.2. Display Serial Interface Timing Characteristics (3-line SPI system)



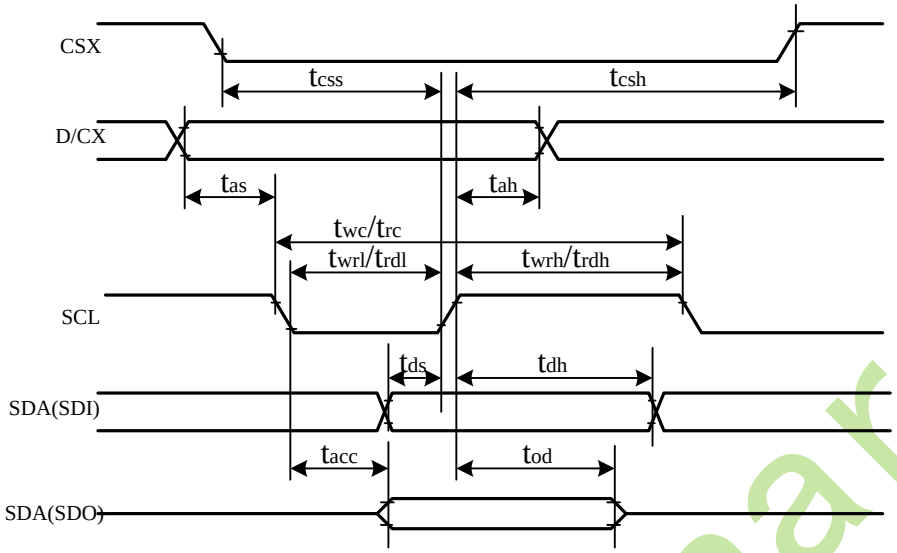
Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V



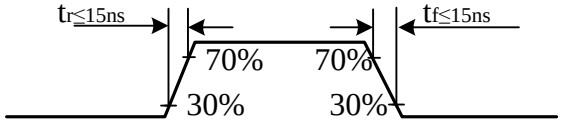
Preliminary

8.3.3. Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	100	-	ns	
	twrh	SCL "H" Pulse Width (Write)	40	-	ns	
	twrl	SCL "L" Pulse Width (Write)	40	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	toh	Output disable time (Read)	10	50	ns	For minmum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V



Preliminary

9. Revision History

Version No.	Date	Page	Description	Author
V1.00	2017-03-08	All	New Created	

Preliminary