PHOENIX DISPLAY
INTERNATIONAL, INC.

# PHOENIX DISPLAY INTERNATIONAL, INC

# SPECIFICATION FOR LCD MODULE

| | |
|---|---|
| **CUSTOMER** | |
| **PART NUMBER** | PDI070WSQH-53 |
| **DESCRIPTION** | 7.0" 1024 * (RGB) * 600 |
| **VERSION** | V1.0 |
| **ISSUE DATE** | 06-Jun-18 |

**COMPANY ADDRESS:**
**Phoenix Display International, Inc.**
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# REVISION RECORD

| REV NO | REV DATE | PAGE | CONTENTS | ISSUER |
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| 1.0 | 2018-6-6 | 19 | First Release | |

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## 1.0 GENERAL SPECIFICATIONS

**070WSQH-53 color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, FPC and a back light unit. The module display area contains1024*600pixels. This product accords with RoHS environmental criterion.**

| Item | Contents | Unit |
|---|---|---|
| Viewing direction | 12:00 | O' Clock |
| Number of Pixels | 1024(RGB) x600 | / |
| Number of color | 16.7M | / |
| outline dimension | 164.65*100*3.25 | |
| Display Mode | Normally White | / |
| Backlight Type | 3*6chips white LED | / |
| Interface Type | TTL | / |
| LCM Luminance | 220(typ) | cd/㎡ |
| Response Time (Tr+Tf) | 25ms (typ) | |
| Contrast Ratio | 200(typ) | |
| Input voltage | 3.3 | V |

## 2.0 ABSOLUTE MAXIMUM RATINGS

AGND= GND=0V, Ta = 25℃

| Parameter | Symbol | Spec. | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Power supply voltage 1 | VGH | -0.3 | - | +42.0 | V |
| Power supply voltage 2 | VDD | -0.3 | - | +6.0 | V |
| Power supply voltage 3 | VEE | VGH-42 | - | +0.3 | V |
| Input voltage | $V_{IN}$ | -0.3 | - | VDD+0.3 | V |

## 3.0 ELECTRICAL CHARACTERISTICS

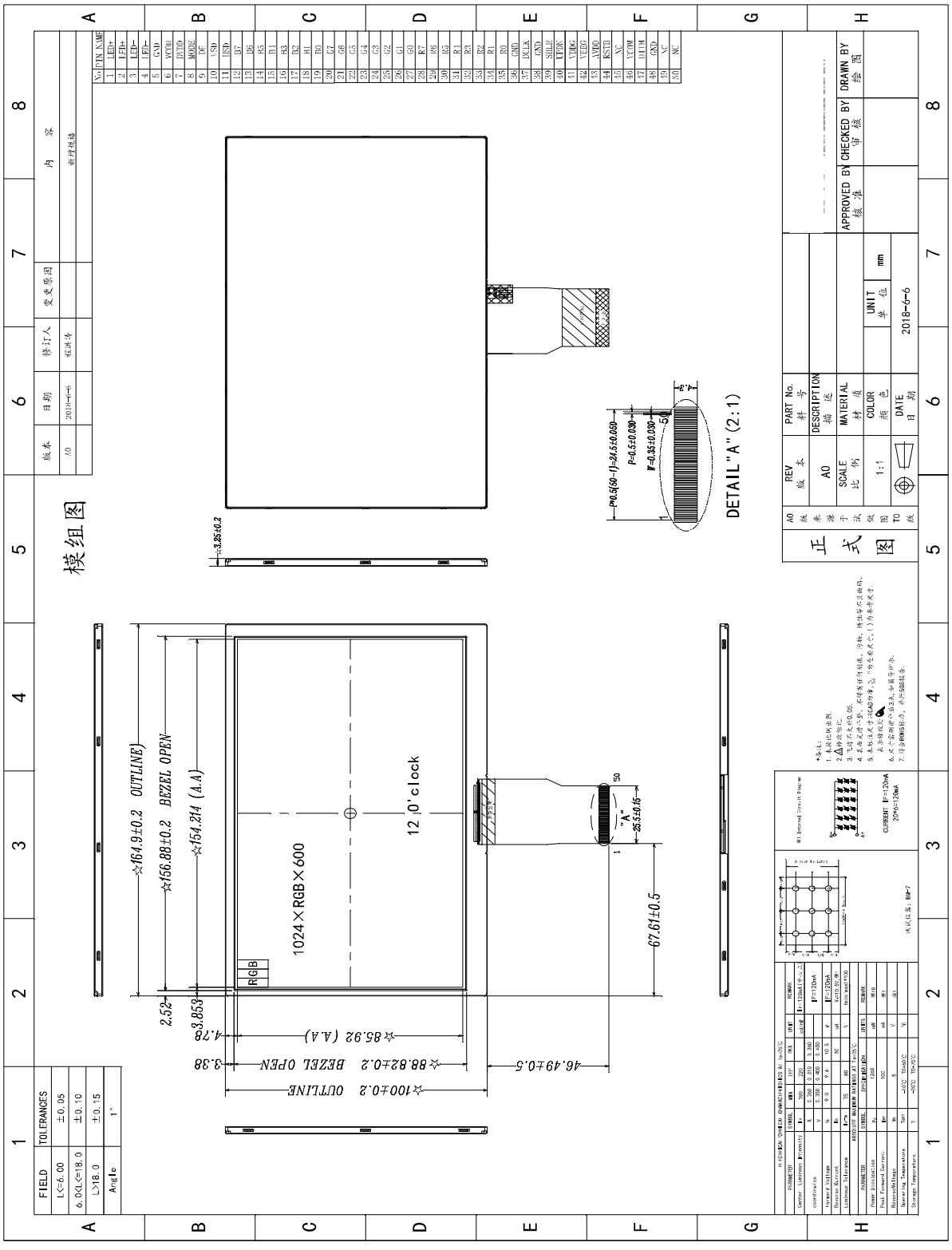
### 3.1 Typical Operation Condition

| Item | Symbol | Min. | TYP | Max. | Unit | NOTE |
|---|---|---|---|---|---|---|
| Digital Power Supply Voltage For LCD | VDD | 3.1 | 3.3 | 3.5 | V | |
| Analog Power Supply Voltage | AVDD | 9.4 | 9.6 | 9.8 | V | |
| TFT Gate on voltage | VGH | 16 | 17 | 18 | V | |
| TFT Gate off voltage | VGL | -8 | -7 | -6 | V | |
| Common Voltage | VCOM | 3.5 | 3.6 | 3.7 | V | |

### 3.1 BACKLIGHT CHARACTERISTICS

| Item | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Forward voltage | Vf | 9.0 | 9.6 | 10.5 | V | If=120mA |
| Luminance | Lv | 180 | 220 | - | cd/㎡ | If=120mA |
| Number of LED | – | 18 | | | Piece | – |
| Connection mode | P | 3serial 6 parallel | | | – | – |

# 4.0 DIMENSIONAL DRAWING



## 5.0 INTERFACE PIN CONNECTIONS

| Pin No. | Symbol | Function |
|---|---|---|
| 1,2 | VLED+ | Power for LED backlight (Anode) |
| 3,4 | VLED- | Power for LED backlight (Cathode) |
| 5 | GND | Power ground |
| 6 | VCOM | Common Voltage |
| 7 | DVDD | Digital Power |
| 8 | MODE | DE/SYNC mode select. Normally pull high<br>H: DE mode. L: HSD/VSD mode |
| 9: | DE | Data Enable signal. |
| 10 | VSD | Vertical sync input. Negative polarity |
| 11 | HSD | Horizontal sync input. Negative polarity |
| 12-19 | B7-B0 | Blue Data |
| 20-27 | G7-G0 | Green Data |
| 28-35 | R7-R0 | Red Data |
| 36 | GND | Ground |
| 37 | DCLK | Colock signal |
| 38 | GND | Display on/off |
| 39 | SHLR | Left or Right Display Control |
| 40 | UPDN | Up / Down Display Control |
| 41 | VDDG | Positive Power for TFT |
| 42 | VEEG | Negative Power for TFT |
| 43 | AVDD | Analog Power |
| 44 | RSTB | Global reset pin. (3.3V) |
| 45 | NC | Not connect |
| 46 | VCOM | Common Voltage |
| 47 | DITH | Dithering setting<br>DITH=”H” 8bit resolution(last 2 bit of input data truncated)<br>DITH=”L” 6bit resolution(default setting) |
| 48 | GND | Power ground |
| 49 | NC | Not connect |
| 50 | NC | Not connect |

# 6.0 TIMING CHARACTERISTICS OF INPUT SIGNAL

## 6.1 Timing characteristics of Input Signals

DE mode

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DCLK frequency @Frame rate=60hz | fclk | 40.8 | 51.2 | 67.2 | Mhz |
| Horizontal display area | thd | | 1024 | | DCLK |
| HSYNC period time | th | 1114 | 1344 | 1400 | DCLK |
| HSYNC blanking | thb+thfp | 90 | 320 | 376 | DCLK |
| Vertical display area | tvd | | 600 | | H |
| VSYNC period time | tv | 610 | 635 | 800 | H |
| VSYNC blanking | tvb+tvfp | 10 | 35 | 200 | H |

## 6.2 DC Characteristics

**(TA = -20 to 85° C, VDD = 2.3 to 3.6V, AVDD = 8 to 13.5V, GND = AGND = GND_LVDS = 0V)**

**TTL mode**

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Low level input voltage | Vil | For the digital circuit | 0 | - | 0.3×VDD | V |
| High level input voltage | Vih | For the digital circuit | 0.7×VDD | - | VDD | V |
| Input leakage current | Ii | For the digital circuit | - | - | ±1 | μA |
| High level output voltage | Voh | Ioh= -400 μA | VDD-0.4 | - | - | V |
| Low level output voltage | Vol | Iol= +400 μA | - | - | GND+0.4 | V |
| Pull low/high resistor | Ri | For the digital input pin @ VDD=3.3V | 200K | 250K | 300K | ohm |
| Digital Operation current | Idd | Fclk=65 MHz, FLD=50KHz, VDD=3.3V | - | 15 | 25 | mA |
| Digital Stand-by current | Ist1 | Clock and all functions are stopped | - | 10 | 50 | μA |
| Analog Operating Current | Idda | No load, Fclk=65MHz, FLD=50KHz @ AVDD=10V,V1=8V, V14=0.4V | - | 10 | 12 | mA |
| Analog Stand-by current | Ist2 | No load, Clock and all functions are Stopped | - | 10 | 50 | μA |
| Input level of V1 ~ V7 | Vref1 | Gamma correction voltage input | 0.4*AVDD | - | AVDD-0.1 | V |
| Input level of V8 ~ V14 | Vref2 | Gamma correction voltage input | 0.1 | - | 0.6*AVDD | V |
| Output Voltage deviation | Vod1 | Vo = AVSS+0.1V ~ AVSS+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V | - | ±20 | ±35 | mV |
| Output Voltage deviation | Vod2 | Vo = AVSS+0.5V ~ AVDD-0.5V | - | ±15 | ±20 | mV |
| Output Voltage Offset between Chips | Voc | Vo = AVSS+0.5V ~ AVDD-0.5V | - | - | ±20 | mV |
| Dynamic Range of Output | Vdr | SO1 ~ SO1536 | 0.1 | - | AVDD-0.1 | V |
| Sinking Current of Outputs | IOLy | SO1 ~ SO1536; Vo=0.1V v.s 1.0V , AVDD=13.5V | 80 | - | - | uA |
| Driving Current of Outputs | IOHy | SO1 ~ SO1536; Vo=13.4V v.s 12.5V , AVDD=13.5V | 80 | - | - | uA |
| Resistance of Gamma Table | Rg | Rn: Internal gamma resistor | 0.7*Rn | 1.0*Rn | 1.3*Rn | ohm |

## 6.3 AC Electrical characteristics

(TA = -20 to 85° C, VDD = 2.3 to 3.6V, AVDD = 8 to 13.5V, GND = AGND = 0V)

TTL mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD Power On Slew rate | TPOR | From 0V to 90% VDD | 1 | - | 20 | ms |
| RST pulse width | TRST | DCLK = 65MHz | 50 | - | - | us |
| DCLK cycle time | Tcph | - | 14 | - | - | ns |
| DCLK pulse duty | Tcwh | - | 40 | 50 | 60 | % |
| VSD setup time | Tvst | - | 5 | - | - | ns |
| VSD hold time | Tvhd | - | 5 | - | - | ns |
| HSD setup time | Thst | - | 5 | - | - | ns |
| HSD hold time | Thhd | - | 5 | - | - | ns |
| Data set-up time | Tdsu | D0[7:0], D1[7:0], D2[7:0] to DCLK | 5 | - | - | ns |
| Data hold time | Tdhd | D0[7:0], D1[7:0], D2[7:0] to DCLK | 5 | - | - | ns |
| DE setup time | Tesu | - | 5 | - | - | ns |
| DE hold time | Tehd | - | 5 | - | - | ns |
| Output stable time | Tsst | 10% to 90% target voltage. CL=90pF, R=10K ohm(Cascade) | - | - | 6 | us |
| | | Dual gate | | | 3 | |

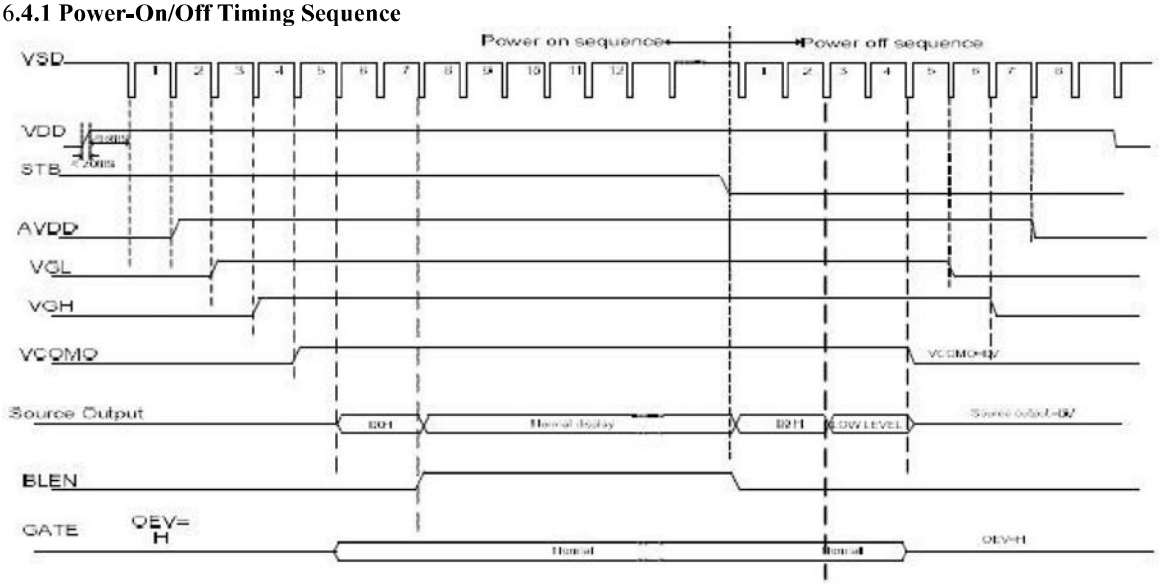
LVDS mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency | $R_{xFCLK}$ | | 20 | - | 71 | MHz |
| Input data skew margin | $T_{RSKM}$ | $\|V_{ID}\|$=400mV $R_{xVCM}$=1.2V $R_{xFCLK}$=71MHz | 500 | | | ps |
| Clock High Time | $T_{LVCH}$ | | | 4/(7* $R_{xFCLK}$) | | ns |
| | | | | | | ns |
| Clock Low Time | $T_{LVCL}$ | | | 3/(7* $R_{xFCLK}$) | | ns |
| PLL wake-up-time | $T_{enPLL}$ | | | | 150 | us |

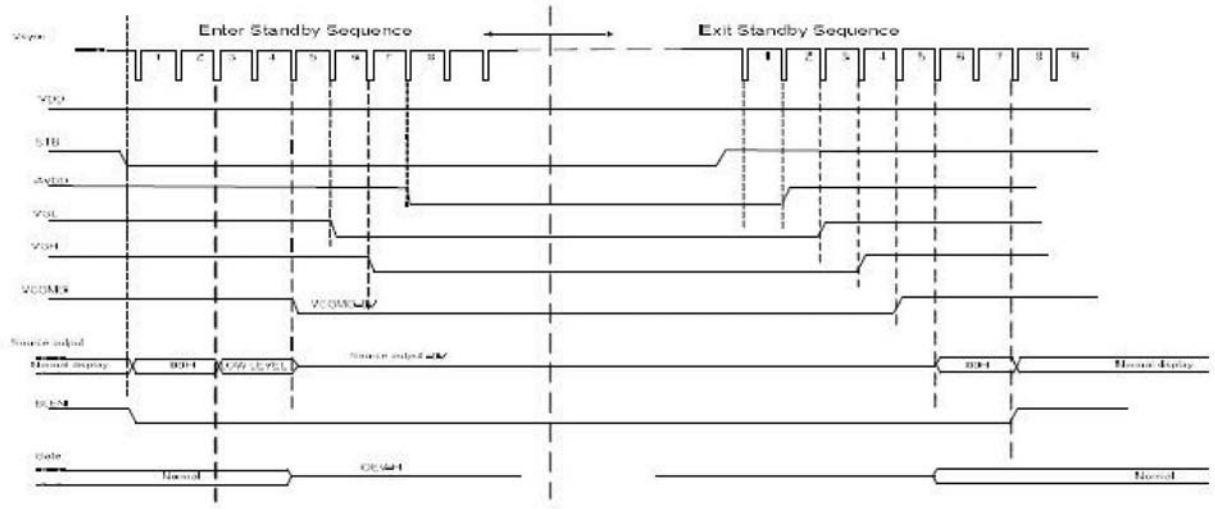
## 6.4 Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

### 6.4.1 Power-On/Off Timing Sequence




Power On/Off timing chart




Enter and Exit Standby Mode timing chart

Note: Low level=3Fh,when NBW=L(Normally white)

Low level=00h,when NBW=H(Normally black)

## 7.0 ELECTRO-OPTICAL CHARACTERISTICS

| ITEM | | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Panel Transmittance | | T | θ= 0° | -- | 6.5 | – | % | |
| Luminance | | L | θ= 0° | 180 | 220 | – | cd/m² | Note1 |
| Luminance Uniformity | | YU | 9points | 75 | 80 | – | % | Note5 |
| Contrast Ratio | | CR | Point-9 | -- | 200 | – | - | Note3 |
| Response Time | | Rr+Tf | Point-5 | -- | 25 | – | ms | Note4 |
| Viewing Angle | Horizontal | ΘL | Point-5 CR≧10 | – | 45 | – | | Note2 |
| | | ΘR | | – | 45 | – | | |
| | Vertical | ΘU | | -- | 45 | – | | |
| | | ΘD | | -- | 20 | – | | |
| Color Filter Chromaticity | White | X | θ= 0° | 0.260 | 0.310 | 0.360 | | Note1 |
| | | Y | | 0.350 | 0.400 | 0.450 | | |
| | Red | X | θ= 0° | TBD | TBD | TBD | | |
| | | Y | | TBD | TBD | TBD | | |
| | Green | X | θ= 0° | TBD | TBD | TBD | | |
| | | Y | | TBD | TBD | TBD | | |
| | Blue | X | θ= 0° | TBD | TBD | TBD | | |
| | | Y | | TBD | TBD | TBD | | |
| Color gamut ( NTSC ratio ) | | | | | TBD | | % | |

Test Conditions:

1. DVDD=3.1V, IL=265mA (Backlight current), the ambient temperature is 25℃.

2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

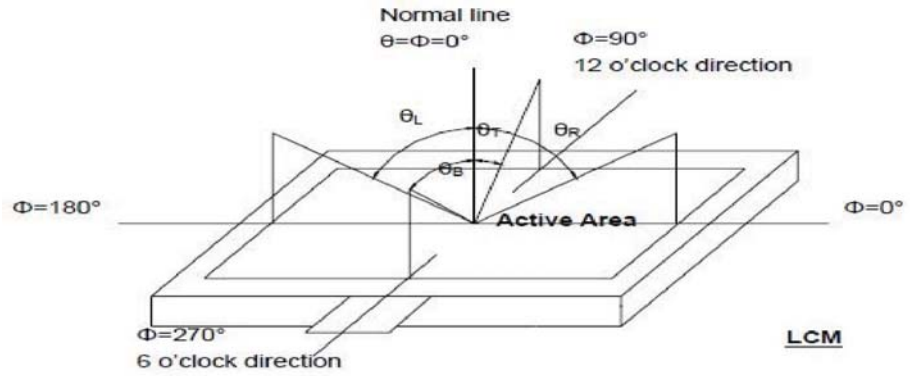



Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

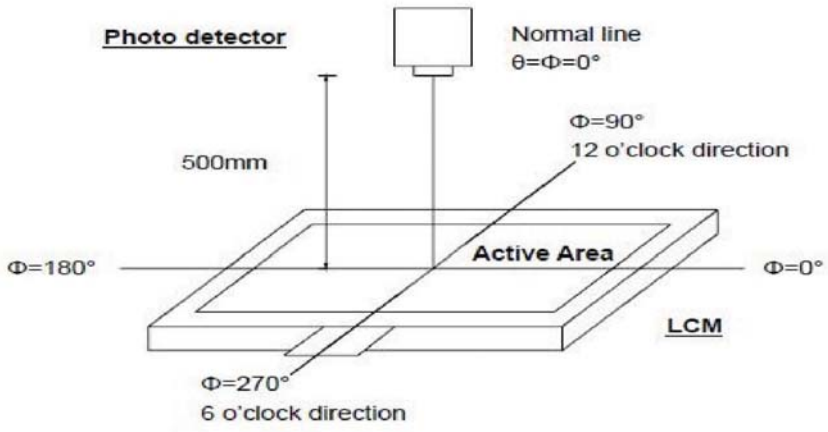



Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

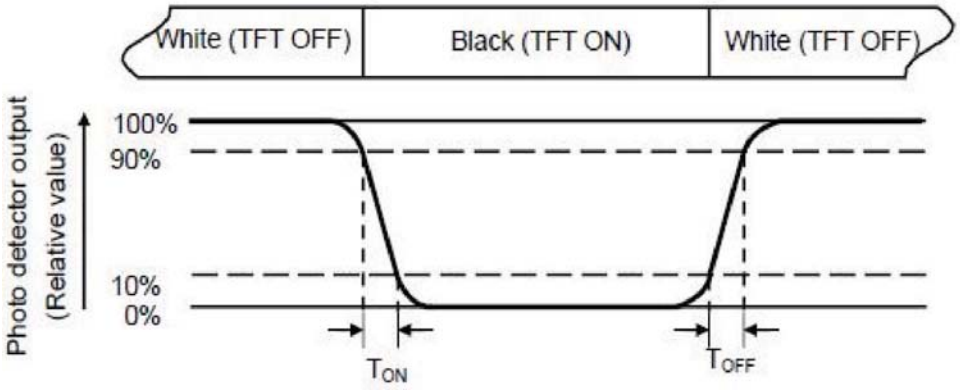



Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of luminance:

Measured at the center area of the panel when LCD panel is driven at "white " state. The LED driving condition is IL=265mA .

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4 ).Every measuring point is placed at the center of each measuring area

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

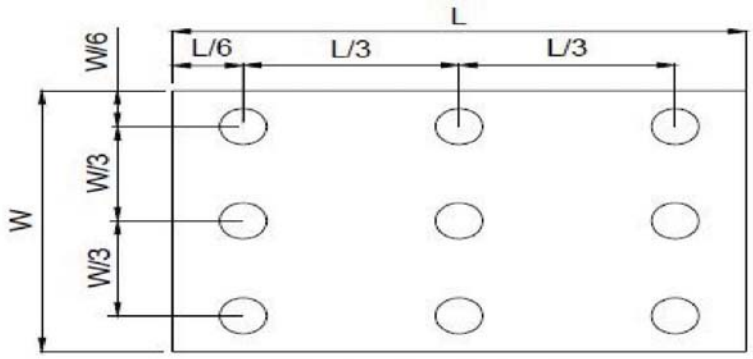



Fig. 4-4 Definition of measuring points

$B_{max}$: The measured maximum luminance of all measurement position.
$B_{min}$: The measured minimum luminance of all measurement position.

# 8.0 RELIABILITY

## 8.1 MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

## 8.2 TESTS

| NO. | Test Item | Test condition | Criterion |
|---|---|---|---|
| 1 | High Temperature Storage | 70℃±2℃ 96H<br>Restore 2H at 25℃<br>Power off | |
| 2 | Low Temperature Storage | -20℃±2℃ 96H<br>Restore 2H at 25℃<br>Power off | |
| 3 | High Temperature Operation | 60℃±2℃ 96H<br>Restore 2H at 25℃<br>Power on | |
| 4 | Low Temperature Operation | -10℃±2℃ 96H<br>Restore 2H at 25℃<br>Power on | |
| 5 | High Temperature & Humidity Operation | 50℃±2℃ 90%RH 96H<br>Power on | |
| 6 | Temperature Cycle | -20℃←→70℃<br>30min 30min<br>after 10cycle, Restore 2H at 25℃<br>Power off | Aftertesting,cosmetic and electrical defects should not happen. |
| 7 | Vibration Test | 10Hz~150Hz, 100m/s2, 120min | |
| 8 | Shock Test | Half-sinewave,300m/s2,11ms | |
| 9 | Drop Test(package state) | 800mm, concrete floor,1corner, 3edges, 6 sides each time | 1.After testing, cosmetic and electrical defects should not happen.<br>2.the product should remain at initial place<br>3.Product uncovered or package broken is not permitted. |
| 10 | Electro Static Discharge Test (non-operation) | 150pF，330Ω，Contact:±4KV,Air:±8KV<br>Measure point :LCD glass and metal bezel<br>200pF，0Ω，±200V contact test<br>Measure point :IF connector pins | IEC61000-4-2：2001<br>GB/T17626.2-2006 |

# 9.0 INSPECTION STANDARDS

## 9.1 Purpose

This incoming inspection standard shall be applied to TFT-LCD supplied byTSDto its customer.

## 9.2 Scope

This inspection standard contains Cosmetic Specifications and Electrical Specifications.

## 9.3 Classification of defects

9.3.1 Major defect.

The major defect is a defect that is likely to result in product failure or reduction in

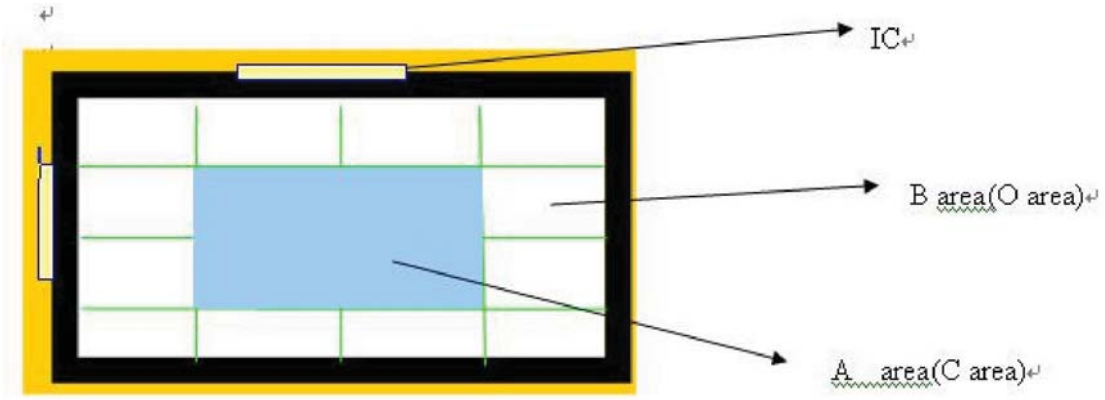
Product's intended usage.

9.3.2 Minor defect.

The minor defect is a defect that has little bearing on the effective use or Operation of the product.

## 9.4 Definition

9.4.1 Display area definition



## 9.5 Inspection conditions is as follows

9.5.1 Viewing distance is approximately 35-40 cm

9.5.2 Viewing angle is normal to the LCD panel as 45°

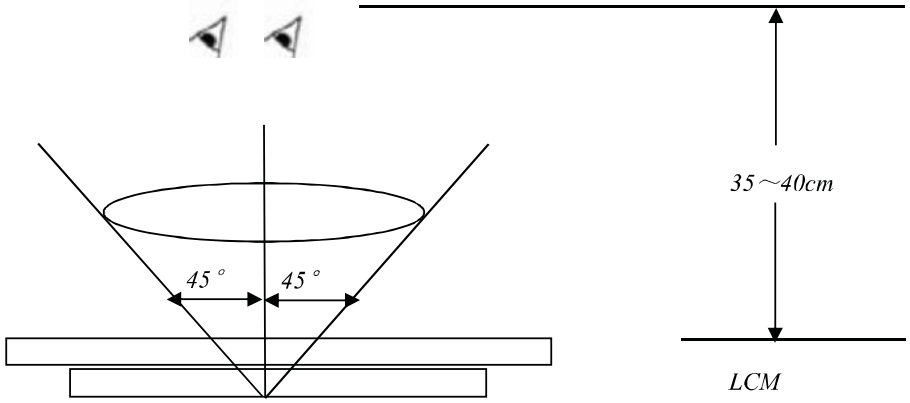
9.5.3 Ambient temperature is approximately 25±5°C

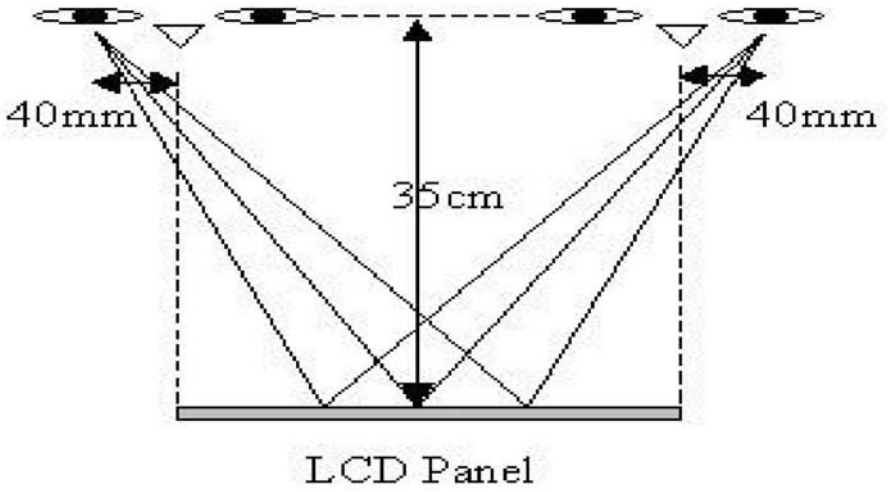
9.5.4 Ambient humidity is 60±5% RH

9.5.5 Ambient luminance is from 300-500 Lux.

9.5.6 Input signal timing should be typical value(3s-5s).

9.5.7 Mura & Light leakage inspection at ND-Filter 6%.



## 9.6 Sampling method

9.6.1 According to the MIL-STD-105E general inspection level , Ⅱ Sampling plan.

9.6.2 AQL: MA 0.65 MI 1.0

## 9.7 Inspection Criteria

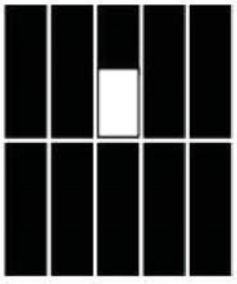
| DEFECT TYPE | | | LIMIT | | | Defect | Note |
|---|---|---|---|---|---|---|---|
| VISUAL DEFECT | SCRATCH | | W≤0.05mm and L≤5mm | | Ignore | Maj | NOTE1 |
| | | | 0.05mm<W≤0.2mm L≤10mm | | N≤4 | | |
| | | | 10mm<L, 0.1mm<W | | N=0 | | |
| | INTERNAL | SPOT | Φ≤0.2mm | | Ignore | | |
| | | | 0.2mm<Φ≤0.5mm | | N≤4 | | |
| | | | Φ>0.5mm | | N=0 | | |
| | | FIBER | 0.1mm≤W≤0.2mm L≤2.5mm | | N≤4 | | |
| | | | 0.2mm<W, 2.5mm<L | | N=0 | | |
| | | POLARIZER BUBBLE | Φ≤0.25mm | | Ignore | | |
| | | | 0.25mm<Φ≤0.5mm | | N≤4 | | |
| | | | Φ>0.5mm | | N=0 | | |
| | | DENT | Φ<0.25mm | | Ignore | | |
| | | | 0.25mm≤Φ≤0.5mm | | N≤4 | | |
| | | | Φ>0.5mm | | N=0 | | |
| ELECTRICAL DEFECT | BRIGHT DOT | | C Area | O Area | Total | Maj | NOTE2 NOTE3 |
| | | | N≤4（contain C area and O area） | | N≤4 | | |
| | DARK DOT | | N≤5（contain C area and O area） | | N≤5 | | |
| | TWO ADJACENT DOT | | N≤1 | N≤2 | N≤3 | | |
| | THREE OR MORE ADJACENT DOT | | NOT ALLOWLED | | | | |

| | | | | |
|---|---|---|---|---|
| | LINE DEFECT | NOT ALLOWLED | | |

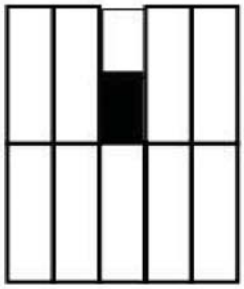
Note1: Minimum distance between dot defects and spot is 5mm;

Note2: The definition of Bright dot and Dark dot

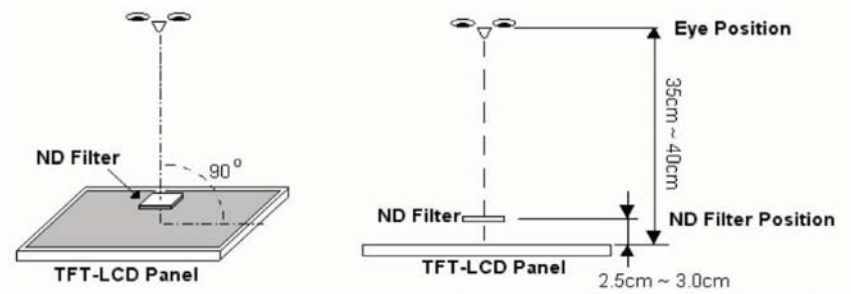
-bright area is more than 50% of one dot



-dark area is more than 50% of one dot



-The bright dot shall be visible under ND-Filter 5% as following:




NOTE3:

-A bit rate(bright dot model )≤10%;

-Class Chipping but not affect the function of quality OK;

-Polarizing film appearance does not affect the function OK;

## 10.0 PACKING DRAWING

TBD.

## 11.0 HANDLING PRECAUTION

(1) Don't disassemble and reassemble the module by self.
(禁止自行拆解)
(2) Acid, alkali, alcohol or touched directly by hand will damage the display.
(酸性、碱性、酒精或手的直接接触将会损伤显示面)
(3) Static electricity will damage the module. Please configure grounding device.
(静电会损伤模组，请装配接地设备)
(4)The strong vibration, shock, twist or bend will cause material damage, even module broken.
(强烈的撞击、震动、扭转或弯曲将会造成原材损伤，甚至面板破裂)
(5) It is easy to cause image sticking while displaying the same pattern for very long time.
(长期显示同一画面会造成影像残留)
(6) The response time, brightness and performance will vary from different temperature.
(响应时间、亮度与均匀性会因温度而有所改变)
(7) Starting from the date of shipment in the photoelectric products for a period of 12 months.
(从出货之日开始产品保质期为 12 个月)