DATA SHEET

(DOC No. HX8379-C-DS)

HX8379-C

480RGB x 864 dot,
16.7M color,
TFT Mobile Single Chip Driver

Version 01 December, 2013

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This document describes Himax IC, HX8379-C, which is a FWVGA (480RGBx864) resolution driving controller. HX8379-C is designed to provide a single-chip solution that combines source driver control, gate in panel control and power supply circuit to drive a TFT dot matrix LCD with 480RGB x 1024 dots at maximum.

HX8379-C can operate in low-voltage condition for the interface and produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8379-C also supports various functions to reduce the power consumption of a LCD system via software control.

HX8379-C also supports several interface modes, including MIPI DPI and DBI Type C, I2C , SPI 16bits interface mode, MIPI DSI (Display Serial Interface) interface mode, . The interface mode is selected by the external hardware pins IM[3:0].

HX8379-C is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and other mobile devices.

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2. Features

2.1 Display

- Single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display
- Resolution:
  - 480RGB x 320/360/640/720/800/864/1024/(320+8*NL)
  NL is internal register setting, and the maximum Gate number is 1024.
  - 480RGB x 854
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit ; 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit; 6(R):6(G):6(B))
    - 65k colours (16-bit; 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 1441 source channel outputs
- Gate driver control signal for GIP
- Supports 1-dot / 2-dot / 3-dot /4-dot/ 8-dot / Column / Zig-Zag / Zig-Zag-2 inversion
- Output voltage level
  - VSP is 4.5V ~ 6.5V
  - VSN is -4.5V ~ -6.5V
  - Positive source output high voltage level: VSPR is 3.0V ~ 6.3V
  - Negative source output high voltage level: VSNR is -3.0V ~ -6.3V
  - Positive gate driver output voltage level: VGH is 6.4V ~ 18V
  - Positive gate driver output voltage level: VGH_REG is 6.4V ~ 18V
  - Negative gate driver output voltage level: VGL is -7V ~ -15V
  - Negative gate driver output voltage level: VGL_REG is -7V ~ -15V
  - Gate driver output voltage range: |VGH| + |VGL| < 30V
  - Common electrode voltage level: VCOM is -0.3V ~ -4V, a step=10mV

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2.3 Display / control interface

- Display interface types supported
  - MIPI-DBI mode
    - MIPI-DBI Type C (Serial data transfer interface) interface
  - MIPI-DPI mode
    - 16 bit/pixel R(5), G(6), B(5)
    - 18 bit/pixel R(6), G(6), B(6)
    - 24 bit/pixel R(8), G(8), B(8)
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.10
    - Support D-PHY version 1.10
  - I2C (Inter-Integrated Circuit) interface
  - SPI 16bits interface

2.4 Input power

- I/O and interface power supply: VDD1 is 1.65V ~ 3.3V
- Analog power supply: VDD2 is 2.5V ~ 3.6V
- Logic power supply: VDD3 is 2.5V ~ 3.6V
- High speed interface power supply HS_VCC is 1.65V ~ 3.3V
- OTP programming voltage: OTP_PWR is 8.25V ± 0.2V.

2.5 Miscellaneous

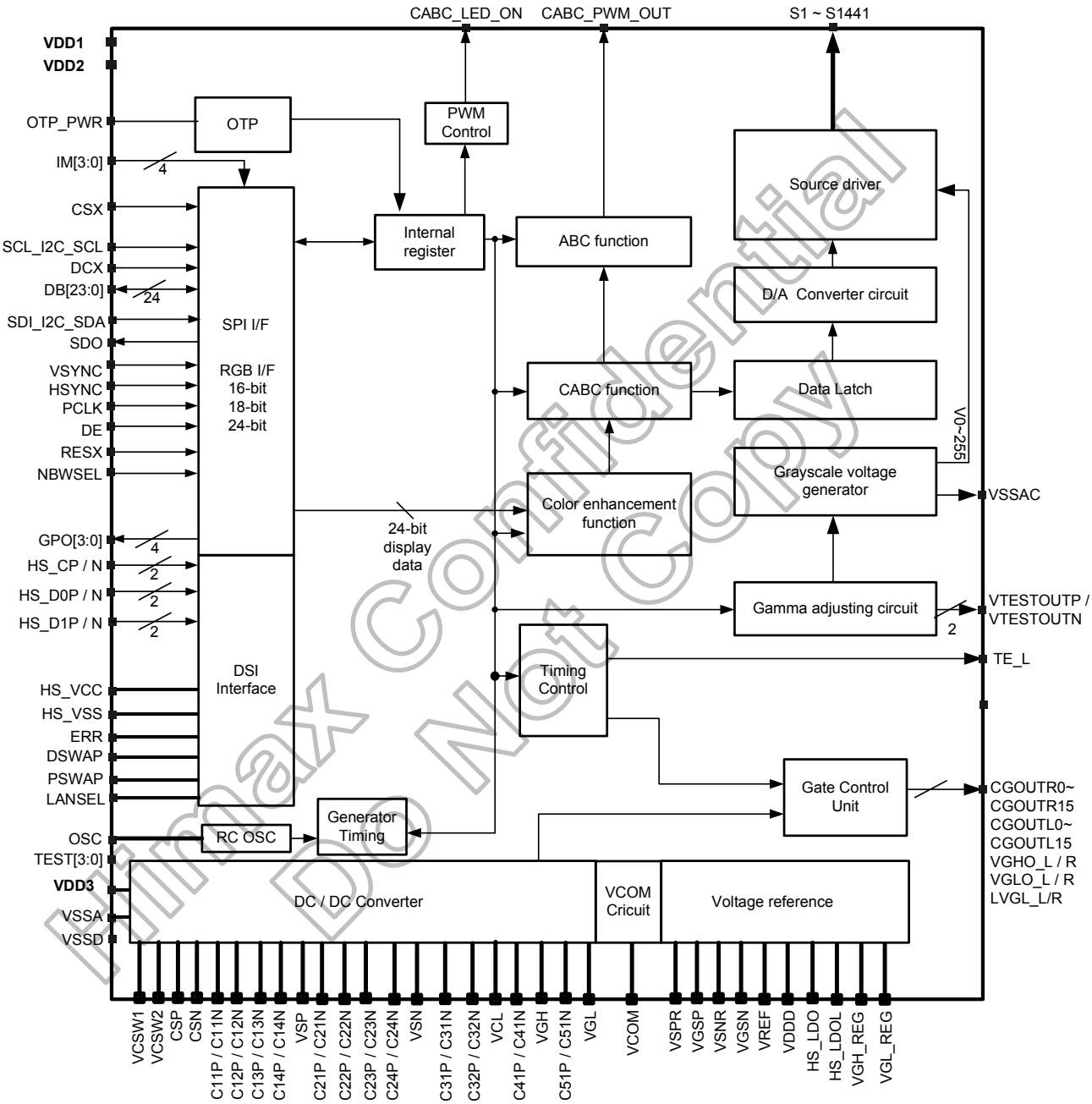
- Software programmable color depth mode
- Low power consumption, suitable for battery operated systems
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Temperature range: -40 to +85 ℃
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM setting ,ID setting
- Support Content Adaptive Brightness Control(CABC) function
- Support 3-Gamma DGC (Digital Gamma Correction) function
- Support Image Enhancement function (Color Saturation / Brightness / Sharpness)
- GPO (General Purpose Output)X 4
- Support Embedded Temperature Sensor for GIP optimized setting

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3. Device Overview

3.1 Block diagram



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3.2 Pin description

<table>
<tr><th colspan="5">Host interface pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin no.</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM [3 : 0]</td><td>I</td><td>4</td><td>VSSD / VDD1</td><td>Select the interface mode as listed below:
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>DPI/DBI TYPE-C Option 1</td><td>SDI/SDO, DB23-DB0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>DPI/DBI TYPE-C Option 3</td><td>SDI/SDO, DB23-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>16bits SPI interface, rising trigger</td><td>SDI/SDO, DB23-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>16bits SPI interface, falling trigger</td><td>SDI/SDO, DB23-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>I2C interface</td><td>I2C_SDA / I2C_SCL, DB23-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>MIPI DSI</td><td>HS_CLK_P/N, HS_D0P/N, HS_D1P/N,</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>MIPI DSI +DBI Type-C Option 1</td><td>I2C_SDA / I2C_SCL, HS_CLK_P/N, HS_D0P/N, HS_D1P/N,</td></tr>
<tr><td colspan="4">Other setting</td><td>Not used</td><td>-</td></tr>
</table>
Must be connected to VSSD or VDD1</td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If this pin is not used, connect it to VDD1 or VSSD.</td></tr>
<tr><td>DCX</td><td>I</td><td>1</td><td>MPU</td><td>Data / Command Selection pin
If this pin is not used, please connect it to VSSD or VDD1.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied
(Must be connected to VSSD or VDD1)</td></tr>
<tr><td>SCL_I2C_SCL</td><td>I</td><td>1</td><td>MPU</td><td>SPI:DBI Type-C Option 1/3: it servers as SCL (Serial Clock)
I2C interface : serial clock input.
If not use, let it open or connected to VDD1 or VSSD.</td></tr>
<tr><td>SDI_I2C_SDA</td><td>I/O</td><td>1</td><td>MPU</td><td>SPI:Serial data input pin.
I2C interface : serial data in/out.
If not used, let it open or VSSD.</td></tr>
<tr><td>SDO</td><td>O</td><td>1</td><td>MPU</td><td>Serial data output pin. If not used, let it open.</td></tr>
<tr><td>DB23~0</td><td>I/O</td><td>24</td><td>MPU</td><td>DPI type interface, refer to section 4.1. 4
<table>
<tr><th>Data bus</th></tr>
<tr><td>16-bit bus</td></tr>
<tr><td>18-bit bus</td></tr>
<tr><td>24-bit bus</td></tr>
</table>
Let the unused pins open for each mode or VSSD.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>1</td><td>MPU</td><td>Select the voltage sequence of V0 ~ V255
<table>
<tr><th>NBWSEL</th><th>V0 ~ V255 voltage</th></tr>
<tr><td>0</td><td>V0 > V1 > … > V254 > V255 (Normally White)</td></tr>
<tr><td>1</td><td>V0 < V1 < … < V254 < V255 (Normally Black)</td></tr>
</table></td></tr>
<tr><td>I2C_SA0</td><td>I</td><td>1</td><td>MPU</td><td>I2C slave address select.
<table>
<tr><th>I2C_SA0</th><th>Slave Address</th></tr>
<tr><td>0</td><td>1001100</td></tr>
<tr><td>1</td><td>1001101</td></tr>
</table></td></tr>
<tr><td>GPO[3:0]</td><td>O</td><td>4</td><td>-</td><td>General purpose output pins to control the external circuits.
Output level is VSSD to VDD1.
If not used, let it open</td></tr>
</table>

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Clock input and RGB interface				
HSYNC	**I**	**1**	**MPU**	Line synchronizing signal. If this pin is not used, connect it to VSSD or VDD1.
DE	**I**	**1**	**MPU**	Data enable signal. If this pin is not used, connect it to VSSD or VDD1.
VSYNC	**I**	**1**	**MPU**	Frame synchronizing signal. If this pin is not used, connect it to VSSD or VDD1.
PCLK	**I**	**1**	**MPU**	Dot clock signal. If this pin is not used, connect it to VSSD or VDD1.
Source driver output pins				
S1 to S1440	**O**	**1440**	**LCD**	Output voltages applied to the liquid crystal.
SDUM[3:0]	**O**	**4**	**LCD**	Dummy Source for Zig-Zag inversion. If not used, let it open
TE_L	**O**	**1**	**MPU**	Tearing Effect pin.
GIP control signal and bias voltage				
CGOUT(0~15)_R/L	**O**	**32/32**	**LCD**	Gate control signals for GIP panel. Output level is VGLO to VGHO
VGHO	**O**	**24**	**LCD**	High voltage level for gate control signals and gate circuits on panel.
VGLO	**O**	**34**	**LCD**	Low voltage level for gate control signals and gate circuits on panel. Voltage source can be chosen from VGL or VGL_REG.
LVGL_R/L	**O**	**3/3**	**LCD**	Low voltage level for gate control signals and gate circuits on panel. Voltage source can be chosen from VGL or VGL_REG. If not used, let it open
Power supply pins				
VDD1	**I**	**8**	**Power supply**	A power supply for the I/O circuit. VDD1=1.65 ~ 3.3V
VDD2	**I**	**4**	**Power supply**	A power supply for the analog power. VDD2=2.5V to 3.6V VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.
VDD3	**I**	**15**	**Power supply**	A power supply for the logic power, DC/DC converter VDD3=2.5V to 3.6V.
VDD3_P	**I**	**11**	**Power supply**	A power supply for charge-pump circuit. Please connect VDD3_P with VDD3 on FPC.
VSSA	**P**	**32**	**Power supply**	Analog ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSAC	**P**	**4**	**Power supply**	Analog ground. Must connect to VSSA on the FPC.
VSSD	**P**	**17**	**Power supply**	Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSSD_P	**P**	**15**	**Power supply**	Ground for charge-pump circuit. Please connect VSSD_P with VSSD on FPC.
OTP_PWR	**I**	**5**	**Power supply**	External high voltage pin used in OTP mode and operates at 8.25V. If not used, let it open.
Output pins of power and reference voltage				
VREF	**O**	**4**	**Stabilizing capacitor**	Reference voltage from internal band gap circuit. The tolerance of VREF voltage is ± 3 %. Connect to a stabilizing capacitor between VSSD and VREF.
VDDD	**O**	**10**	**Stabilizing capacitor**	Internal logic voltage output. (1.5V) Connect to a stabilizing capacitor between VSSD and VDDD.
VSP	**I/O**	**8**	**Stabilizing capacitor**	Voltage from the step-up circuit or external Power IC : HX5186-A/B/C (4.5V to 6.5V). it is generated from VDD3
VSN	**I/O**	**11**	**Stabilizing capacitor**	Voltage from the step-up circuit or external Power IC : HX5186-A/B/C (-4.5V to -6.5V). It is generated from VDD3.
VCL	**O**	**17**	**Stabilizing capacitor**	Voltage from the step-up circuit (-2.5V ~ -3.1V). It is generated from VDD3.
VSPR	**O**	**1**	**-**	Output regulated positive voltage for positive gamma high voltage. (3.0V to VSP – 0.5)
VSNR	**O**	**2**	**-**	Output regulated negative voltage for negative gamma high voltage. (-3.0V to VSN + 0.5)
VGH	**O**	**2**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.
VGH_REG	**O**	**12**	**Stabilizing capacitor**	Output regulated voltage for panel voltage. It is generated from VGH. Connect to a stabilizing capacitor between VSSA and VGH_REG. If not used, let it open.
VGL	**O**	**6**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a Schottkey barrier diode between VSSA and VGL.

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<table>
<tr><td>VGL_REG</td><td>O</td><td>4</td><td>Stabilizing capacitor</td><td>Output regulated voltage for panel voltage. It is generated from VGL.
Connect to a stabilizing capacitor between VSSA and VGL_REG.
If not used, let it open.</td></tr>
<tr><td>VCOM</td><td>O</td><td>10</td><td>Stabilizing capacitor</td><td>The power for common voltage in DC com driving.
(-0.3V to -4V)
Connected a stabilizing capacitor 2.2uF to VSSA.</td></tr>
<tr><td colspan="5">DC/DC pumping</td></tr>
<tr><td>EXT_VSPN</td><td>I</td><td>1</td><td>VDD1 / VSSD</td><td>External/internal power mode selection.
1: External power mode.(external VSP,VSN)
0: Internal power mode. (Refer to PCCS[1:0] for Internal Charge Pump/HX5186 mode selection.)
Must be connected to VSSD or VDD1</td></tr>
<tr><td>C11P, C11N
C12P, C12N
C13P, C13N
C14P,C14N</td><td>I/O</td><td>24</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSP voltage.</td></tr>
<tr><td>C21P, C21N
C22P, C22N
C23P, C23N
C24P,C24N</td><td>I/O</td><td>24</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSN voltage.</td></tr>
<tr><td>C31P, C31N
C32P, C32N</td><td>I/O</td><td>12</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VCL voltage.</td></tr>
<tr><td>C41P, C41N</td><td>I/O</td><td>4</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.</td></tr>
<tr><td>C51P, C51N</td><td>I/O</td><td>4</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.</td></tr>
<tr><td>VCSW1, VCSW2</td><td>O</td><td>4</td><td>-</td><td>VCSW1 and VCSW2 connect with external power IC : HX5186-A/B/C to generate VSP, VSN.</td></tr>
<tr><td colspan="5">CABC & ABC</td></tr>
<tr><td>CABC_PWM_OUT</td><td>O</td><td>1</td><td>LED Driver</td><td>PWM output pin of Backlight control. If use CABC function, the pin can connect to external LED driver IC.
If not used, let it open.</td></tr>
<tr><td>CABC_LED_EN</td><td>O</td><td>1</td><td>LED Driver</td><td>Enable signal of Backlight LED driver(Active high).
If not used, let it open.</td></tr>
<tr><td colspan="5">High speed interface parts</td></tr>
<tr><td>DSWAP,
PSWAP</td><td>I</td><td>2</td><td>MPU</td><td>MIPI DSI : DSWAP select the data output pin sequence.
PSWAP select the signal polarity.
<table>
<tr><th>DSWAP</th><th>PSWAP</th><th>HS_ D0P</th><th>HS_ D0N</th><th>HS_ CP</th><th>HS_ CN</th><th>HS_ D1P</th><th>HS_ D1N</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>Data Lane 0+</td><td>Data Lane 0-</td><td>Clock +</td><td>Clock -</td><td>Data Lane 1+</td><td>Data Lane 1-</td></tr>
<tr><td>1</td><td>Data Lane 0-</td><td>Data Lane 0+</td><td>Clock -</td><td>Clock +</td><td>Data Lane 1-</td><td>Data Lane 1+</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Data Lane 1+</td><td>Data Lane 1-</td><td>Clock +</td><td>Clock -</td><td>Data Lane 0+</td><td>Data Lane 0-</td></tr>
<tr><td>1</td><td>Data Lane 1-</td><td>Data Lane 1+</td><td>Clock -</td><td>Clock +</td><td>Data Lane 0-</td><td>Data Lane 0+</td></tr>
</table>
if not used , Please connected to VSSD</td></tr>
<tr><td>LANSEL</td><td>I</td><td>1</td><td>MPU</td><td>Select number of data lanes for MIPI DSI
Low : 1 data lane.
(HS_D0P/N and HS_CP/N)
High : 2 data lanes.
(HS_D0P/N, HS_D1P/N and HS_CP/N)
If not used in other interface, Please connected to VSSD</td></tr>
<tr><td>HS_D0_P,
HS_D0_N</td><td>I/O</td><td>8</td><td>High Speed Interface Host</td><td>MIPI DSI : Data differential signal input pins. (Data lane 0)
If not used , Please connect to VSSD or open.</td></tr>
<tr><td>HS_CLK_P,
HS_CLK_N</td><td>I</td><td>8</td><td>High Speed Interface Host</td><td>MIPI DSI : Clock differential signal input pins.
If not used , Please connect to VSSD or open.</td></tr>
<tr><td>HS_D1_P,
HS_D1_N</td><td>I</td><td>8</td><td>High Speed Interface Host</td><td>MIPI DSI : Data differential signal input pins. (Data lane 1)
If not used , Please connect to VSSD or open.</td></tr>
<tr><td>ERR</td><td>O</td><td>1</td><td>-</td><td>CRC and ECC output pin for MIPI DSI.
If not used , Please leave this pin open</td></tr>
<tr><td>HS_VCC</td><td>P</td><td>5</td><td>Power Supply</td><td>Power supply for the MIPI DSI analog power.
MIPI DSI : HS_VCC=1.65V ~ 3.3V (Recommend to connect with VDD1)</td></tr>
</table>

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HS_VSS	**P**	**11**	**Ground**	MIPI DSI analogy ground. HS_VSS=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
HS_LDO	**O**	**3**	**Capacitor**	MIPI DSI regulator output pin. (1.5V) Connect to a stabilizing capacitor between HS_VSS and HS_LDO If not used, please open these pins.
Test Pins				
DUMMY_DIOPWR	**I**	**2**	**-**	No function, let it open or connect to VSSD or VDD1
DUMMY_DSTB_SEL	**I**	**1**	**-**	No function, let it open or connect to VSSD or VDD1
DUMMY_KBBC	**I**	**1**	**-**	No function, let it open or connect to VSSD or VDD1
DUMMY_RGBBP	**I**	**1**	**-**	No function, let it open or connect to VSSD or VDD1
DUMMY_VSEL	**-**	**1**	**-**	No function, let it open or connect to VSSD or VDD1
DUMMY_HS_LDOL	**O**	**3**	**Open**	No function, let it open or connect to VSSD or VDD1
OSC	**I**	**1**	**Open**	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.(weak pull low)
DUMMY_OSC	**I**	**1**	**Open**	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.(weak pull low)
DUMMY_TE_R	**O**	**1**	**Open**	No function, let it open or connect to VSSD or VDD1
TEST[3:0]	**I**	**4**	**Open**	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
VTESTOUTP	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	**O**	**2**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMY_VTESTOUTP	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMY_VTESTOUTN	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR_1A, DUMMYR_1B, DUMMYR_2A, DUMMYR_2B	**-**	**4**	**Open**	DUMMYR_1A and DUMMYR_1B are short in driver IC. DUMMYR_2A and DUMMYR_2B are short in driver IC. These pins are for bonding resistance measurement. These pins are Hi-Z in driver IC.
VGSW[3:0]	**-**	**4**	**Open**	Not used. Let it open or connect to VSSD or VDD1.
Dummy_LED_BOOST	**O**	**1**	**Open**	LED boost control signal at high brightness mode.(Active high) If not used, let it open (or connect to VDD1 or VSSD).
Dummy_IDLE_ON	**O**	**1**	**Open**	Digital LED control signal at IDLE mode. If not used, let it open (or connect to VSSD).
Dummy_LED1, Dummy_LED2	**O**	**2**	**Open**	Analog current output for LED control at IDLE mode. If not used, let it open.
DUMMY_CSP	**I**	**2**	**Open**	Not used. Let it open.
DUMMY_CSN	**I**	**2**	**Open**	Not used. Let it open.
DUMMY1-103	**-**	**103**	**Open**	Not used. Let it open.

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4. Interface

4.1 System interface

The HX8379-C supports MIPI interfaces: DBI (Display Bus Interface) serial interface Type-C, DPI (Display Pixel Interface), DSI (Display Serial Interface), where the interface mode can be selected by IM[3:0] pins setting as show in Table 4.1.

IM3	IM2	IM1	IM0	MPU interface mode	Display Data
1	0	1	0	DPI/DBI TYPE-C Option 1	DPI
1	0	0	1	DPI/DBI TYPE-C Option 3	DPI
0	0	1	1	16bits SPI interface, rising trigger	DPI
1	0	1	1	16bits SPI interface, falling trigger	DPI
0	1	0	0	I2C interface	DPI
0	1	0	1	MIPI DSI	DSI
1	1	1	1	MIPI DSI + Type-C Option 1	DSI
Other setting				Not used	-

Table 4.1: Interface Selection

Interface	RDX	SCL / I2C_SCL	DCX	D23–D0 or other input pin
DPI/DBI TYPE-C Option 1	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
DPI/DBI TYPE-C Option 3	Unused	SCL	DCX	DB23–DB0: 24-bit data bus SDI / SDO
16bits SPI interface, rising trigger	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
16bits SPI interface, falling trigger	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
I2C Interface	Unused	I2C_SCL	Unused	DB23–DB0: 24-bit data bus I2C_SDA, I2C_SCL
MIPI DSI	Unused	Unused	Unused	HS_CLK_P/N, HS_D0P/N, HS_D1P/N,
MIPI DSI + Type-C Option 1	Unused	SCL	Unused	HS_CLK_P/N, HS_D0P/N, HS_D1P/N, I2C_SDA, I2C_SCL

Table 4.2: Pin Connection based on Different Interface

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4.1.1 Serial data transfer interface (MIPI DBI TYPE-C)

The HX8379-C supports DBI Type C option 1 (3-wire) and option 3 (4-wire) serial data transfer interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set "1010" is select option1 (3-wire) serial bus. The IM[3:0] set "1001" is select option 3 (4-wire) serial buses.

The 3 wire serial bus uses: chip select line (CSX), serial data input (SDI), serial data output (SDO) and the serial transfer clock line (SCL).

The 4 wire serial bus uses: chip select line (CSX), data/command select (DCX), serial data input (SDI), serial data output (SDO) and the serial transfer clock line (SCL).

4.1.1.1 Serial data write mode

The 3-pin serial data packet contains a control bit DCX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal DCX is transferred by DCX pin. If DCX is low, the transmission byte is command byte. If DCX is high, the transmission byte is stored in to command register. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDI and SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

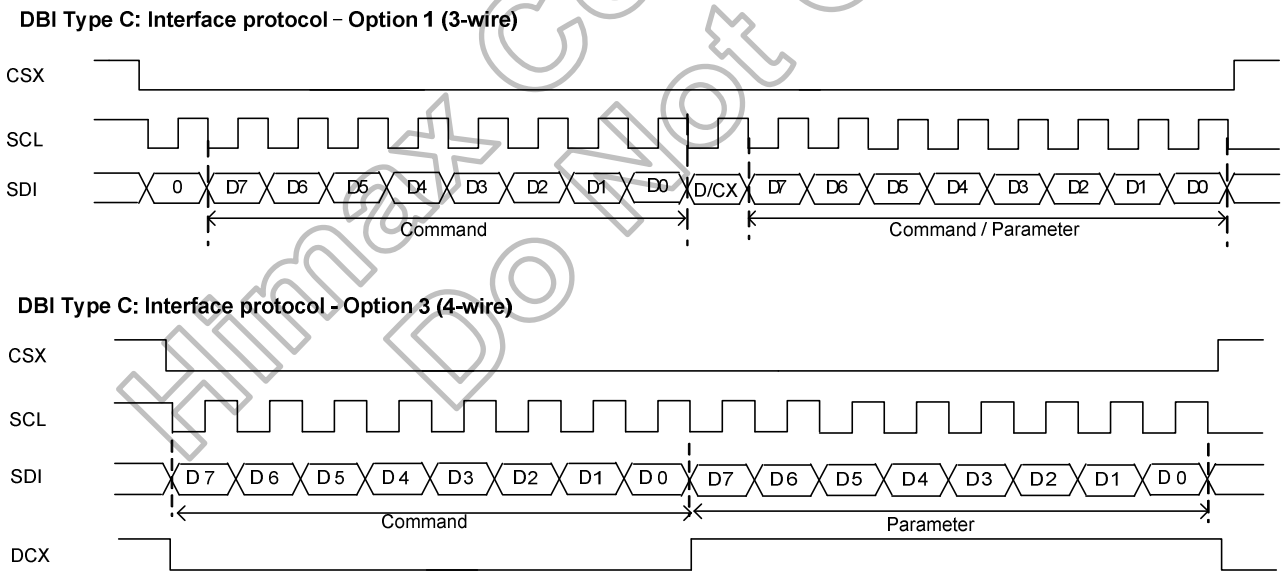


Figure 4.1: DBI Type C: Serial Interface Protocol 3-Wire/4-Wire, Write Mode

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4.1.1.2 Serial data read mode

In serial peripheral interface read operation, the host controller first has to send a command and then the following byte is transmitted to host controller in the SDI.

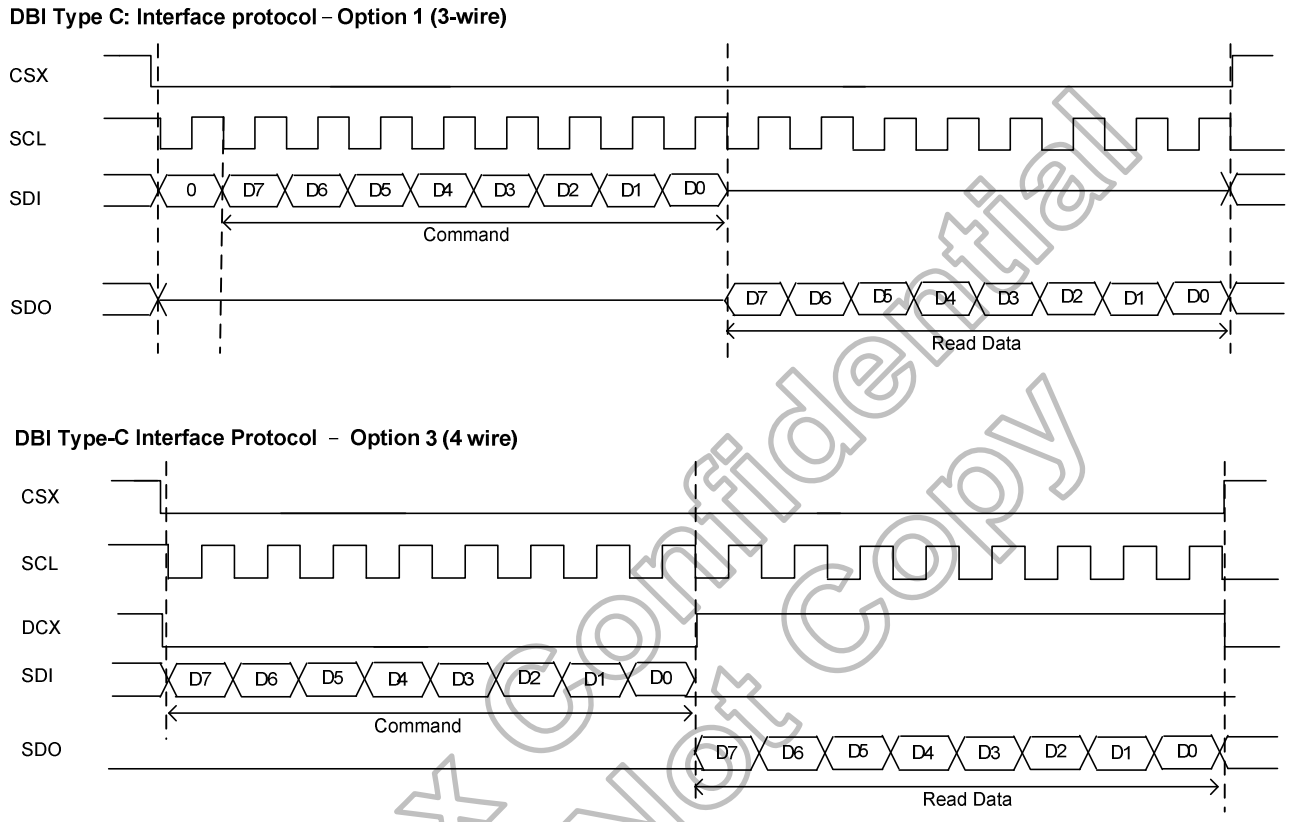


Figure 4.2: DBI Type C: Serial Interface Protocol 3-Wire/4-Wire Read Mode

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

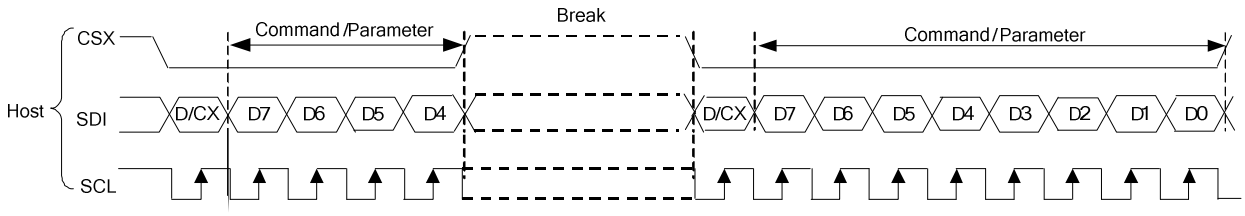


Figure 4.3: Display Module Data Transfer Recovery

If one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmit the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

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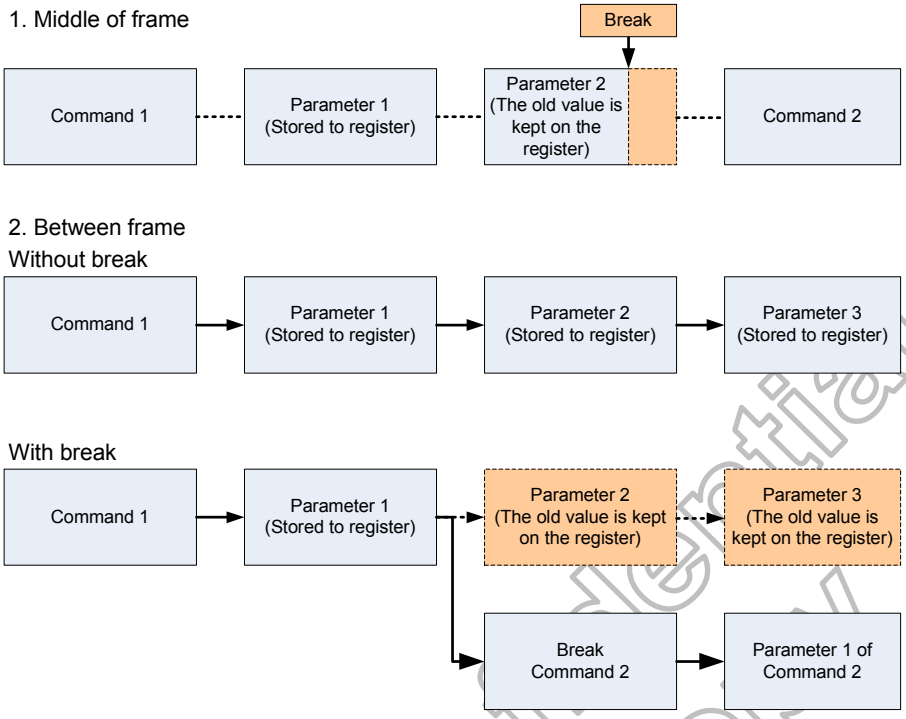


Figure 4.4: Break During Parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the write sequence at the point where the sequence was paused.

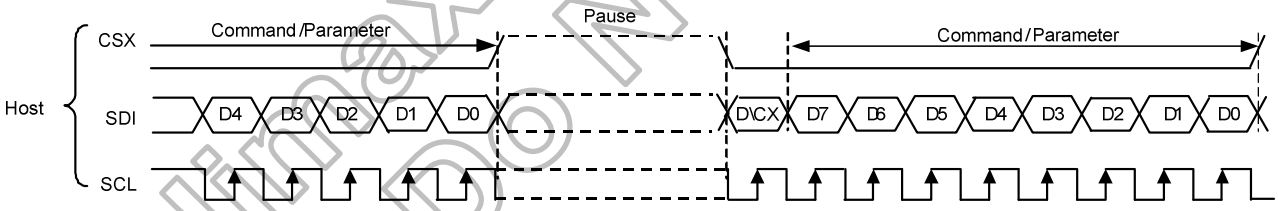


Figure 4.5: Display Module Data Transfer Pause

There are 4 cases where there is possible to see this kind of pause:

1. Command – Pause – Command

2. Command – Pause – Parameter

3. Parameter – Pause – Command

4. Parameter – Pause – Parameter

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4.1.2 Serial data transfer interface (16bits data transfer)

The HX8379-C supports SPI 16bits dat transfer interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set “0011” is select SPI 16bits, SCL rising trigger. The IM[3:0] set “1011” is select SPI 16bits, SCL falling trigger.

The SPI 16bits data transfer interface uses: chip select line (CSX), serial data input

4.1.2.1 Serial data 16bits write mode

The 3-pin serial data packet cont

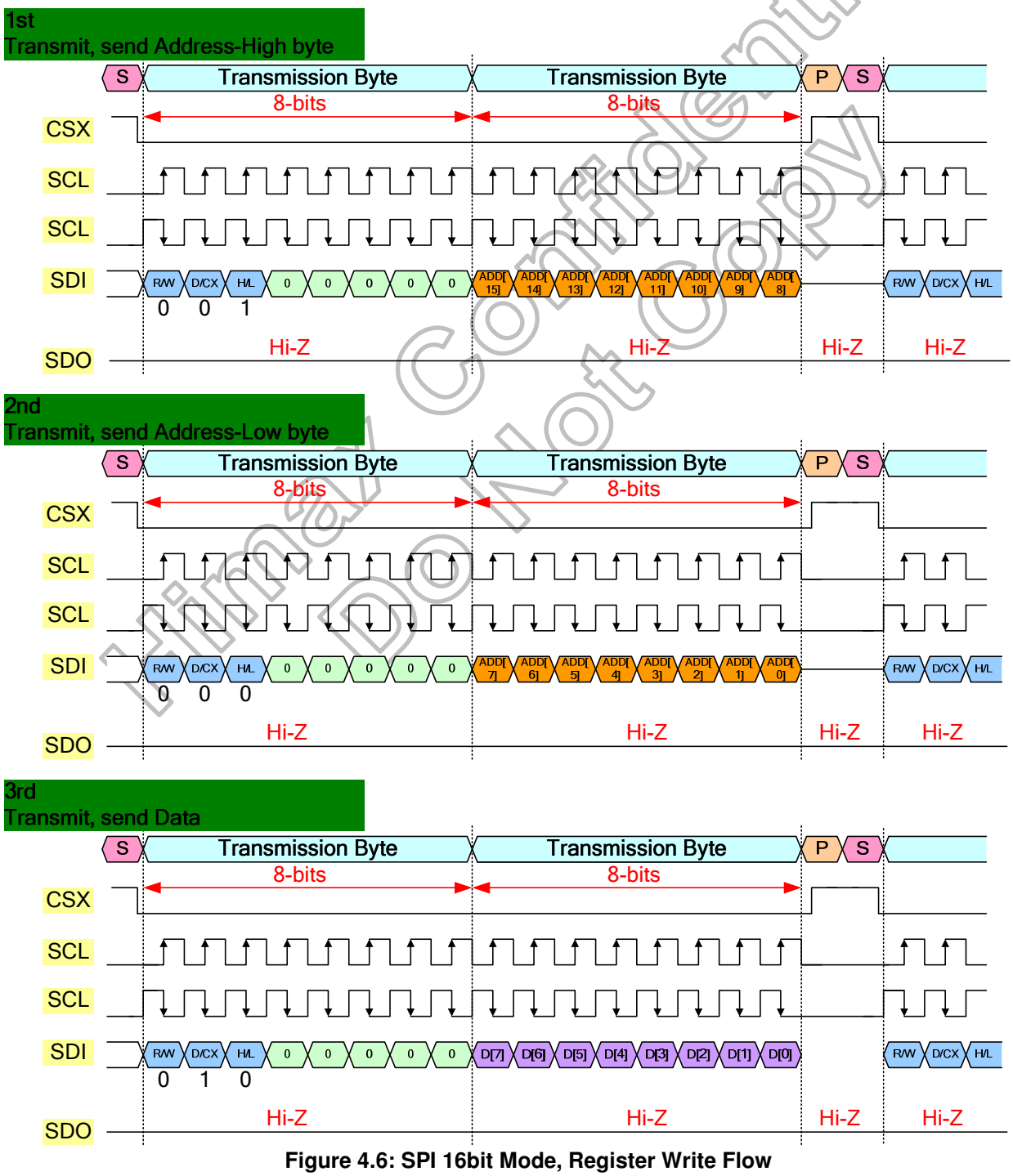


Figure 4.6: SPI 16bit Mode, Register Write Flow

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4.1.2.2 Serial data 16bits read mode

The 3-pin serial data packet cont

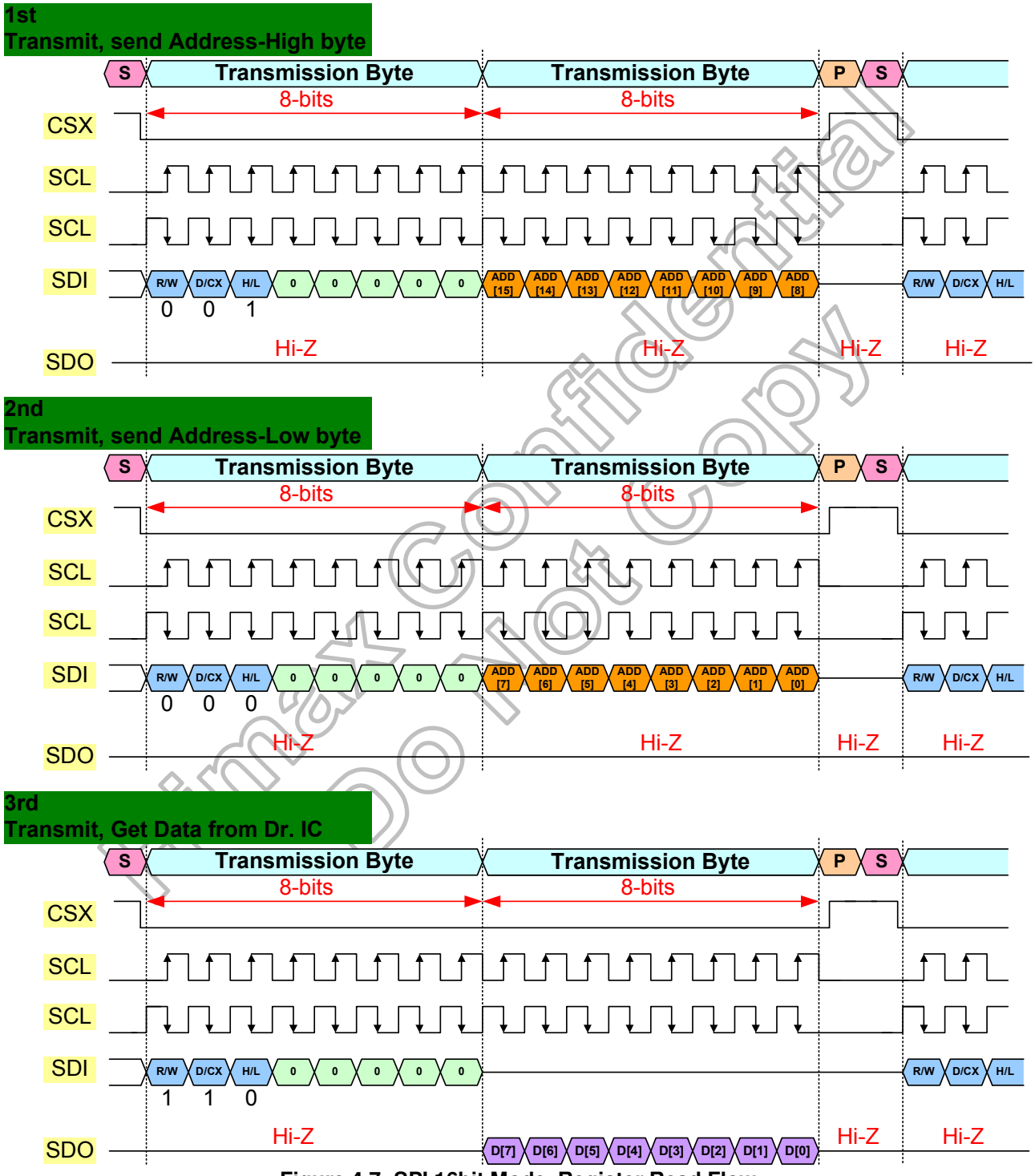


Figure 4.7: SPI 16bit Mode, Register Read Flow

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4.1.3 I2C interface

The HX8379-C supports I2C interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set “0100” is select I2C interface.

I2C interface 2 hardware pin – serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address — whether it’s a microcontroller, LCD driver, memory or keyboard interface — and can operate as either a transmitter or receiver, depending on the function of the device. Both SDA and SCL need to be connected to a positive supply voltage via a pull-up resistor. The pull-up resistor should be connected to VDDI. When the bus is free, both lines are HIGH.

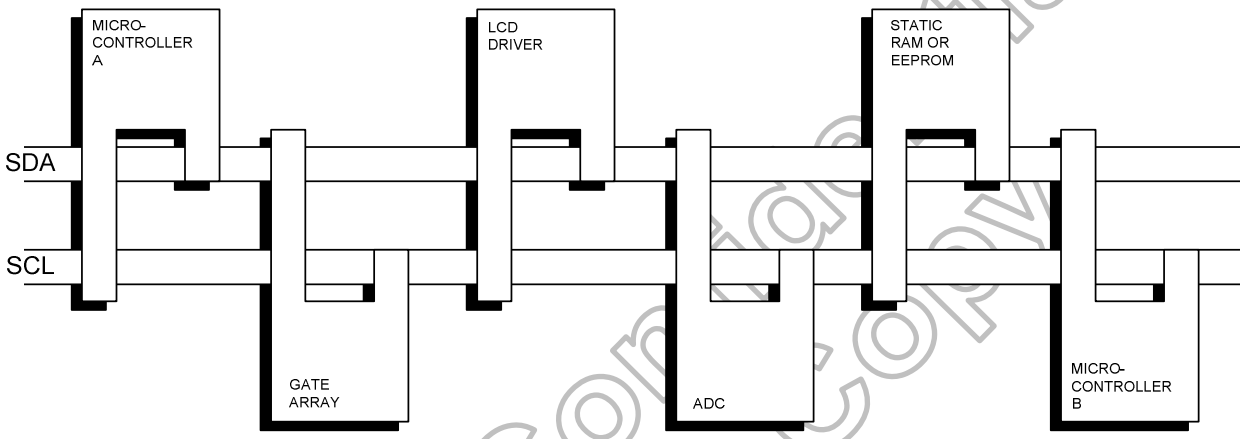


Figure 4.8 I2C Connection Diagram

4.1.3.1 I2C protocol

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

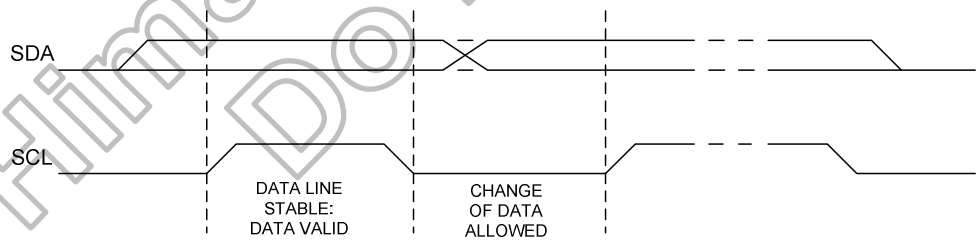


Figure 4.9: I^2C Signal Timing

Within the procedure of the I^2C-bus, unique situations arise which are defined as START and STOP conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The I^2C bus is considered to be busy after the START condition. The I^2C bus is considered to be free again a certain time after the STOP condition.

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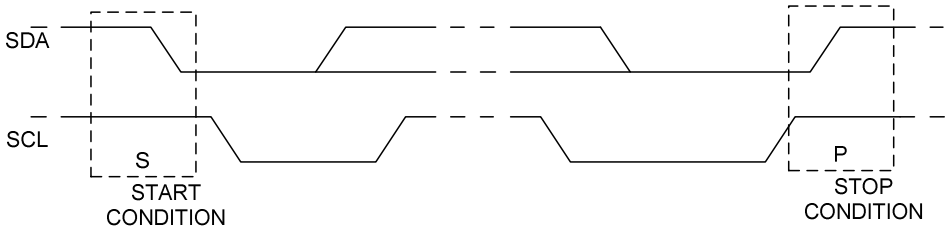


Figure 4.10: I2C Start/Stop

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

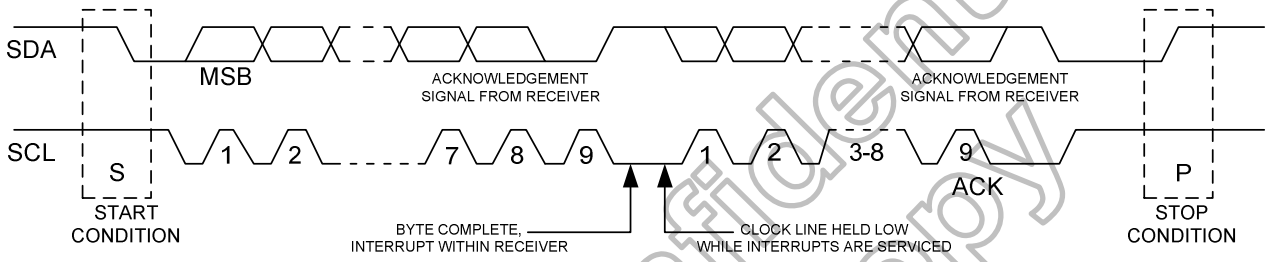


Figure 4.11: I2C Data Transfer

4.1.3.2 I2C slave address

HX8379-C has two slave address could be select by setting HW signal “I2C_SA0”. The slave address of I2C selected by I2C_SA0 line is defined a follow table.

I2C_SA0	Slave address (A6-A0)
0	1001100
1	1001101

Table 4.3: I2C Slave Address Table

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4.1.3.3 I2C interface write mode

HX8379-C support I2C to write data to register. The write flow is described as below

A. Send Start condition followed by I2C 6 bits slave address and 1 bit '0'(write flag)
B. Send High byte of 16bits address, then IC feedback Ack.
C. Send Low byte of 16bits address, then IC feedback Ack.
D. Send 8bits register data, MSB first , ADD[7] send first, the IC feedback Ack
E. Send Stop condition

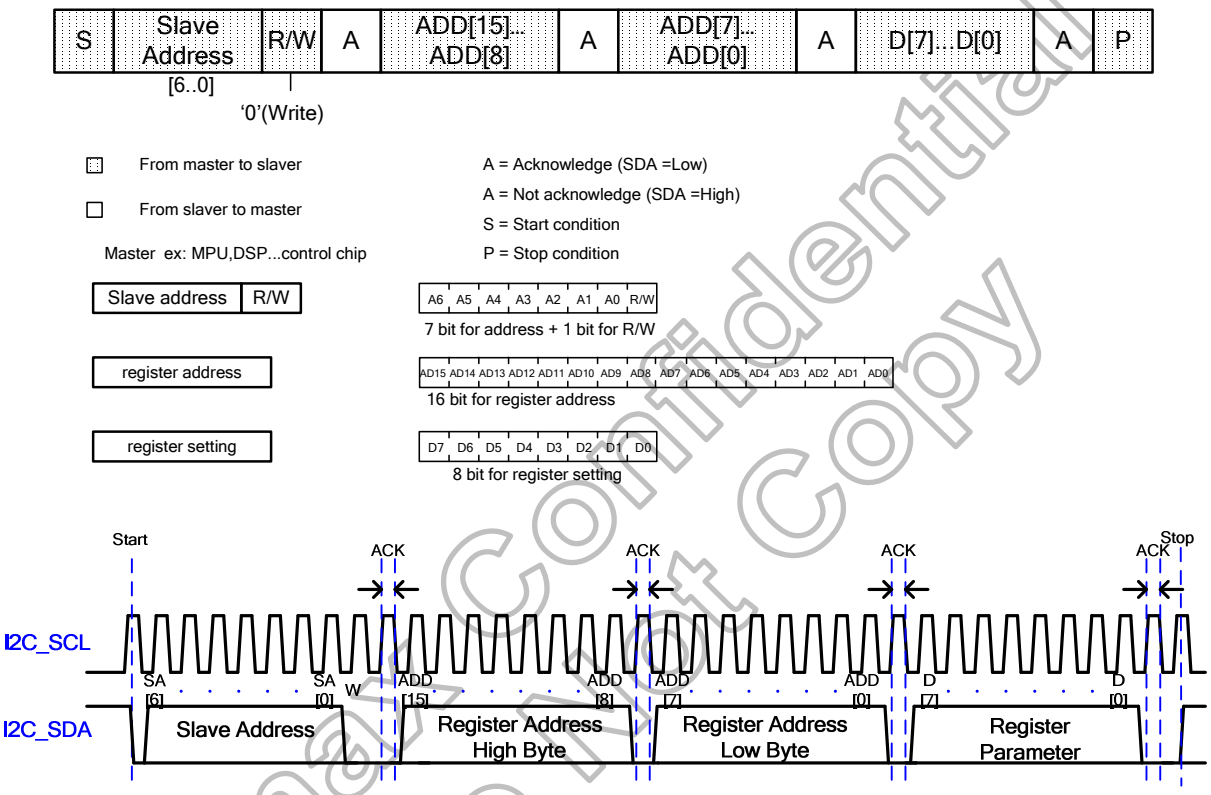


Figure 4.12: I2C Interface Register Write Flow

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4.1.3.4 I2C interface read mode

HX8379-C also supports I2C to read data from register. The write flow is described as below

A. Send Start condition followed by I2C 6 bits slave address and 1 bit '0'(write flag)
B. Send High byte of 16bits address, then IC feedback Ack.
C. Send Low byte of 16bits address, then IC feedback Ack.
D. Send restart condition followed by I2C 6 bits slave address and 1 bit '1'(read flag)
E. IC sends register data to baseband, and followed by a non-ack.
F. Send Stop condition

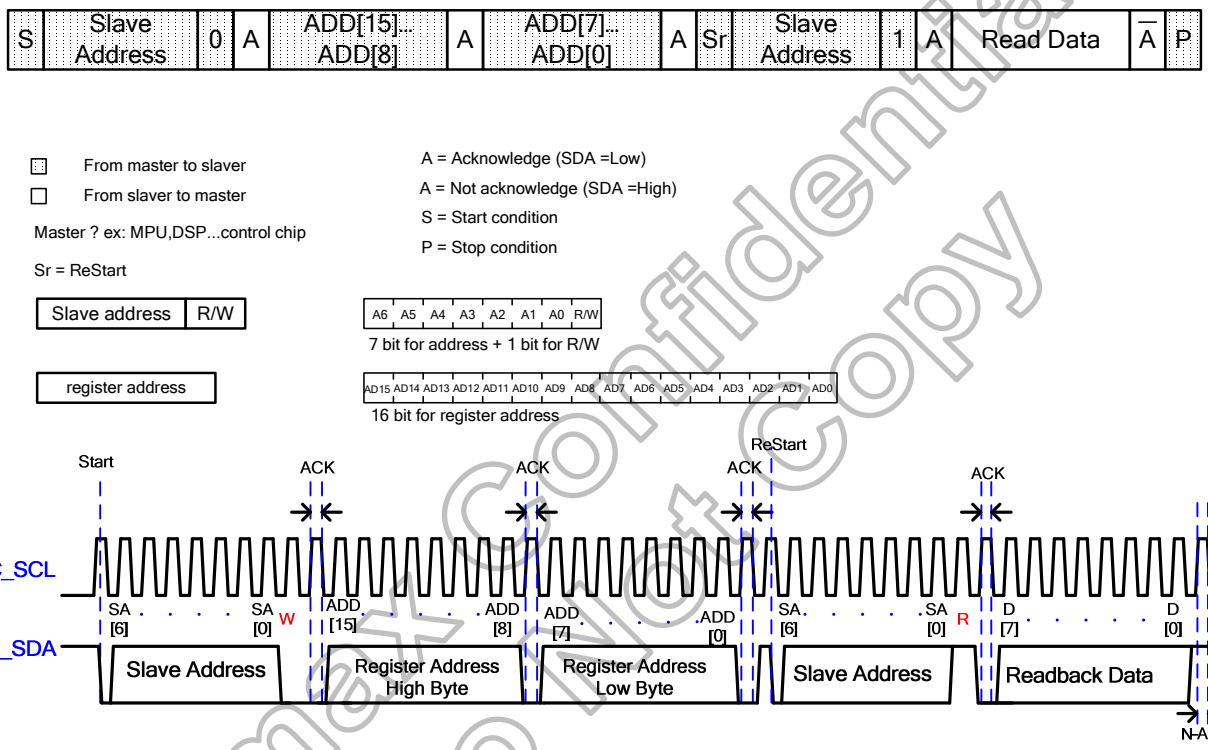


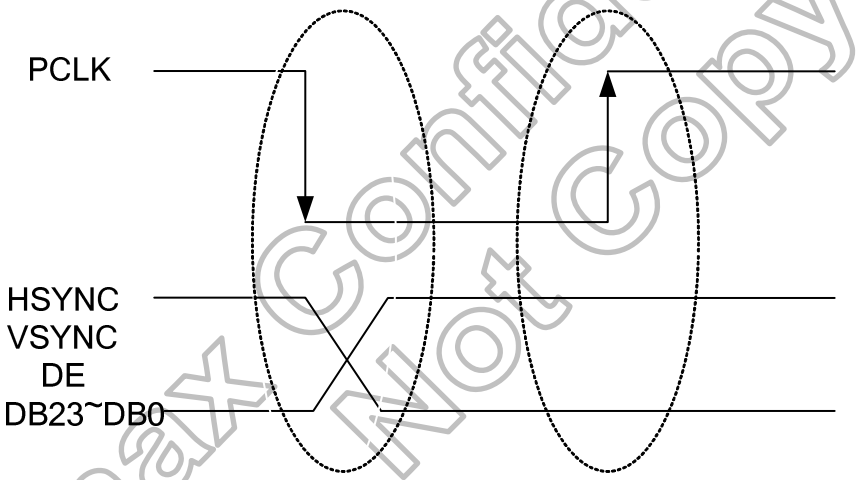
Figure 4.13: I2C Interface Register Read Flow

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4.1.4 MIPI DPI interface (Display Pixel Interface)

The HX8379-C uses 16 or 18-bit or 24-bit parallel DPI interface which includes: HSYNC, VSYNC, DE, PCLK, DB23~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB23~DB0– lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In– mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (“-“, “0”, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (“-“, “0”, low) active and its state is read to the display module by a rising edge of the PCLK- line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (“+”, “1”, high) active and its state is read to the display module by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).
Figure 4.14: PCLK Cycle

Register 3Ah	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode	
50h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0		Configuration 1
	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	16-bit	Configuration 2
	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x		Configuration 3
60h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0		Configuration 1
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	18-bit	Configuration 2
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit	-

Table 4.4: DPI Color Mapping

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4.1.4.1 General timing diagram

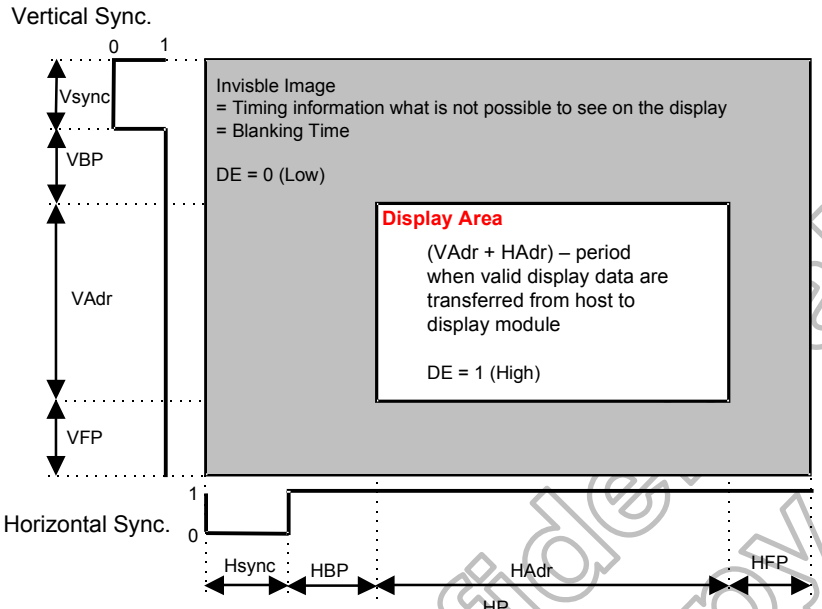


Figure 4.15: General Timing Diagram

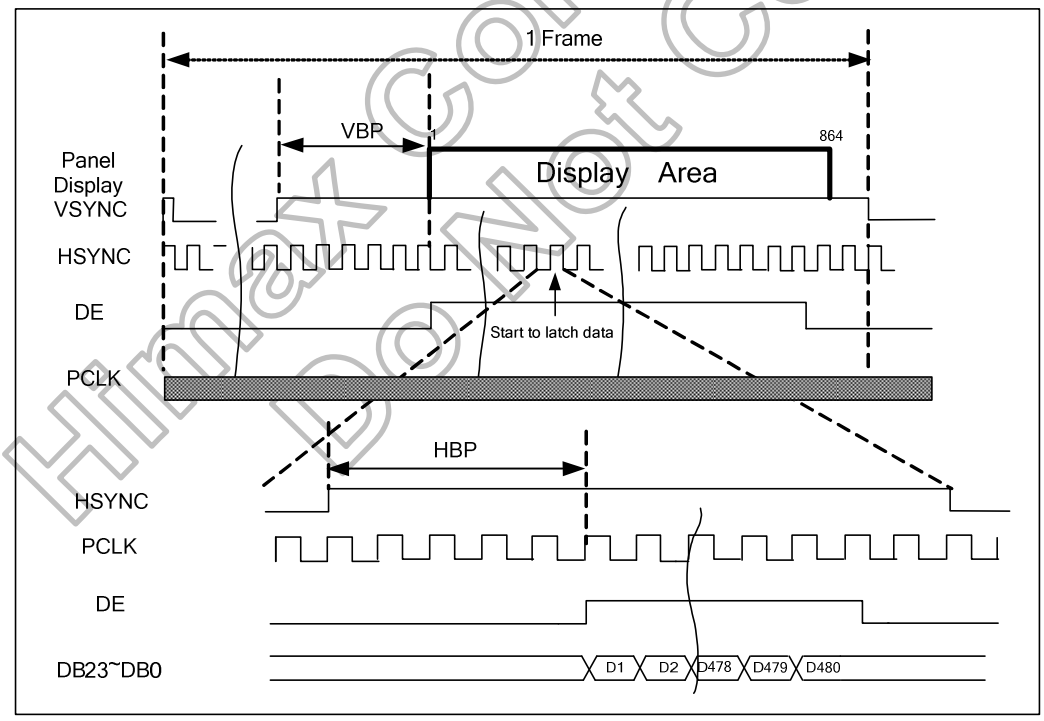


Figure 4.16: DPI (480RGB x 864) Timing Diagram

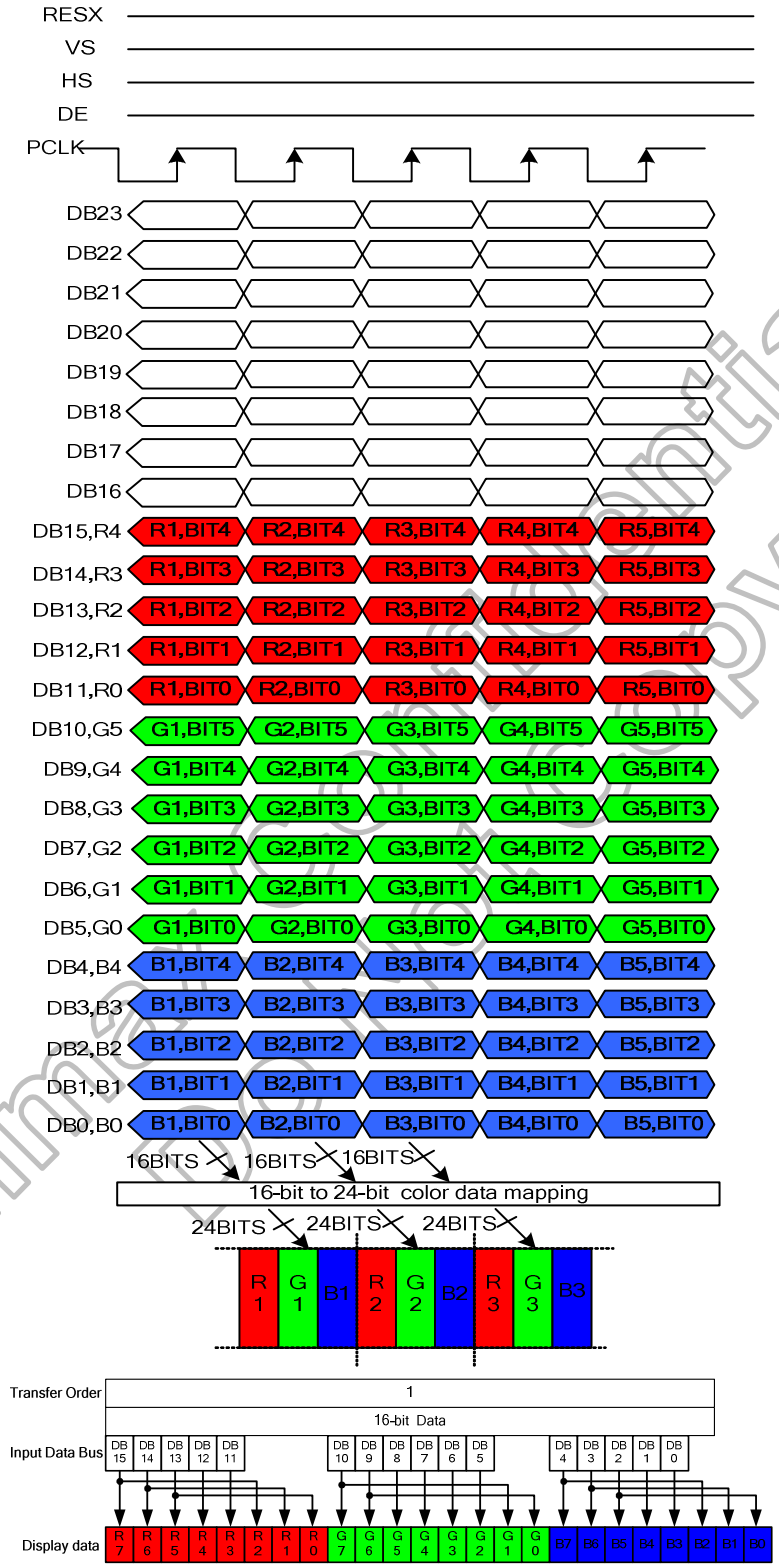
The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

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4.1.5 16-bit / pixel color order on the DPI I/F

4.1.5.116-bit / pixel color order on the DPI I/F – Configuration 1

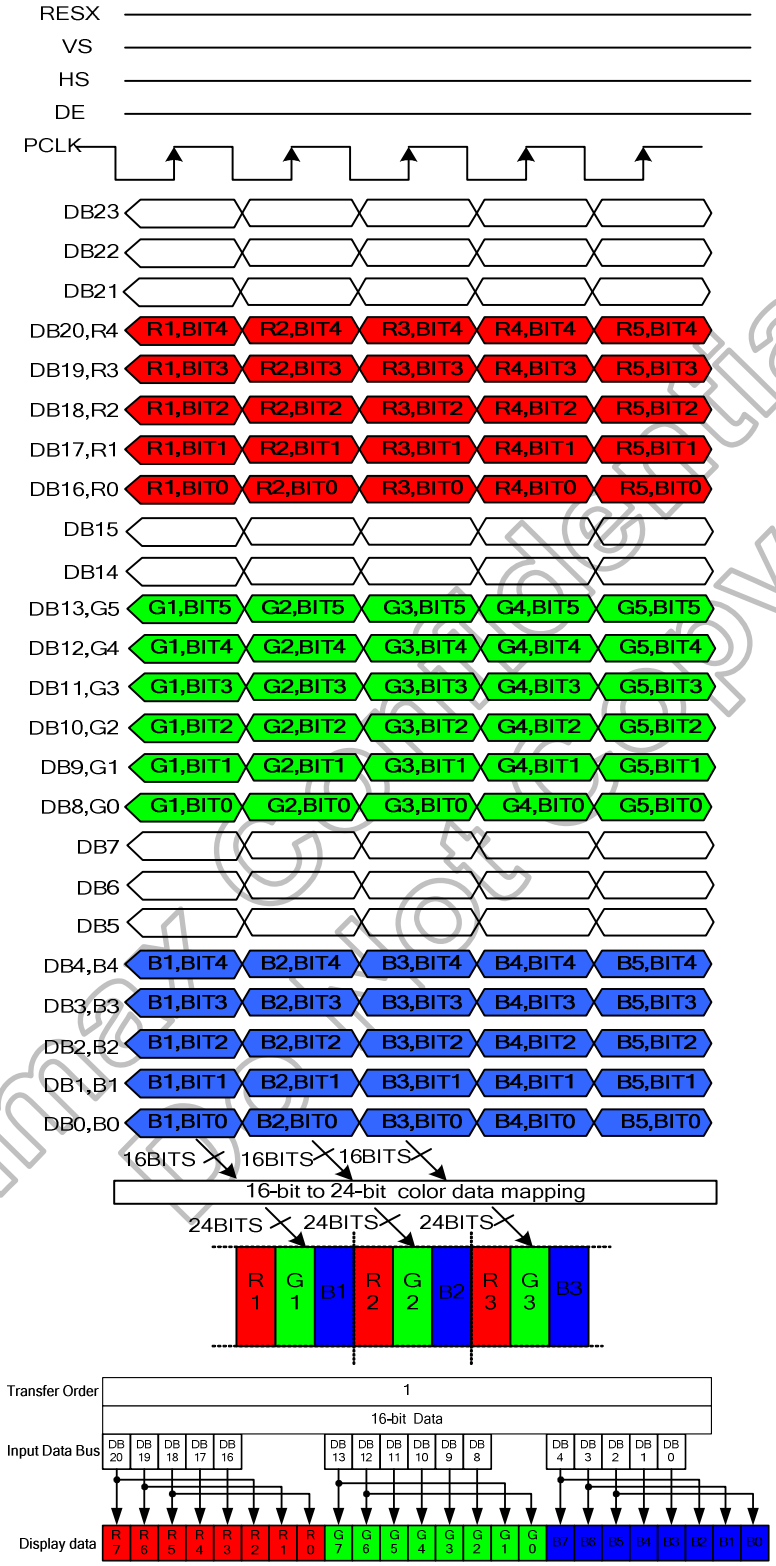


Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.17: 16-Bit / Pixel, 65K Colours Order on the DPI I/F– Configuration 1

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4.1.5.216-bit / pixel color order on the DPI I/F – Configuration 2

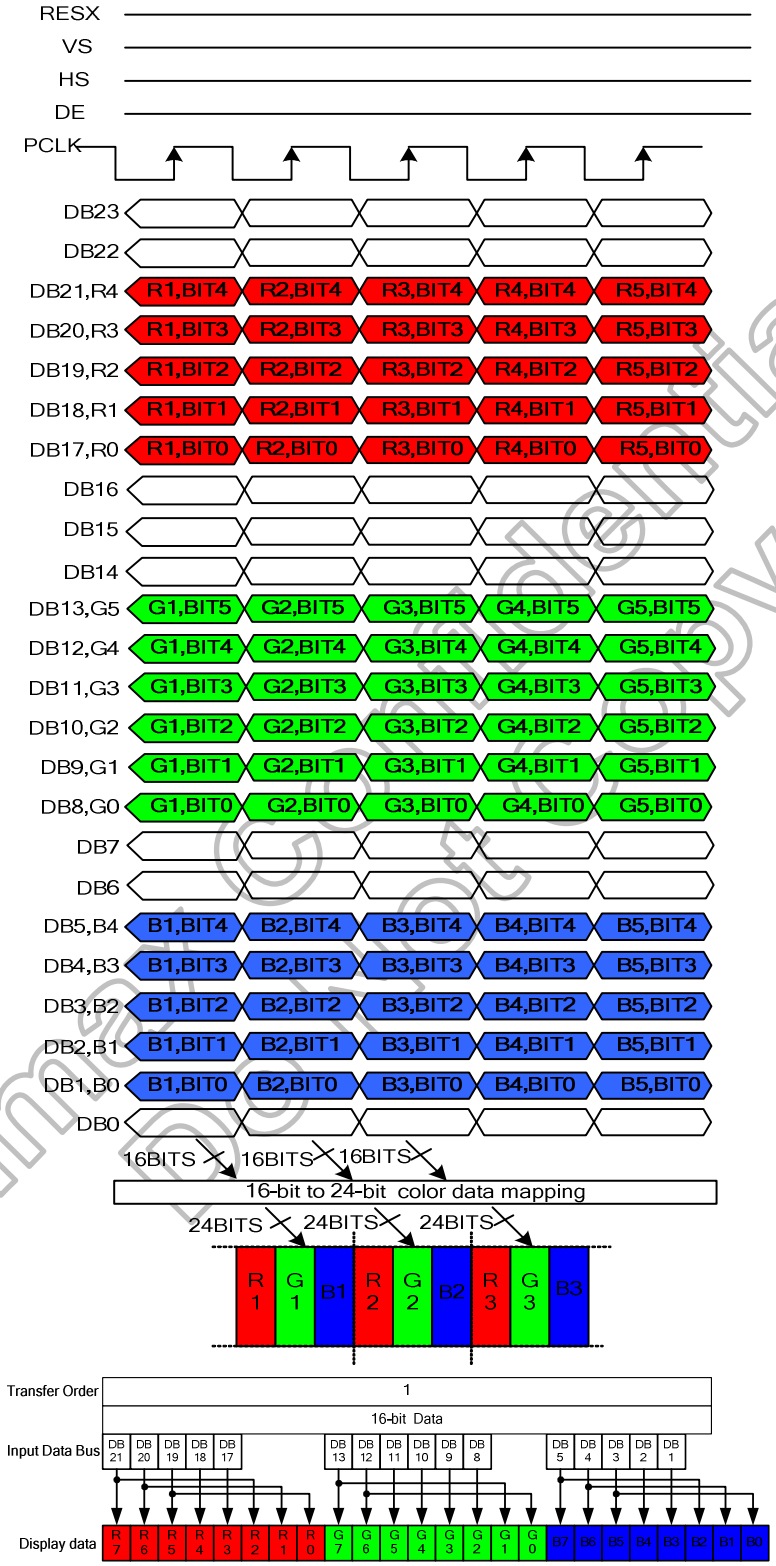


Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.18: 16-Bit / Pixel, 65K Colours order on the DPI I/F– Configuration 2

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4.1.5.3 16-bit / pixel color order on the DPI I/F – Configuration 3



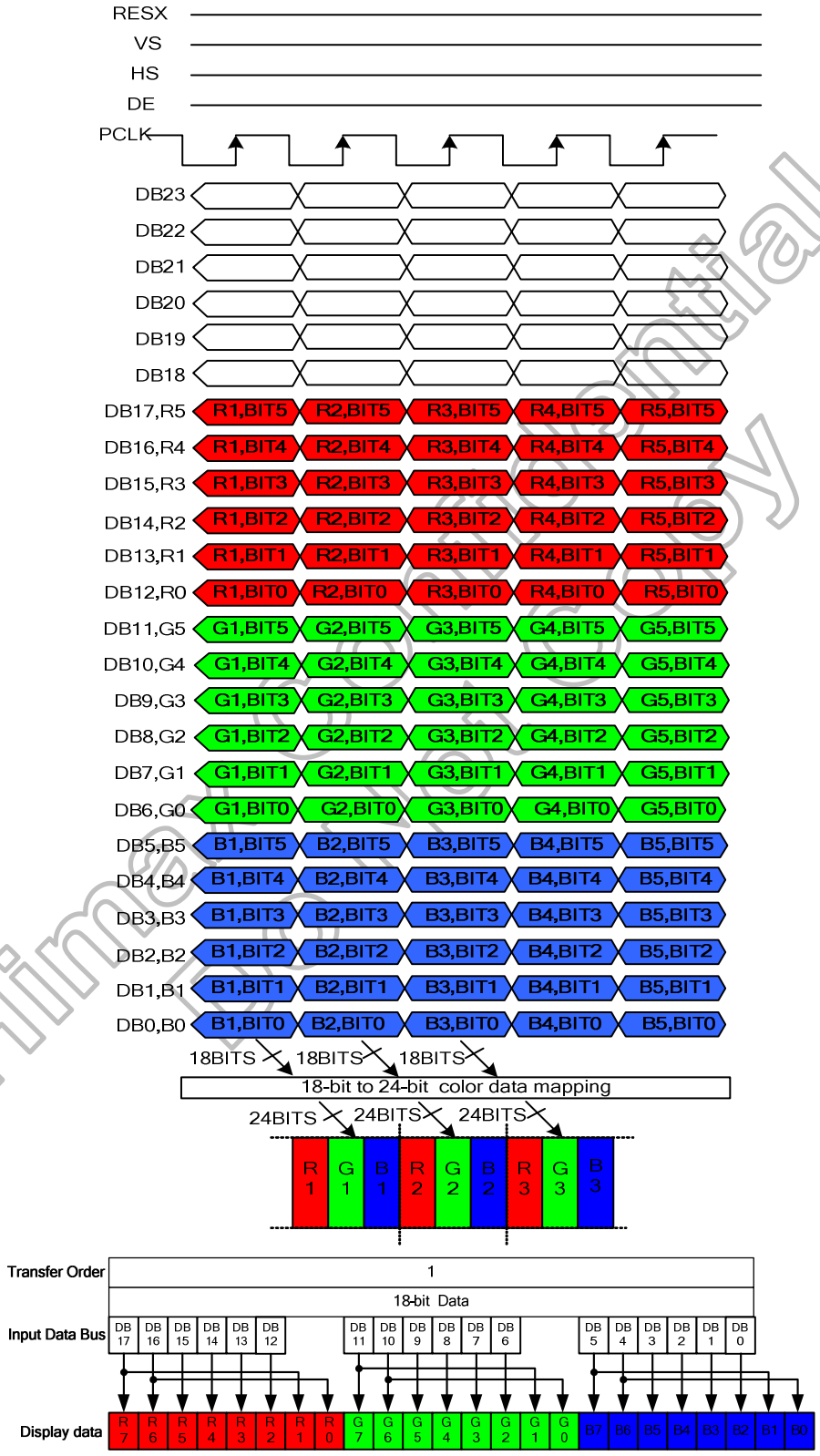
Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.19: 16-Bit / Pixel, 65K Colours Order on the DPI I/F– Configuration 3

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4.1.6 18-bit / pixel color order on the DPI I/F

4.1.6.118-bit / pixel color order on the DPI I/F – Configuration 1

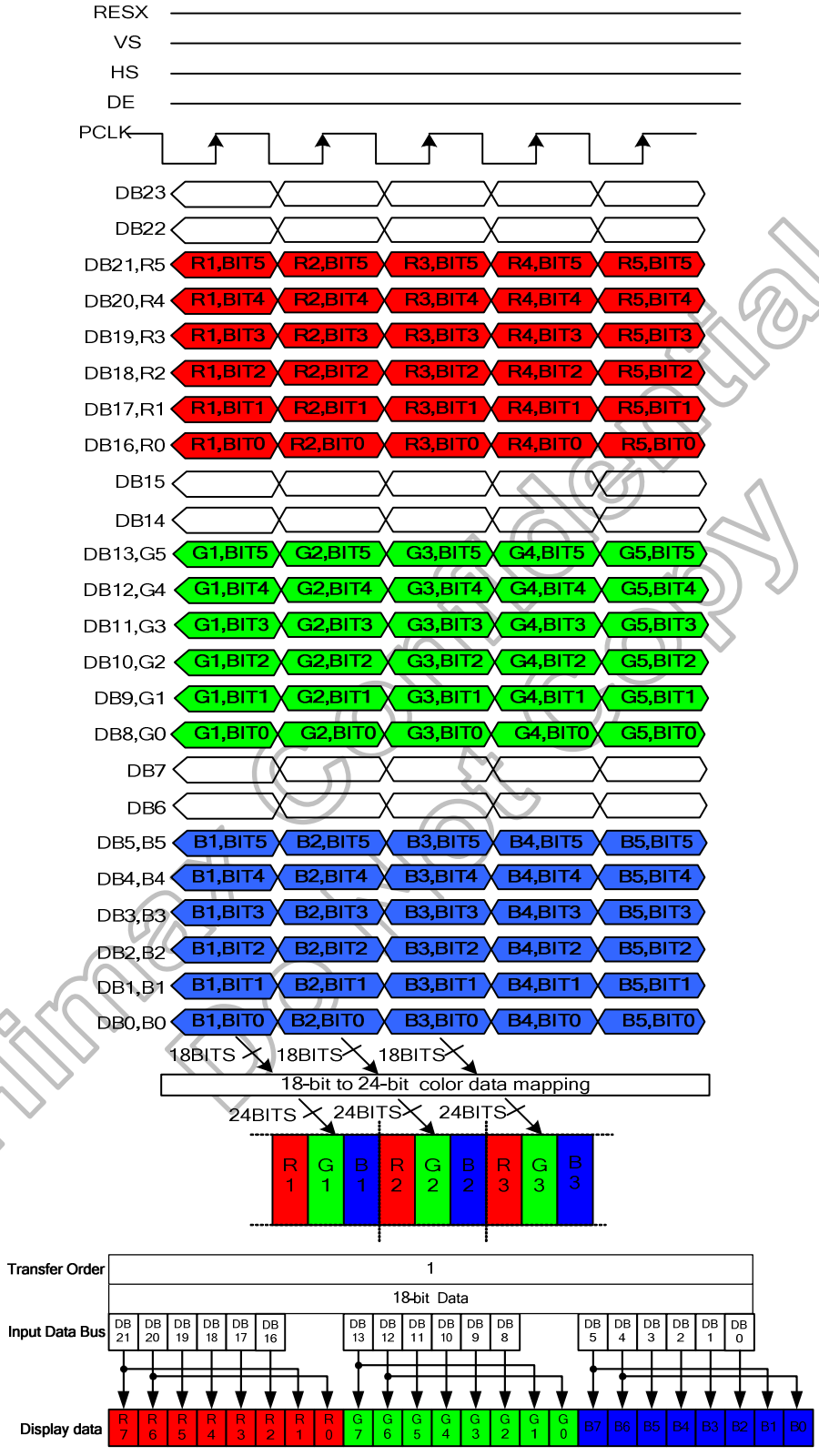


Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.20: 18-Bit / Pixel, 262k Colours Order on the DPI I/F– Configuration 1

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4.1.6.218-bit / pixel color order on the DPI I/F – Configuration 2

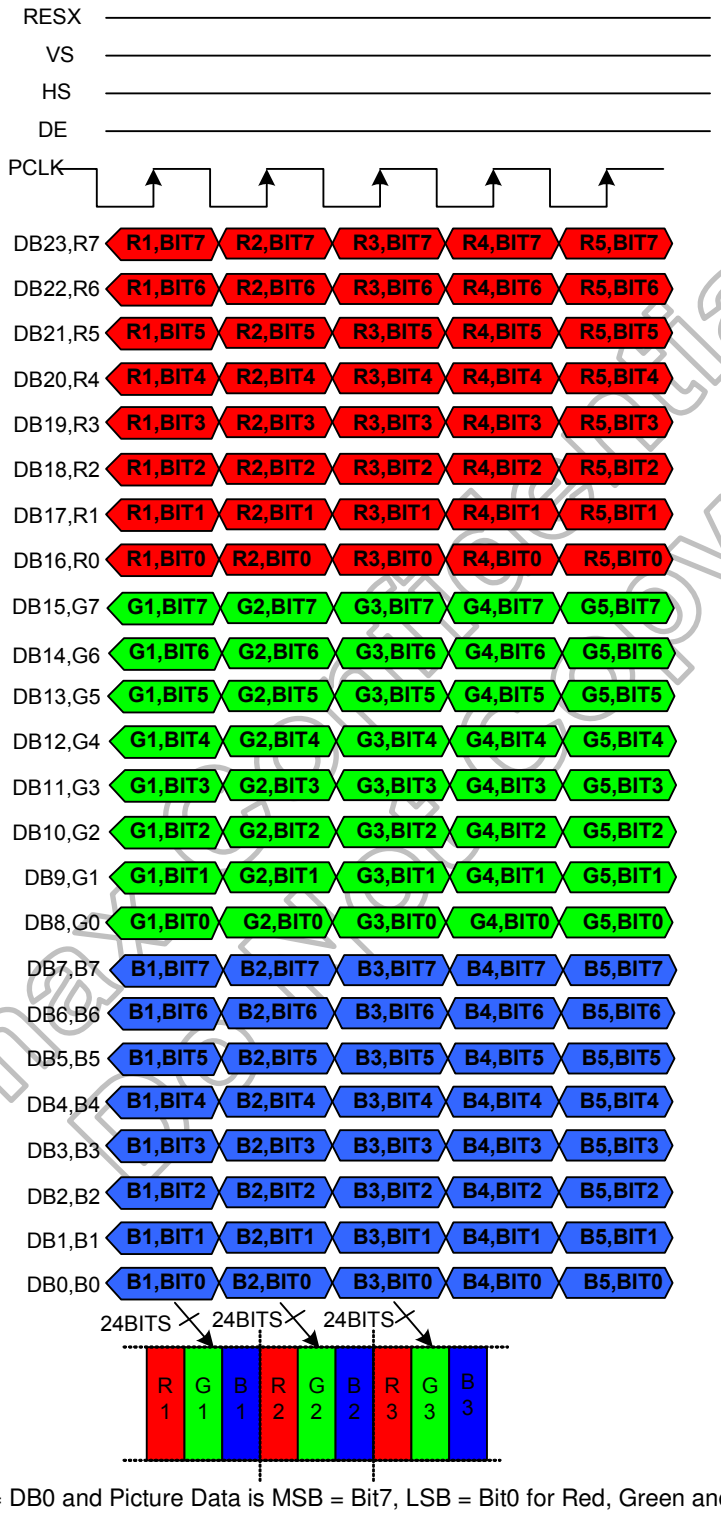


Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.21: 18-Bit / Pixel, 262k Colours Order on the DPI I/F– Configuration 2

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4.1.7 24-bit / pixel color order on the DPI I/F



Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

Figure 4.22: 24-Bit / Pixel, 16.7M Colours Order on the RGB I/F

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4.2 DSI system interface

The DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.23 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands and events.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

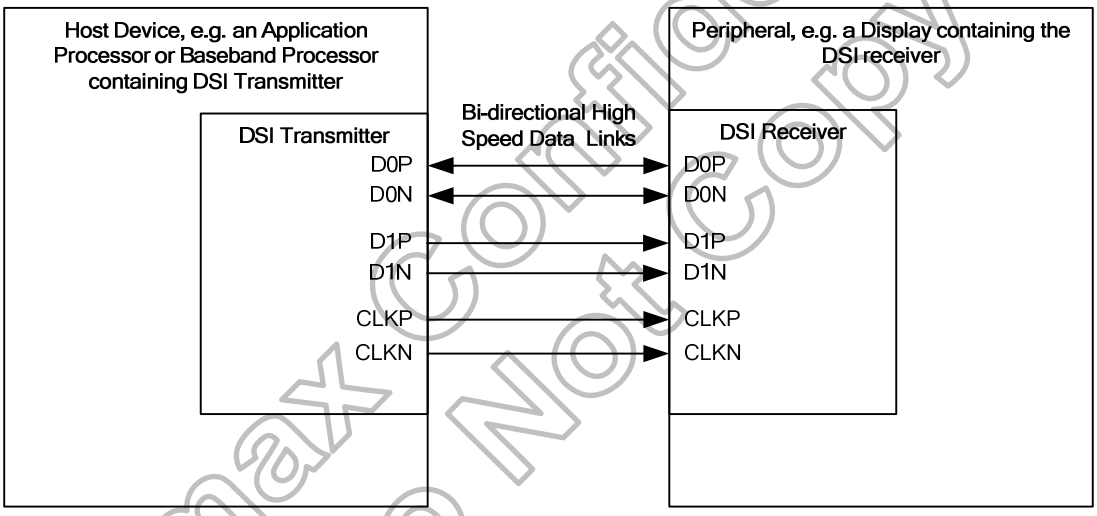


Figure 4.23: DSI Transmitter and Receiver Interface

Please refer to "**DRAFT MIPI Alliance Standard for DSI**" for DSI detailed specifications. The data lane number select by internal register (RBAh).

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4.2.1 DSI layer definitions

According Figure 4.24 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

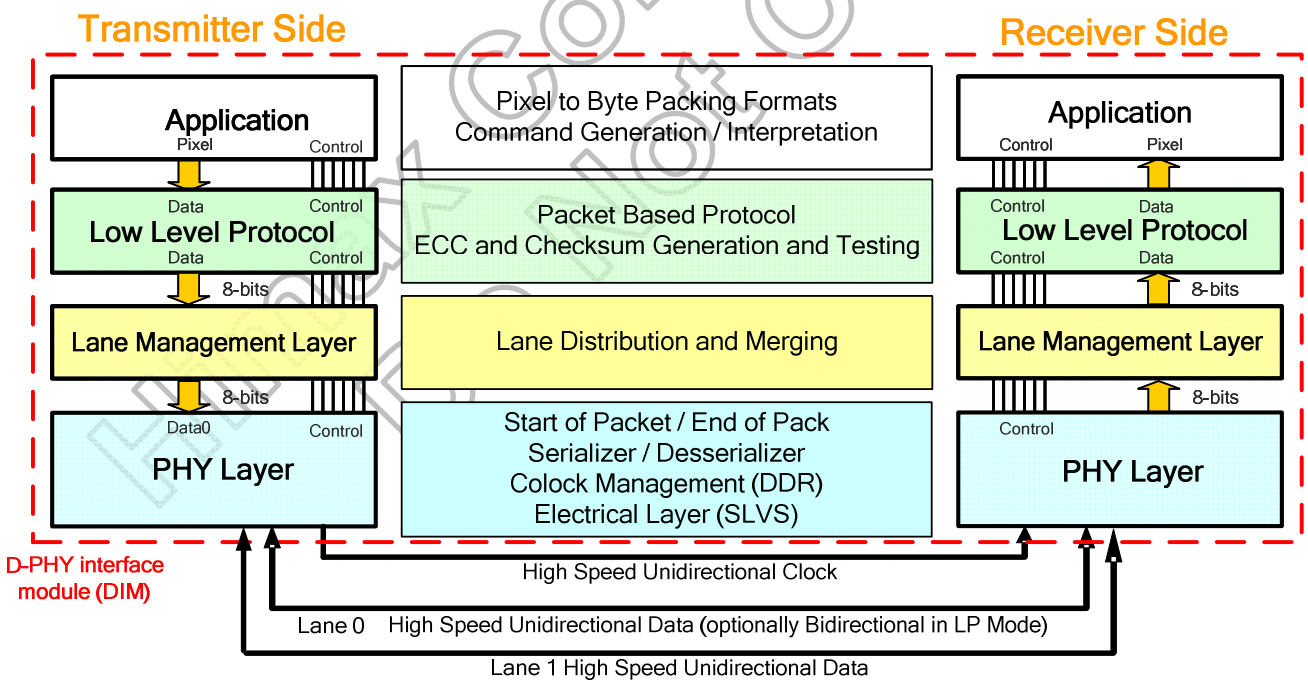


Figure 4.24: DSI Layer

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4.2.1.1 Lane States

The HX8379-C uses Data Lane and Clock Lane differential pairs for DSI. Both differential lane pairs can be driven LP (Low Power) or HS (High Speed) mode.

LP mode means each line of the differential pairs are used independently and single-ended. In LP mode differential receiver is disable (termination resistor of the receiver is disable). In LP mode there are four possible Low-Power Lane states (LP-00, LP-01, LP-10, and LP-11).

HS mode means the differential pairs are not used in single-end and termination resistor of the receiver is enabled. There are different modes and protocol in each mode when transfer display data from MCU to the display module.

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note1	Note1
HS-1	HS High	HS Low	Differential-1	Note1	Note1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note2

Note1: During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.

Note2: If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

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4.2.1.2 Clock Lane Mode

Figure 4.25 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State (ULPS) and High Speed clock transmission.

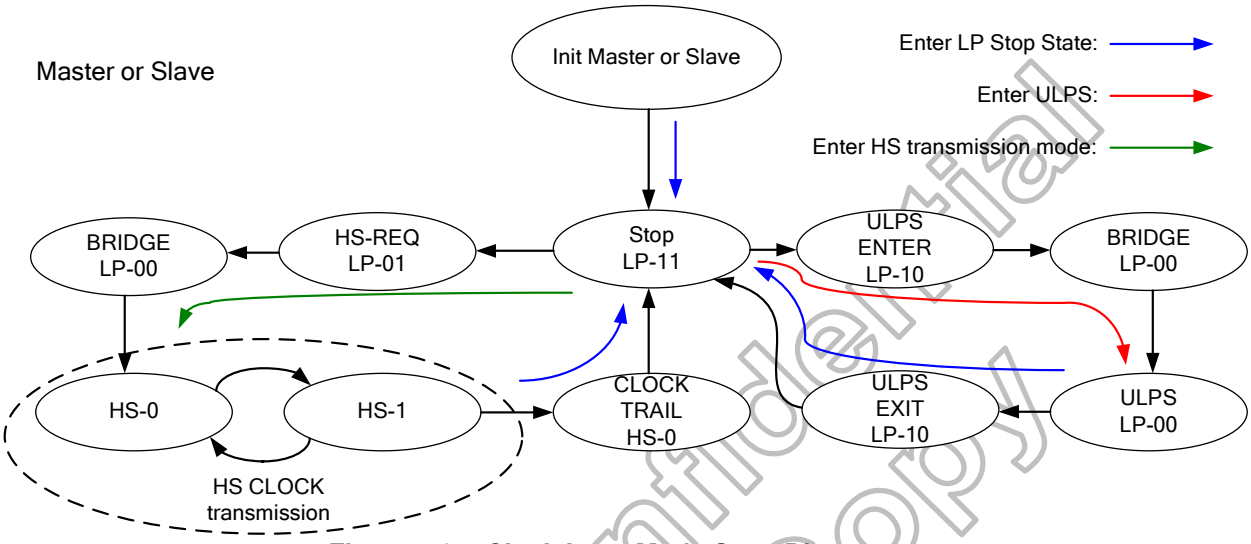
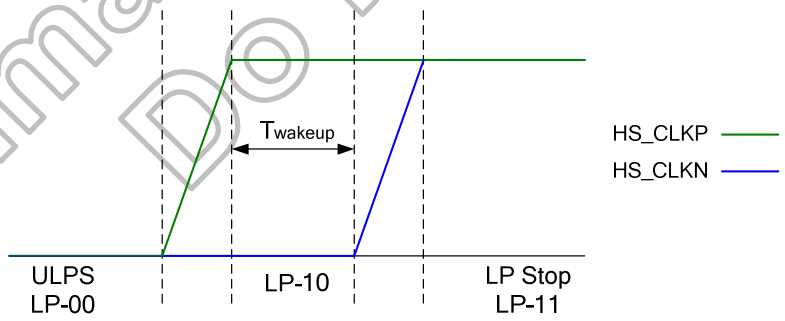


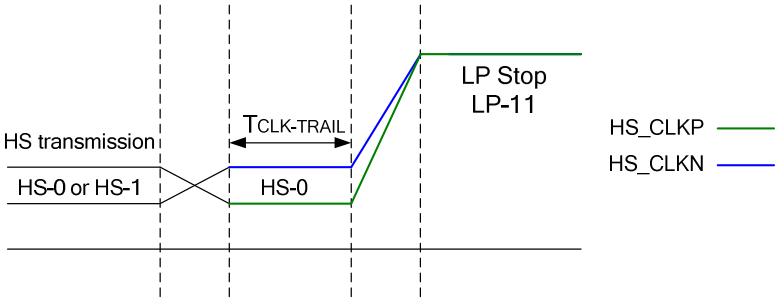
Figure 4.25: Clock Lane Mode State Diagram

Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

(1) After Initial state (HW reset, SW reset, Power on sequence).
(2) Leaving ULPS: ULPS LP-00 -> LP-10 -> Low Power Stop State LP-11.

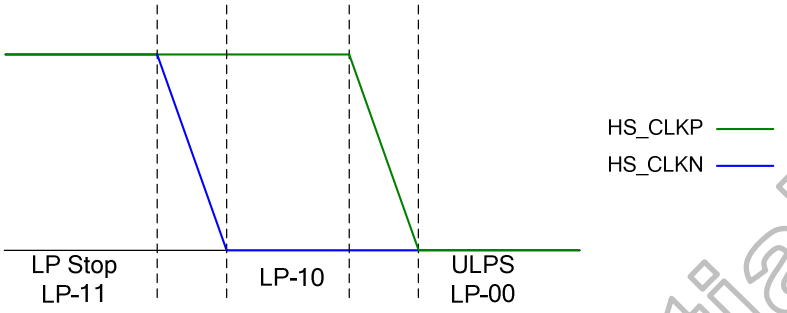


(3) Leaving HS clock transmission mode: HS mode (HS-0 or HS-1) -> HS-0 -> Low Power Stop State LP-11.

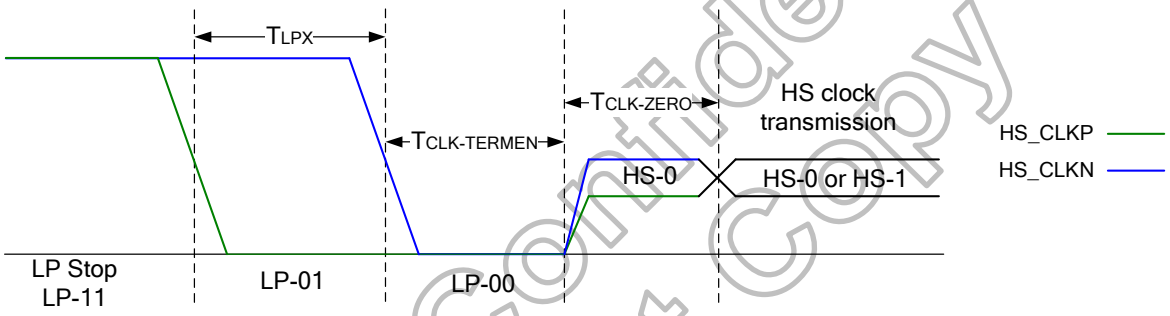


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Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-10 -> ULPS LP-00.



Clock Lane can be High Speed Clock Transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-01 -> LP-00 -> HS-0 -> HS-0/1.



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4.2.1.3 Data Lane Mode

Figure 4.26 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.

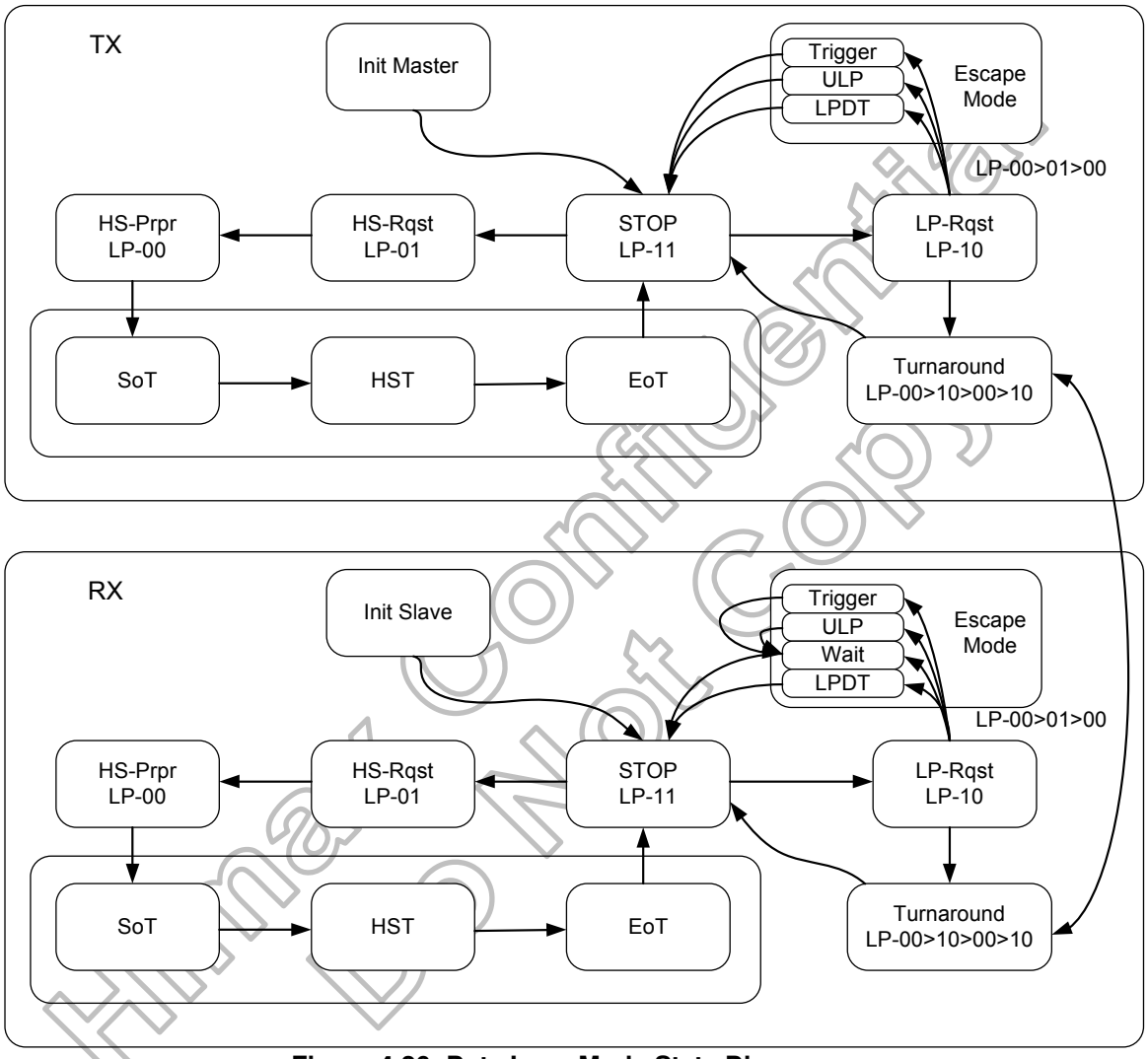


Figure 4.26: Data Lane Mode State Diagram

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4.2.1.3.1 Escape Mode

Data Lane0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-11 -> LP-10 -> LP-00 -> LP-01 -> LP-00 and exit Escape mode via LP-10 -> LP-11.

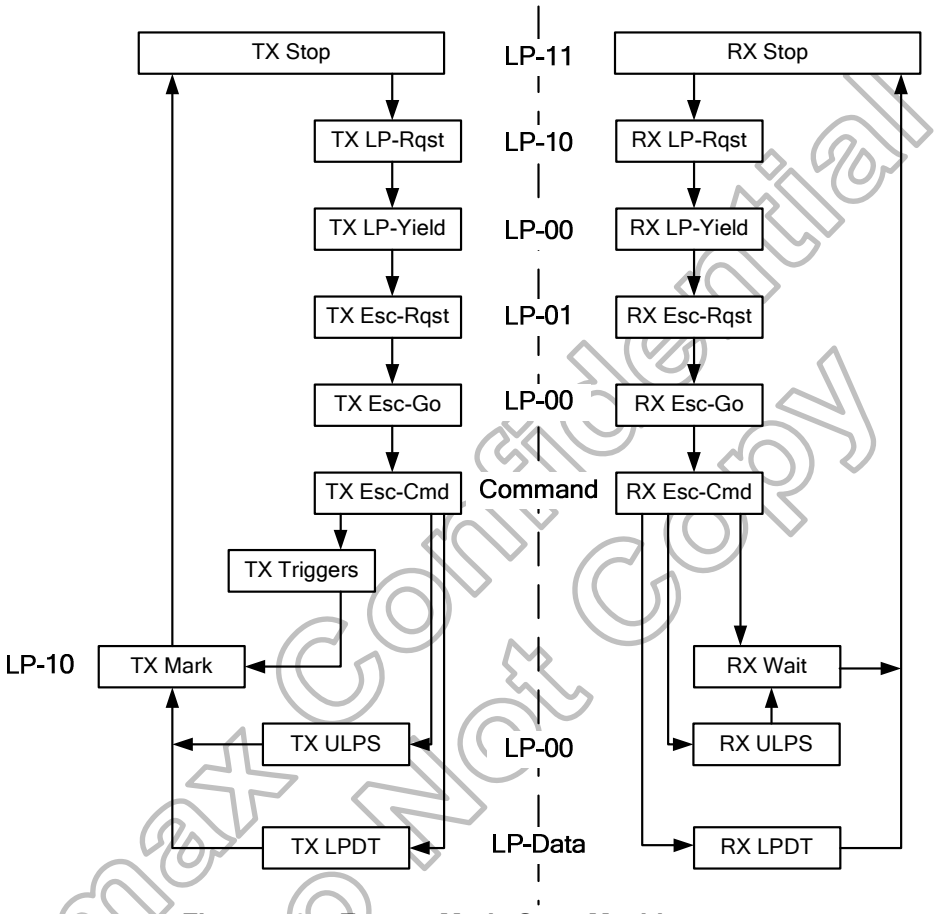


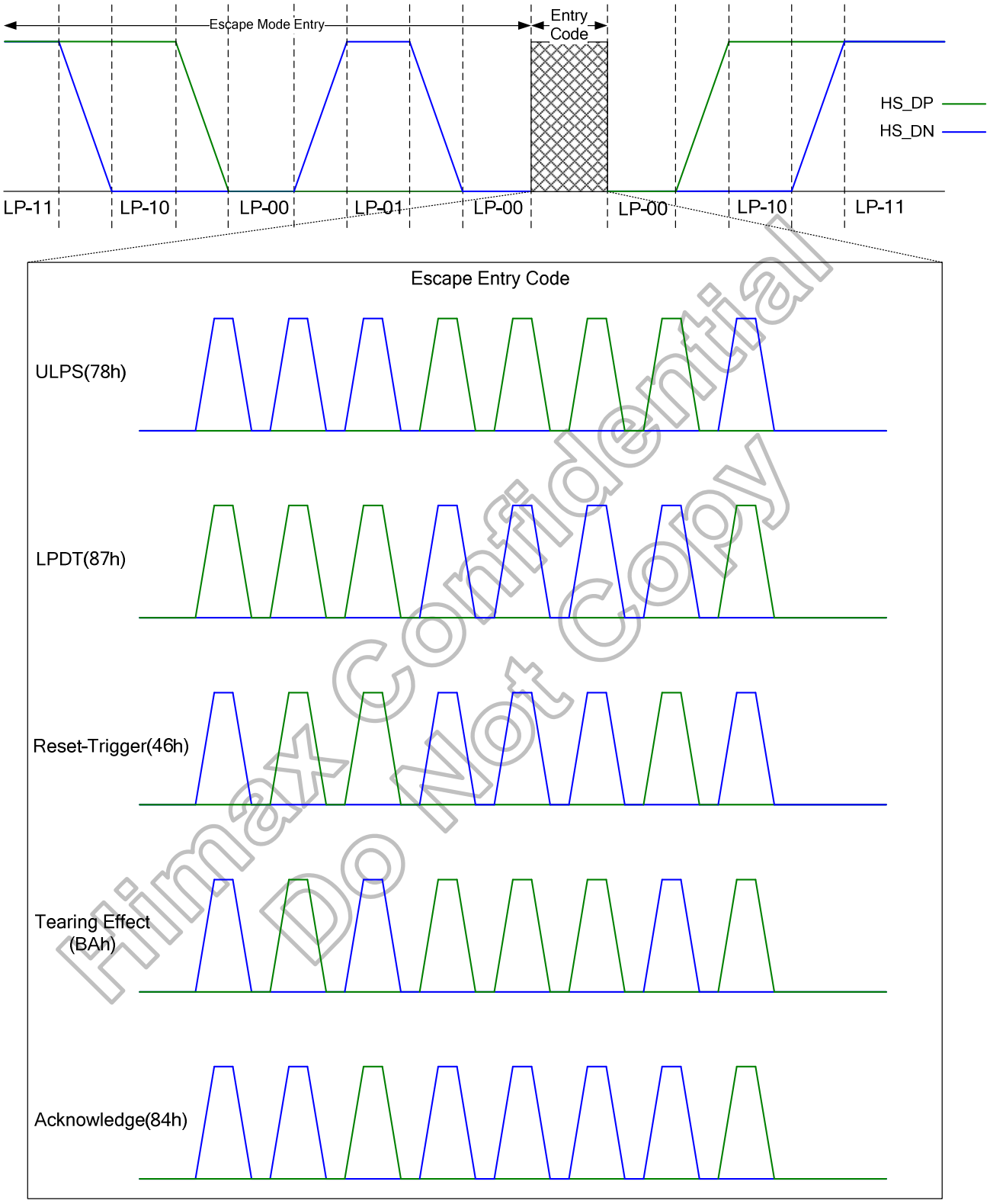
Figure 4.27: Escape Mode State Machine

Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action. The Entry Code as follows:

(1) Trigger (Reset-Trigger(46h), Tearing effect(BAh), Acknowledge(84h))
(2) Drive Data Lane to Ultra Low Power State(78h)
(3) Send Low Power Data Transmission(87h)

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Figure 4.28: Escape Mode Timing Sequence

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4.2.1.3.2 High Speed Data Transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enters High Speed Data Transmission by the flow: LP-11 -> LP-01 -> LP-00 -> SoT (HS-00011101), and exits High Speed Data Transmission by the flow: Toggle the last payload data bit to different state immediately and keeps that state for a time $T_{HS-TRAIL}$.

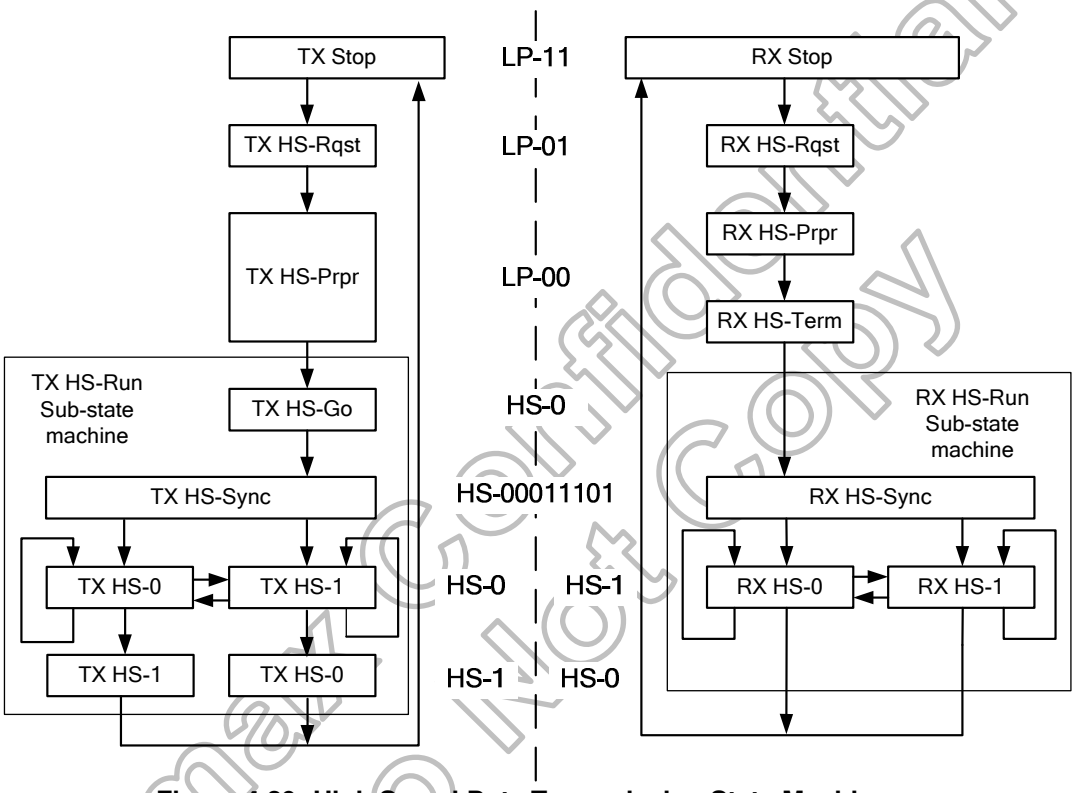


Figure 4.29: High Speed Data Transmission State Machine

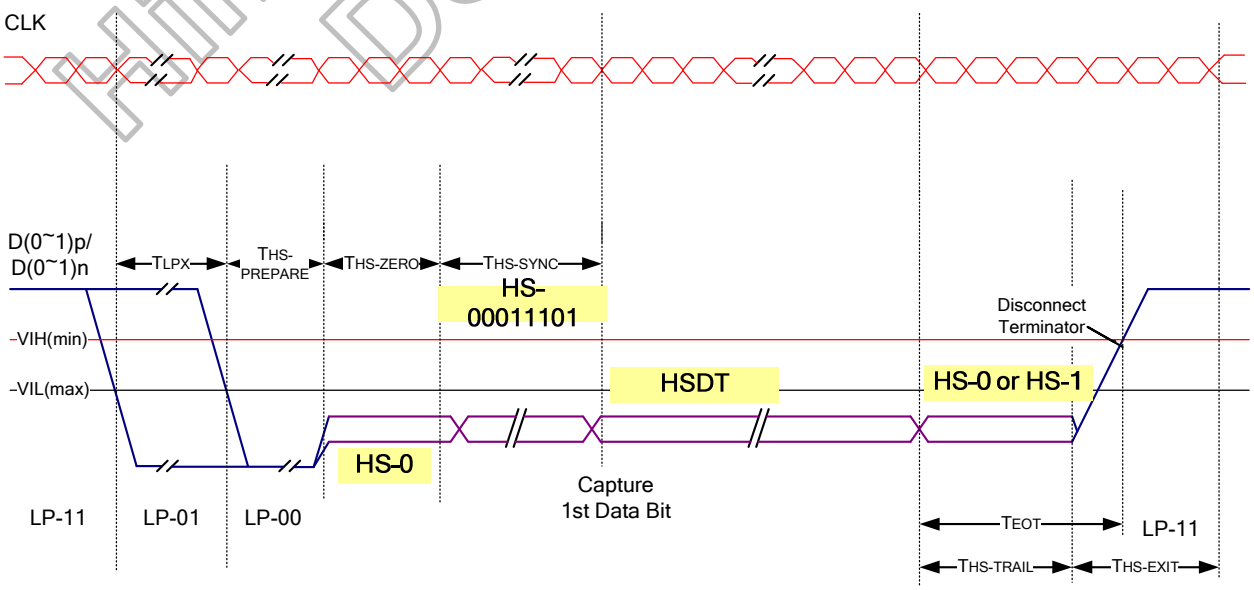


Figure 4.30: High Speed Data Transmission Timing Sequence

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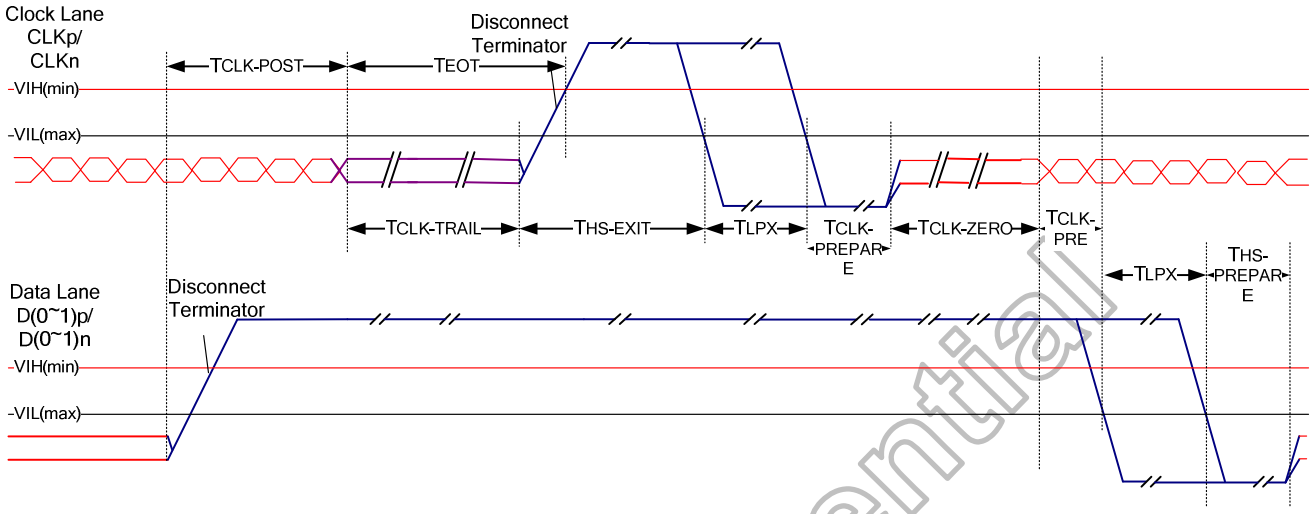


Figure 4.31: Switching the Clock Lane between Clock Transmission and LP Mode

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4.2.1.3.3 Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

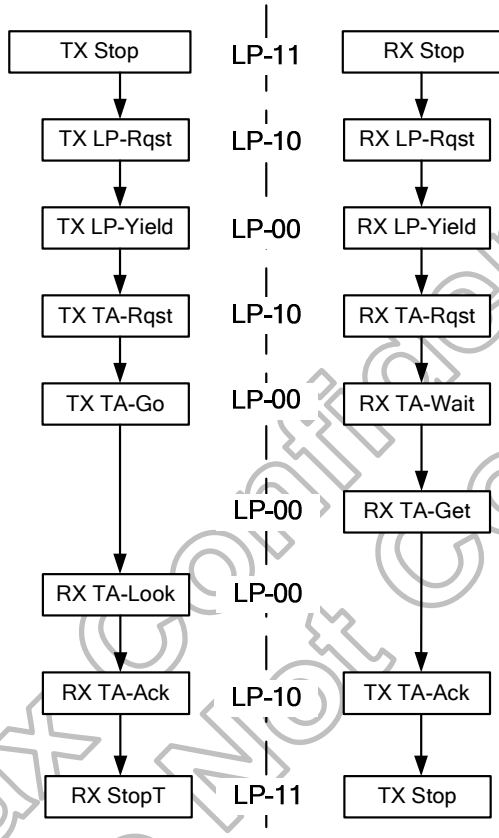


Figure 4.32: Turnaround State Machine

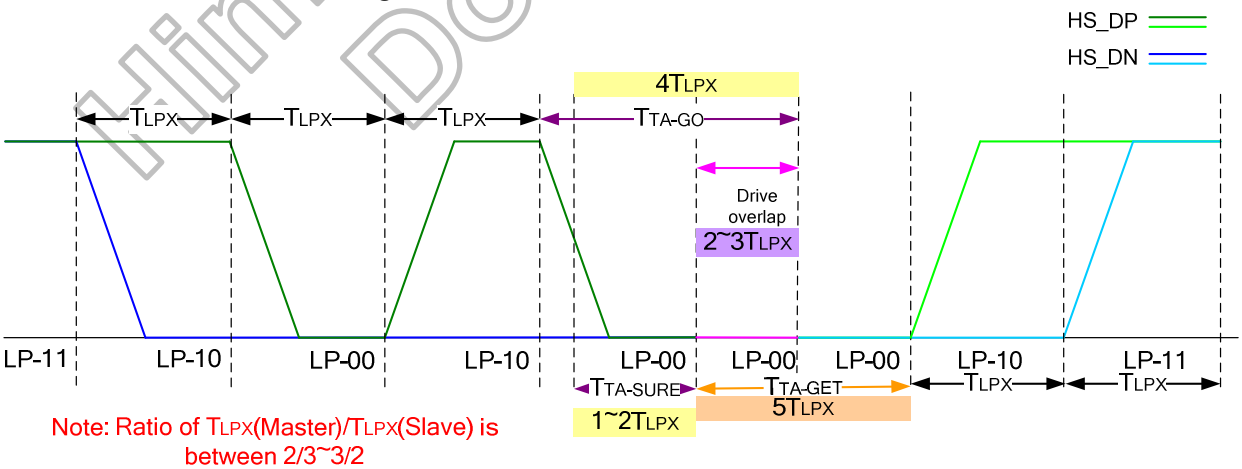


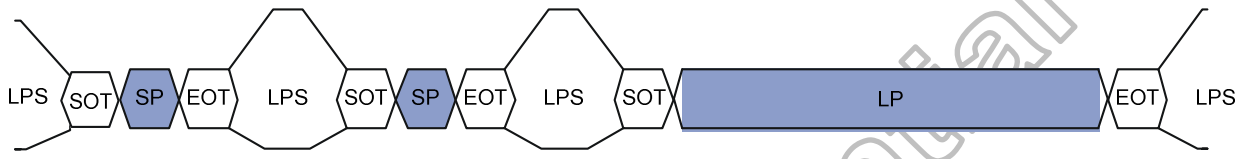
Figure 4.33: Turnaround Procedure

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4.2.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. Figure 4.34 illustrates a case where multiple packets are being sent separately.

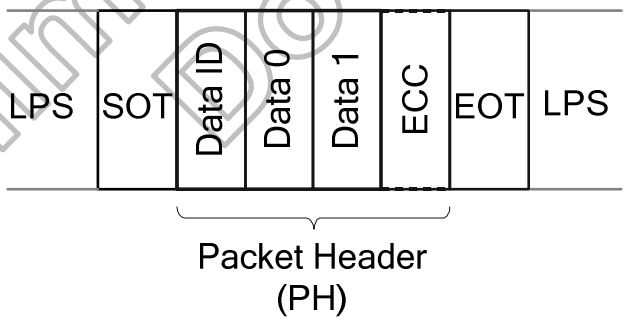


LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

Figure 4.34: Separate HS Transmission Packets

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet.

Short packets shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. Figure 4.35 shows the structure of the Short packet.



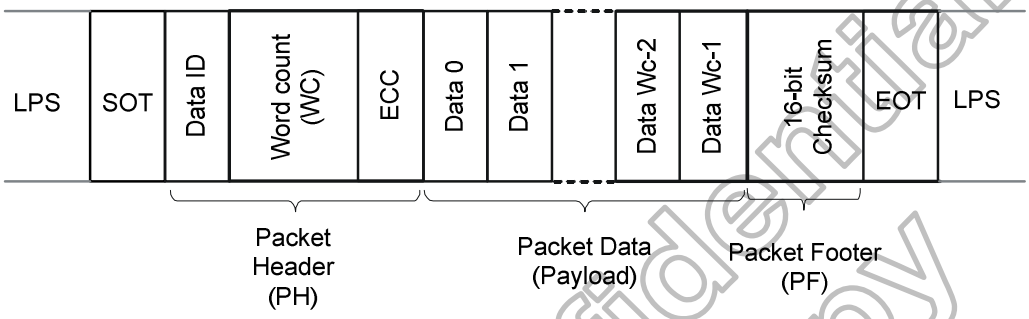
DI(Data ID)：Contain Virtual Channel Identifier and Data Type.
ECC(Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4.35: Short Packet Structure

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Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.36 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

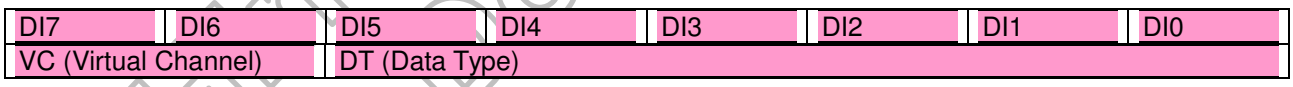
Where 65,541 bytes = (2^{16}-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：The receiver use WC to define packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：16-bit Checksum.

Figure 4.36: Long Packet Structure

According to packet form, basic elements include DI and ECC. Figure 4.37 the shows format of Data ID.



DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

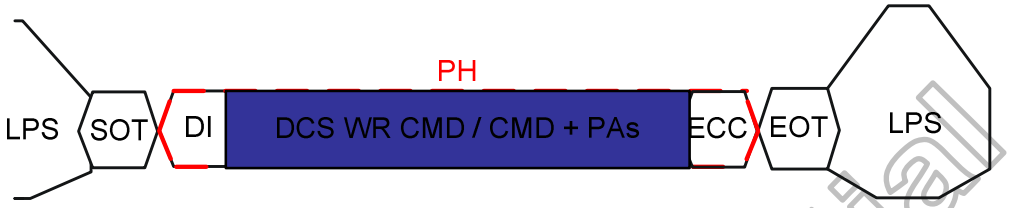
Figure 4.37: The Format of Data ID

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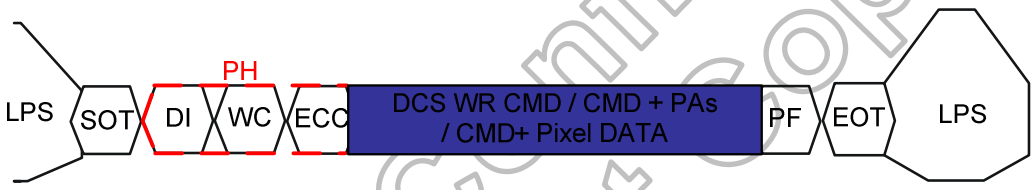
Figure 4.38 show Short- / Long-packet command transmission sequence.

Short packet write Command / Parameters:



DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

Long packet write Command / Parameters / Pixel Data:



DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Figure 4.38: Short- / Long Packet Command Transmission Sequence

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4.2.3 Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.5 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet(EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
05h	000101	DCS WRITE, no parameter	Short
15h	010101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
29h	10 1001	Generic Long Write	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.5: Data Types for Processor-sourced Packets

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The following tables list function of all data types in detail.

Sync Event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h 11h 21h 31h	V Sync start, Start of VSA pulse. V Sync End, End of VSA pulse. H Sync Start, Start of HSA pulse. H Sync End, End of HSA pulse.	4 bytes (DI+Data0+Data1+ECC)
Note: V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.		

EoT Packet		
Data type, hex	**Function description**	**Number of bytes**
08h	End of Transmission Packet (EoTp) (08,0F,0F,01)	4 bytes (DI+Data0+Data1+ECC)
Note: The main objective of the EoTp is to enhance overall robustness of the system during HS transmission mode. Therefore, DSI transmitters should not generate an EoTp when transmitting in LP mode.		

Color Mode Off /On Command		
Data type, hex	**Function description**	**Number of bytes**
02h 12h	Color Mode Off Packet (02,00,00,0B) Color Mode On Packet (12,00,00,18)	4 bytes (DI+Data0+Data1+ECC)
Note: Color Mode Off is a Short packet command that returns a Video Mode display module from low-color mode to normal display operation. Color Mode On is a Short packet command that switches a Video Mode display module to a low-color mode for power saving.		

Display Status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h 32h	Shutdown Peripheral Packet (22,00,00,1E) Turn On Peripheral Packet (32,00,00,0D)	4 bytes (DI+Data0+Data1+ECC)
Note: Shutdown Peripheral command that turns off the display in a Video Mode display for power saving. Turn On Peripheral command that turns on the display in Video Mode display for normal display.		

DCS Short Write Packet (0,1 parameter)		
Data type, hex	**Function description**	**Number of bytes**
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types = 00 0101(05h), 01 0101 (15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)
NOTE: (1) For write part, If DCS Short Write command, followed by BTA (Bus Turn-Around), the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.		

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC

Ex. 05h, 29h, 00, 1Ch — Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC

Ex. 15h, 36h, 08h, 11h — MADCTL(36h)-BGR bit=1

DCS Read Request,No Parameter		
Data type, hex	**Function description**	**Number of bytes**
06h	DCS Read Request, the returned data may be of Short or Long packet format.	4 bytes (DI+Data0+Data1+ECC)

NOTE: (1) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(2) The peripheral shall respond to DCS Read Command Request in one of the following ways:

◆ If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral

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shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(3) **One byte <= Length of payload DATA <= 2^{WC}-1**

Return Packet Size Setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + WC + ECC)

Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

Null Packet and Blanking packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

Note: (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.
(2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display,

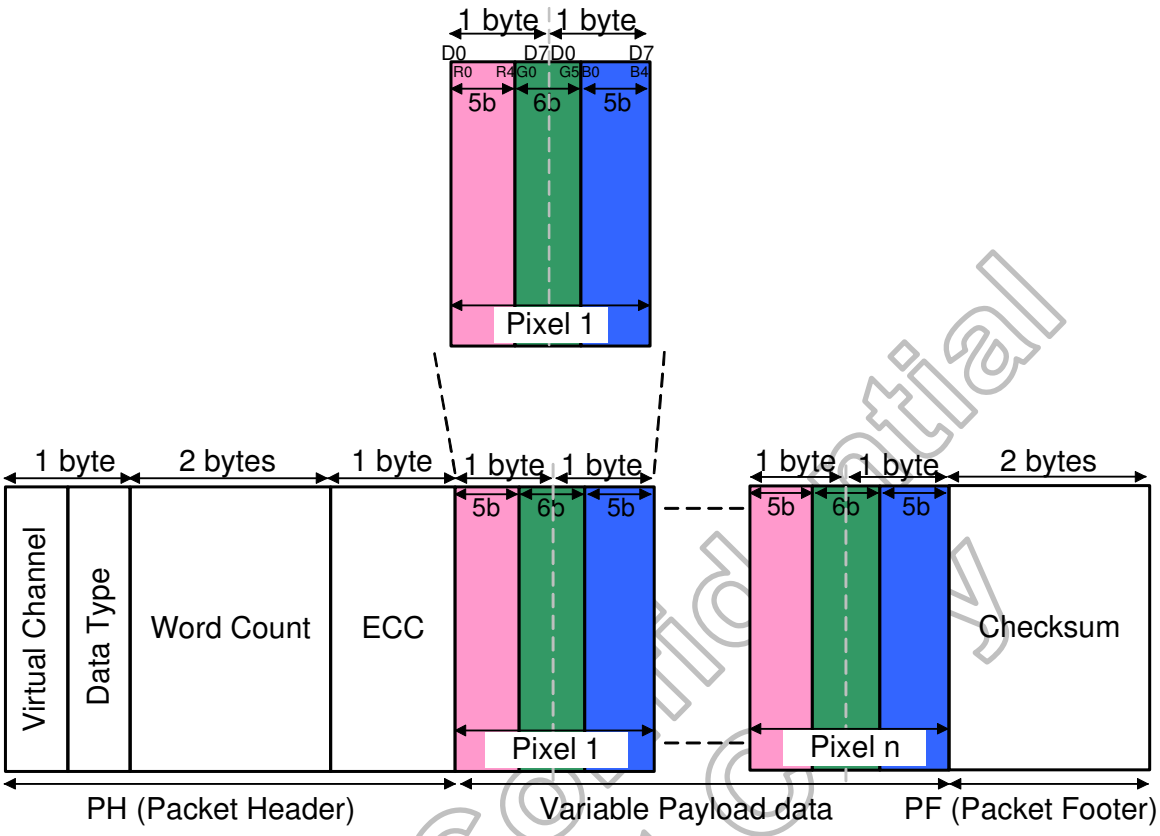
DCS Long Write packet		
Data type, hex	**Function description**	**Number of bytes**
39h	DCS Long Write/ Write_LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Generic Long Write packet		
Data type, hex	**Function description**	**Number of bytes**
29h	A:Same as DCS Long Write (39h) B:Continuous Write Function , could be used after 29h / 39h	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1) For DCS Long Write: Send a NOP or NULL packet in front of 29h to avoid Continuous Write Function beginning.
(2) For Continuous Write: WC shoud be 4N+1 and the times of continuous write cannot be over 3 times.

Data Stream Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

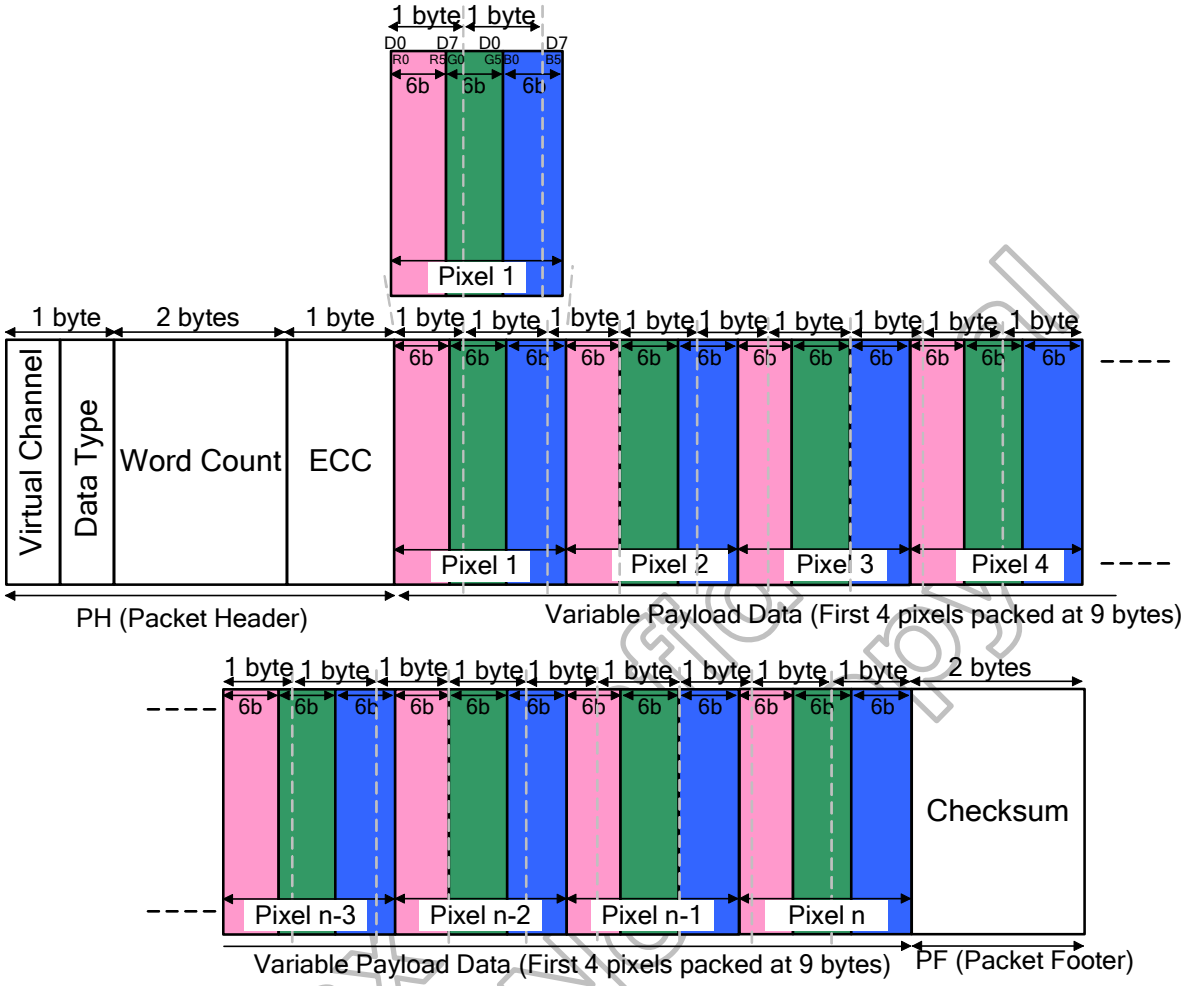
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Note: Within a color component, the "LSB is sent first, the MSB last ".

Data Stream Format		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

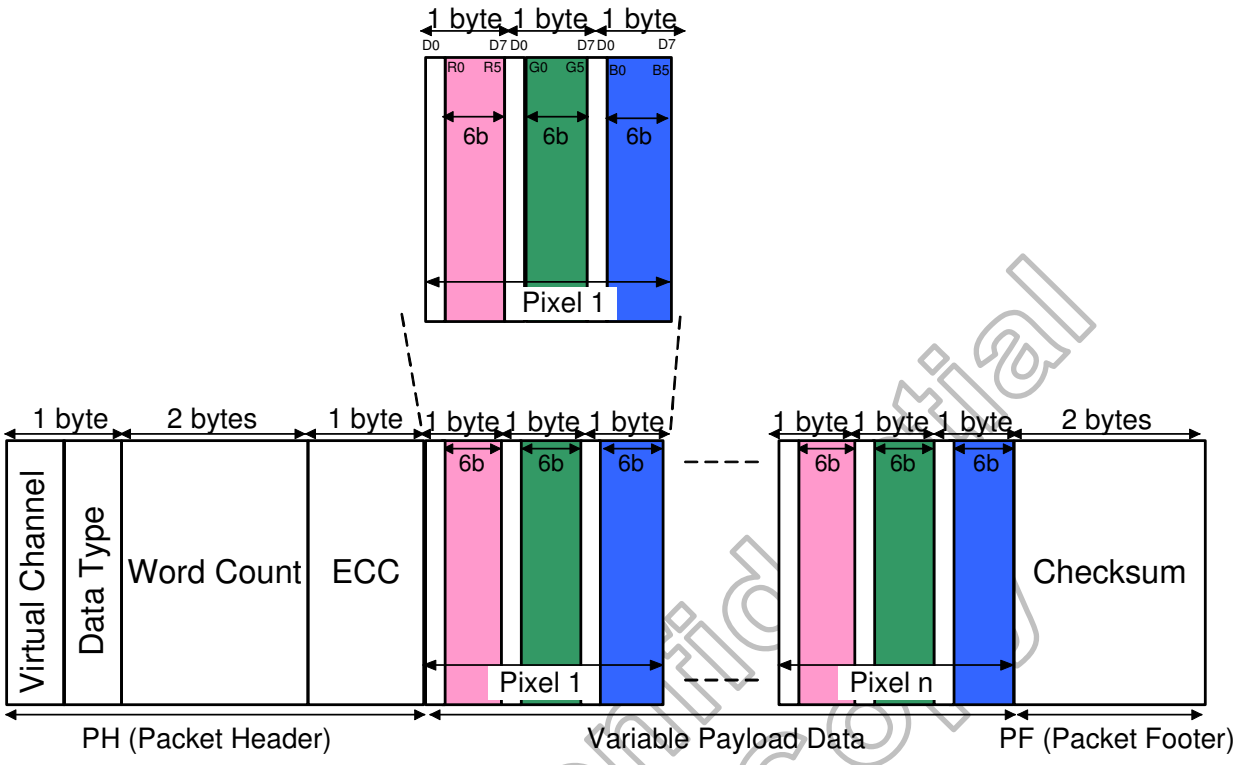
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Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

Data Stream Format		
Data type, hex	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

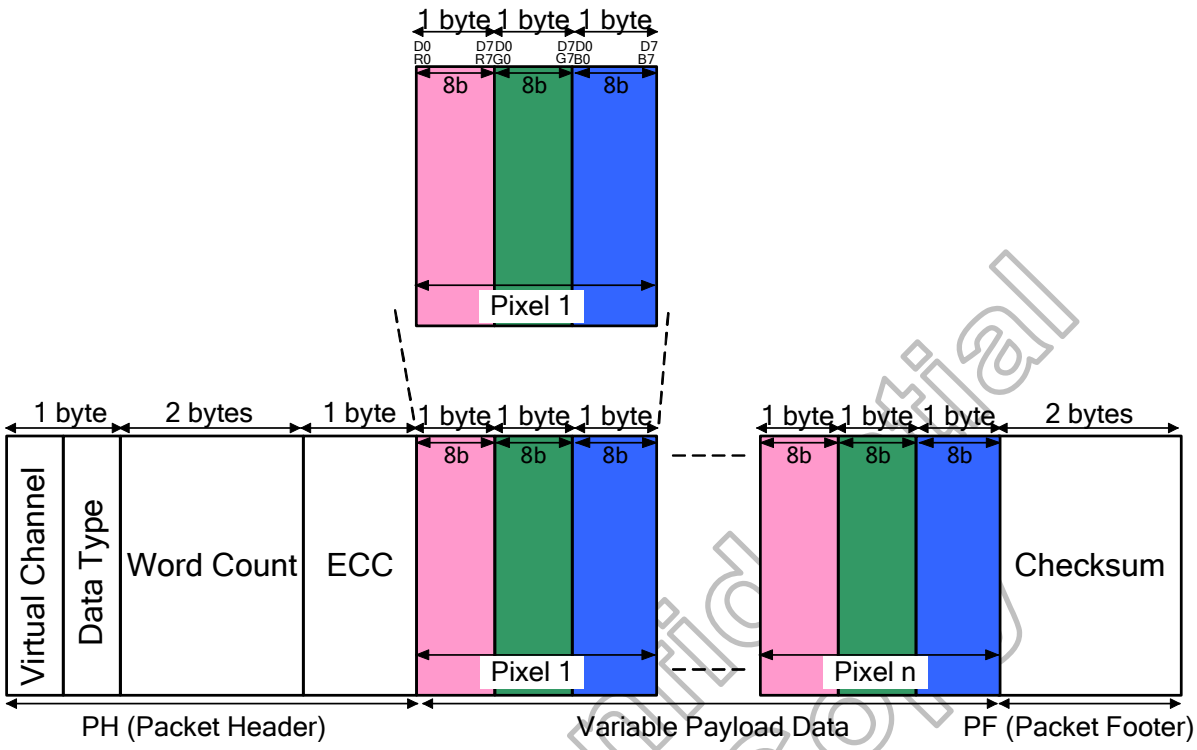
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Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Packed Pixel Stream, 24-bit format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

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Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

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4.2.4 Peripheral to processor (reverse direction)

HX8379-C has the bidirectional capability for returning READ data, ACK or error information to the host processor. The packet structure for peripheral-to-processor transactions is the same as that for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

A. *Tearing Effect:* a trigger message sent to convey display timing information to the host processor.
B. *Acknowledge:* a trigger message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
C. *Acknowledge and Error Report:* a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
D. *Response to Read Request:* a Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain the following forms.

A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report*)* packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report*)* packet, the Error Report shall have the ECC Error flag set.
E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is composed of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.6 shows the Error Report Bit Definitions. And Table 4.7 lists complete set of peripheral-to-processor Data Types.

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Bit	Description
0	SoT Error
1	SoT Sync Error
2	reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	LP-TX Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	reserved
15	DSI Protocol Violation

Table 4.6: Error Report Bit Definitions.

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)		Reserved	-

Table 4.7: The Complete Set of Peripheral-to-Processor Data Types.

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error→Acknowledge with error report, Without error→ Acknowledge.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

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5. Function Description

5.1 Tearing effect output line

The Tearing Effect output line supplies a panel synchronization signal to the MPU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images.

5.1.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

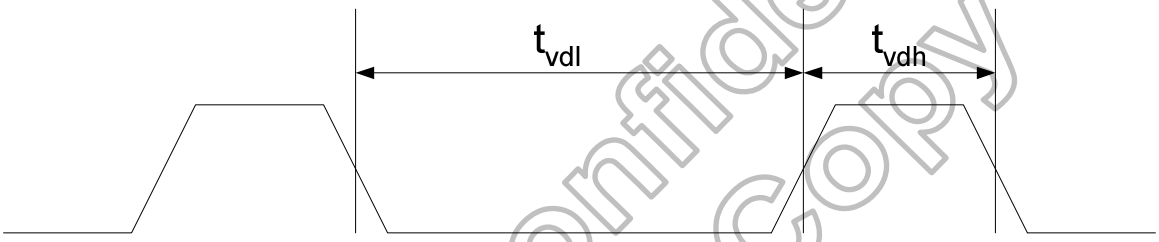


Figure 5.1: Tearing Effect Output Signal Mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TEP[9:0] setting.

Ex: 1. FB=BP=0x01h (3 line) .

TEP[9:0]=0, then TE signal will output after last Line finished.

TEP[9:0]=7, then TE signal will output at second Line start.

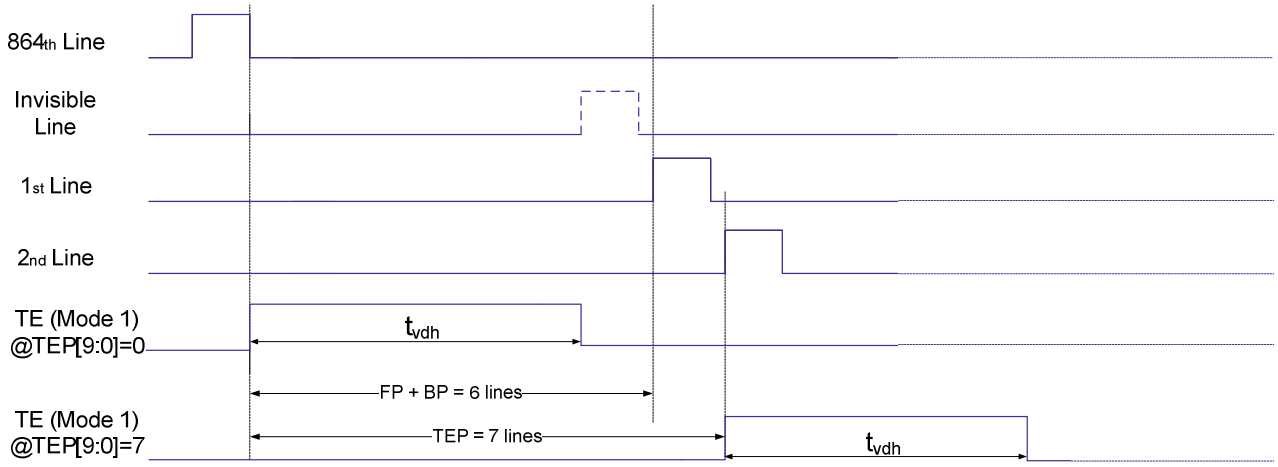


Figure 5.2: TE Delay Output

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Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 864 H-sync pulses per field.

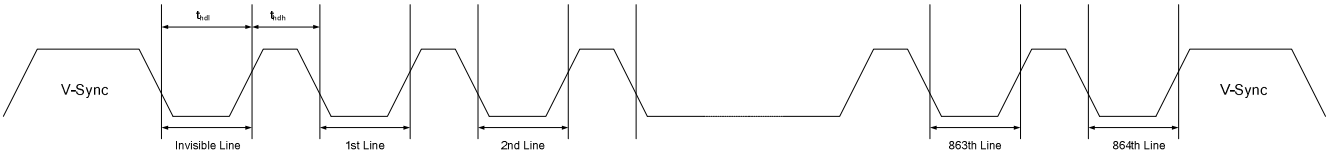


Figure 5.3: Tearing Effect Output Signal Mode 2

thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Under Mode2, the H-sync pulses output amount will be defined by TESL[15:0] setting.

Ex: 1. TESL[15:0]=0, then TE signal will like TE mode 1.

TESL[15:0]=1, then TE signal will output 864 H-sync.

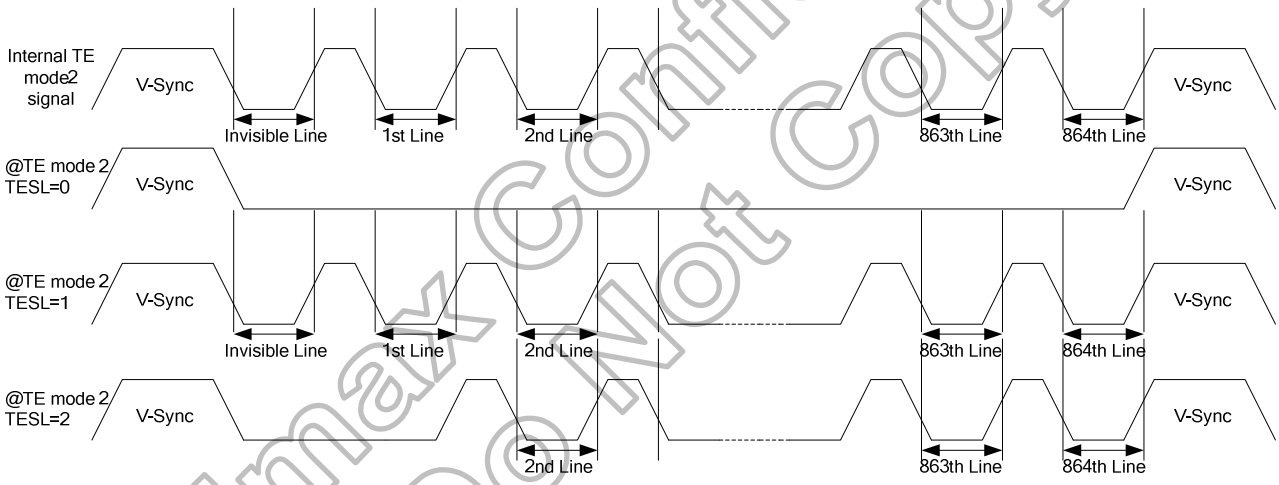


Figure 5.4: TE Output for TELINE Setting

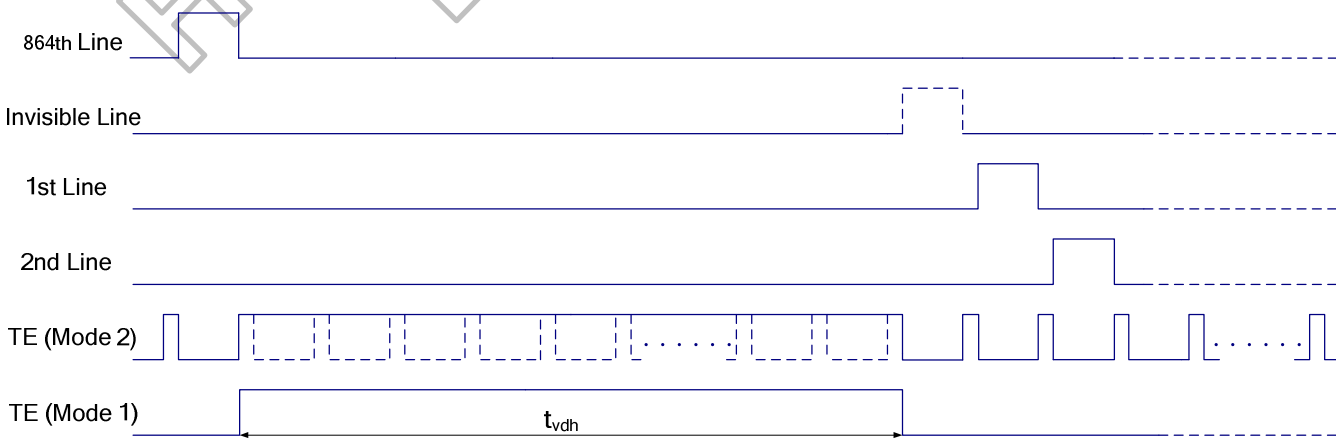


Figure 5.5: Tearing Effect Output Signal

Note: During Sleep In Mode, the Tearing Output Pin is active Low

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5.1.2 Tearing effect line timing

The tearing effect signal is described below :

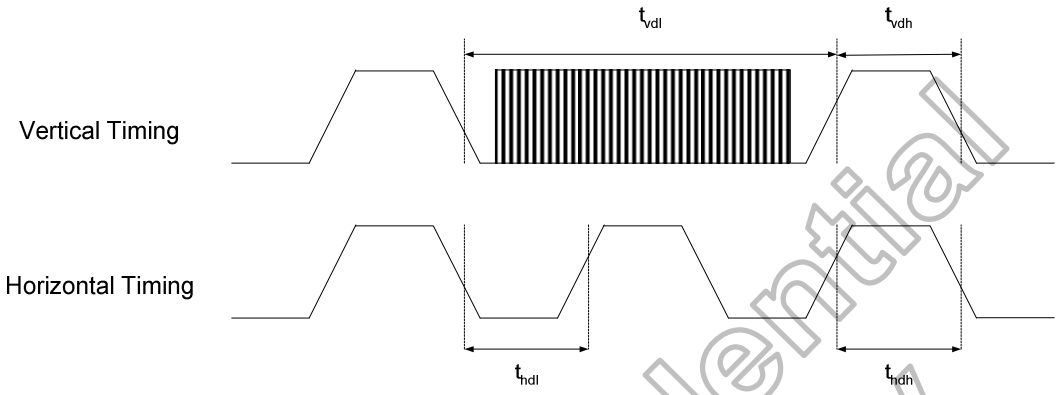


Figure 5.6: Tearing Effect Line Timing

Idle mode off (Frame rate=60Hz)

Symbol	Parameter	Min.	Max.	Unit	description
tvdl	Vertical Timing Low Duration	15	-	ms	-
tvdh	Vertical Timing High Duration	VFP+VHP+VBP	-	us	-
tr	Rise Time	-	15	ns	-
tf	Fall Time	-	15	ns	-

Note: The timings in Table 5.1 apply when MADCTL ML=0 and ML=1

Table 5.1: AC Characteristics of Tearing Effect Signal

The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.

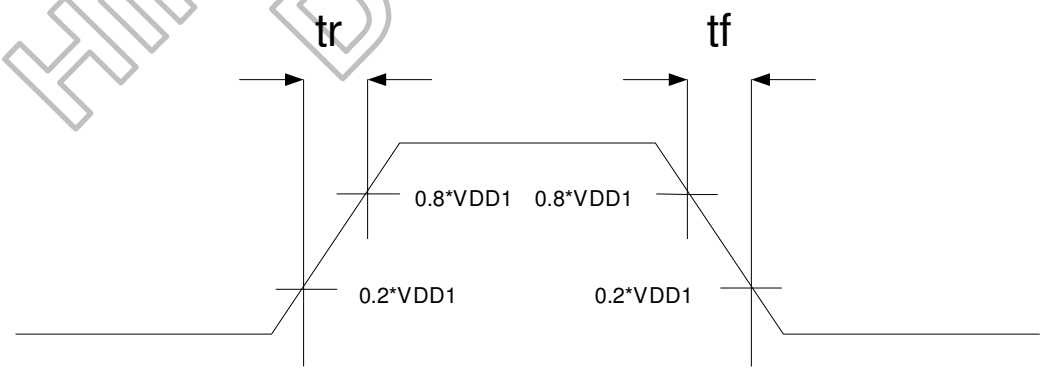


Figure 5.7: Rise and Fall Time of TE Signal

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5.2 Oscillator

The HX8379-C can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to OSC control register (RCBh). The default frequency is 32MHz.

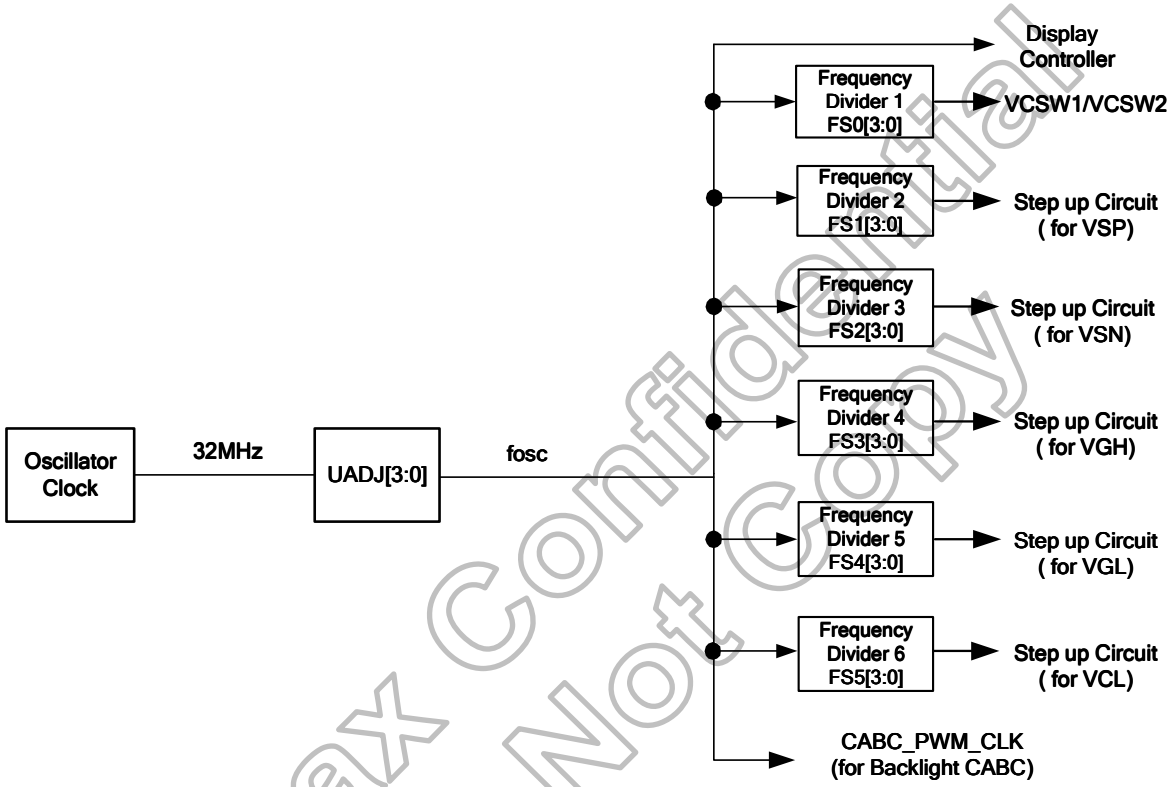


Figure 5.8: OSC Architecture

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5.3 Source driver

The HX8379-C contains 1442-channel source driver which is used for driving the source line of TFT LCD panel. The source driver converts the digital data into the analog voltage for 1442 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

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5.3.1 Zig-Zag Inversion

The HX8379-C supports Zig-Zag inversion which can reduce power consumption. This inversion uses the same polarity as column inversion for data line and has similar display quality as 1-dot inversion. It applies SDUM1 as S0, SDUM2 as S1441.

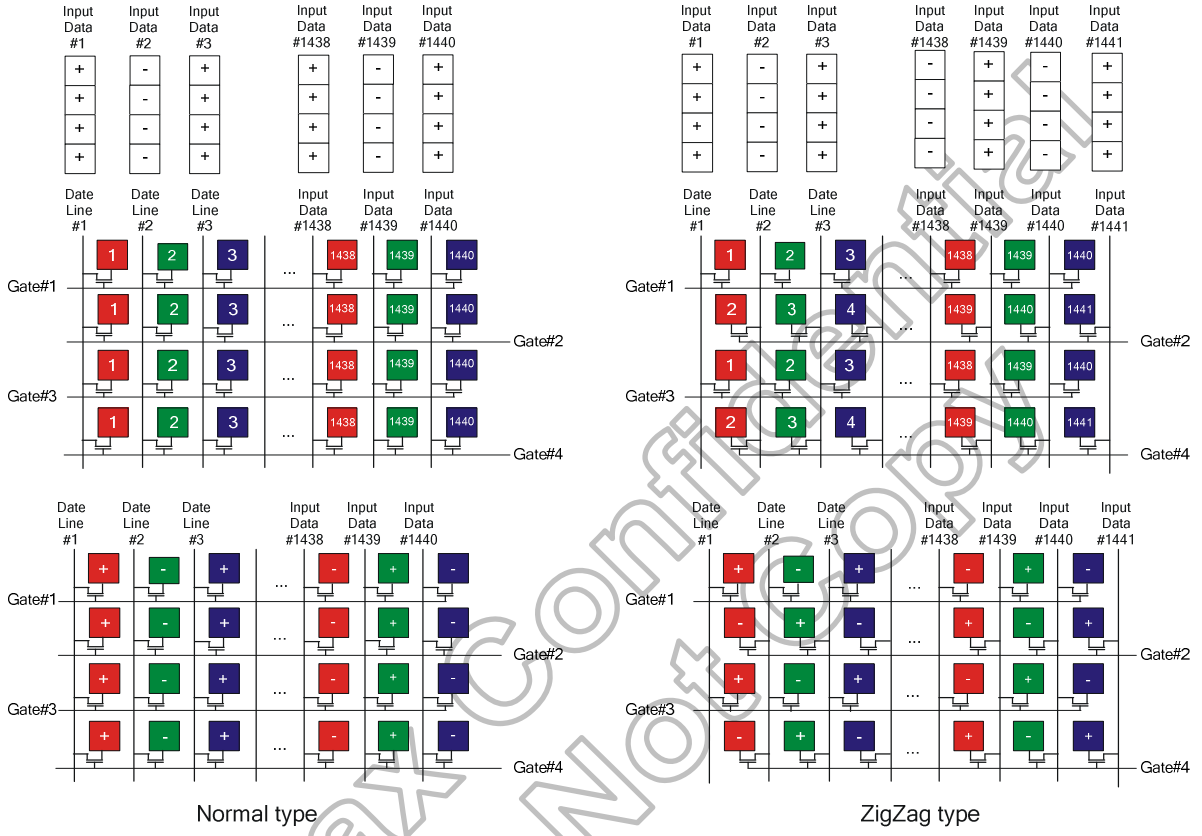
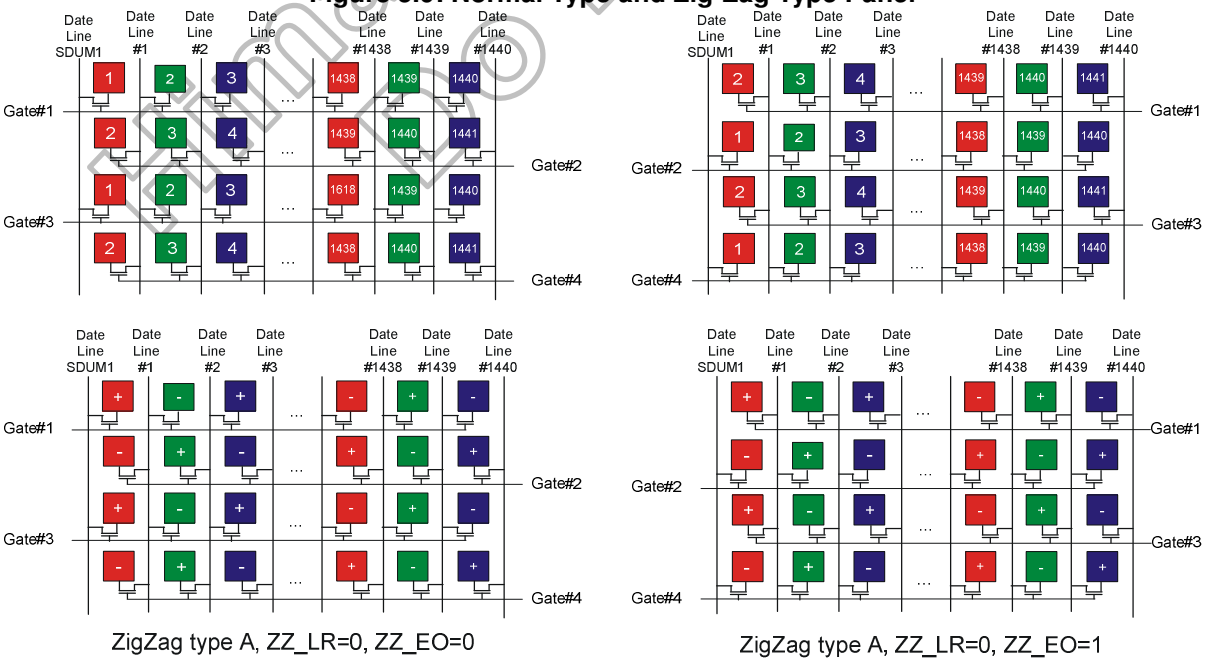
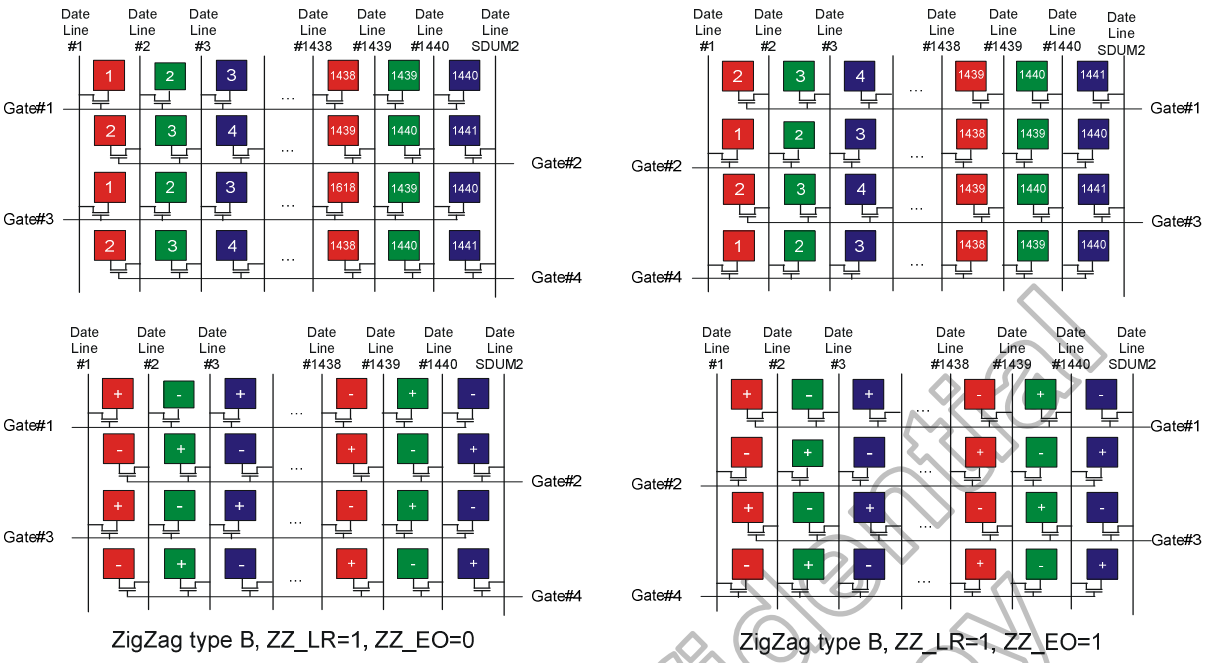


Figure 5.9: Normal Type and Zig-Zag Type Panel



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ZigZag type B, ZZ_LR=1, ZZ_EO=0

ZigZag type B, ZZ_LR=1, ZZ_EO=1

Figure 5.10: Different Zig-Zag Type Panel

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5.3.2 Zig-Zag 2 Inversion

The HX8379-C also supports another Zig-Zag inversion type panel as below.

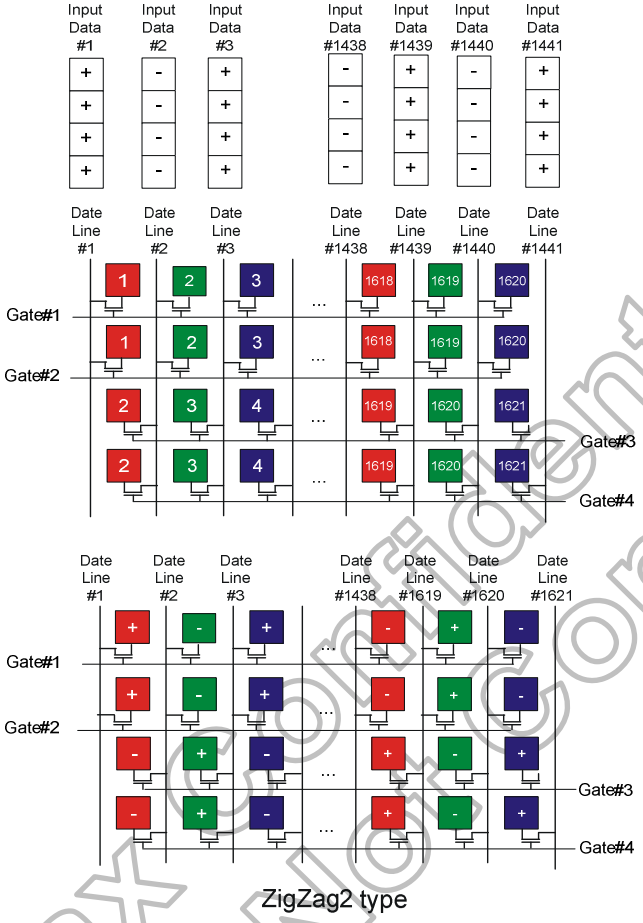


Figure 5.11: ZigZag 2 Inversion

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5.4 LCD power generation scheme

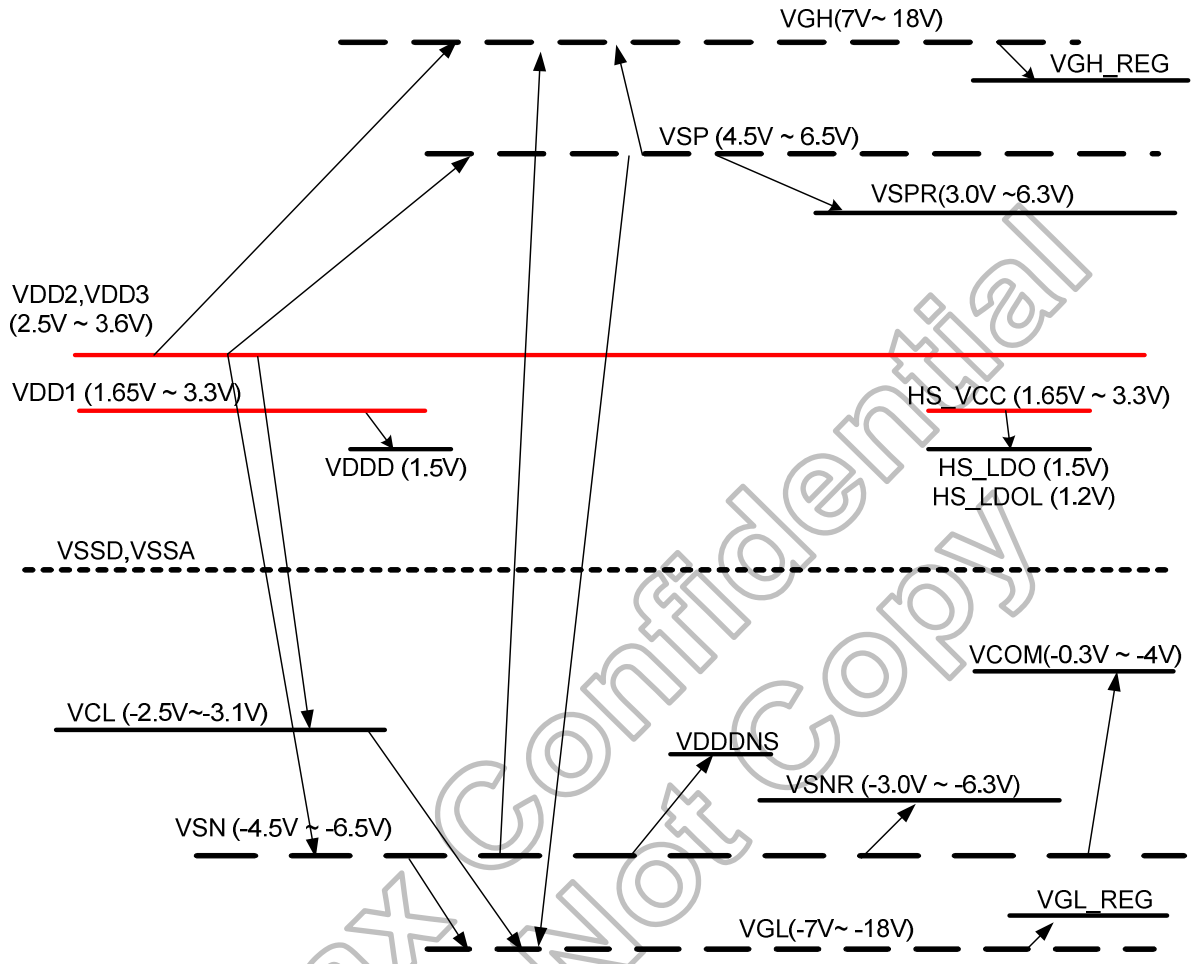


Figure 5.12: LCD Power Generation Scheme

Voltage configuration

Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VREF	Reference voltage from internal band gap circuit	1.64V	-
VSP	DC/DC converter circuit output	4.5V ~ 6.5V	Do not exceed 6.6V
VSN	DC/DC converter circuit output	-4.5V ~ -6.5V	Do not exceed -6.6V
VSPR	Regulated high positive voltage for gamma circuit	3.0V ~ 6.3V	Reference register
VSNR	Regulated high negative voltage for gamma circuit	-3.0V ~ -6.3V	Reference register
VDDD	Logic power supply	1.5V	-
VCL	Negative voltage for level shifter and VSN voltage.	-2.5V ~ -3.1V	-
VGH	Positive gate driver output voltage level	6.4V ~ 18.0V	Depend on VSP and VSN, VGH-VGL<30V
VGL	Negative gate driver output voltage level	-7.0V ~ -15.0V	
VGH_REG	Output regulated voltage for LCD panel	6.4V ~ 18.0V	Reference register
VGL_REG	Output regulated voltage for LCD panel	-7.0V ~ -15.0V	Reference register
VCOM	VCOM DC voltage	-0.3V ~ -4.0V	Reference register
HS_LDO	Analog power for High speed interface circuit	1.5V	DSI I/F
HS_LDOL	Analog power for High speed interface circuit low power mode	1.2V	DSI I/F

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5.5 DC/DC converter circuit

5.5.1 Power Generation Mode

HX8379-C supports various kinds of power generation mode, including internal charge pump mode, external HX5186-A/B/C, or external VSP & VSN power mode. Power mode selection is set by hardware pin(EXT_VSPN) and register(PCCS[1:0]) as below:

- **EXT_VSPN=0(VDD1/2/3 from external circuit ;VSP/VSN from Dr.IC or HX5186)**
- **EXT_VSPN=1(VSP/VSN/VDD1 from external circuit; VDD2/3 from Dr.IC)**

PCCS[1:0]: (valid only in EXT_VSPN=0)

EXT_VSPN	PCCS1	PCCS0	Driving mode
0	0	0	Internal Charge Pump
	0	1	Reserved
	1	0	Reserved
	1	1	HX5186-A/B/C
1	X	X	External VSP/VSN

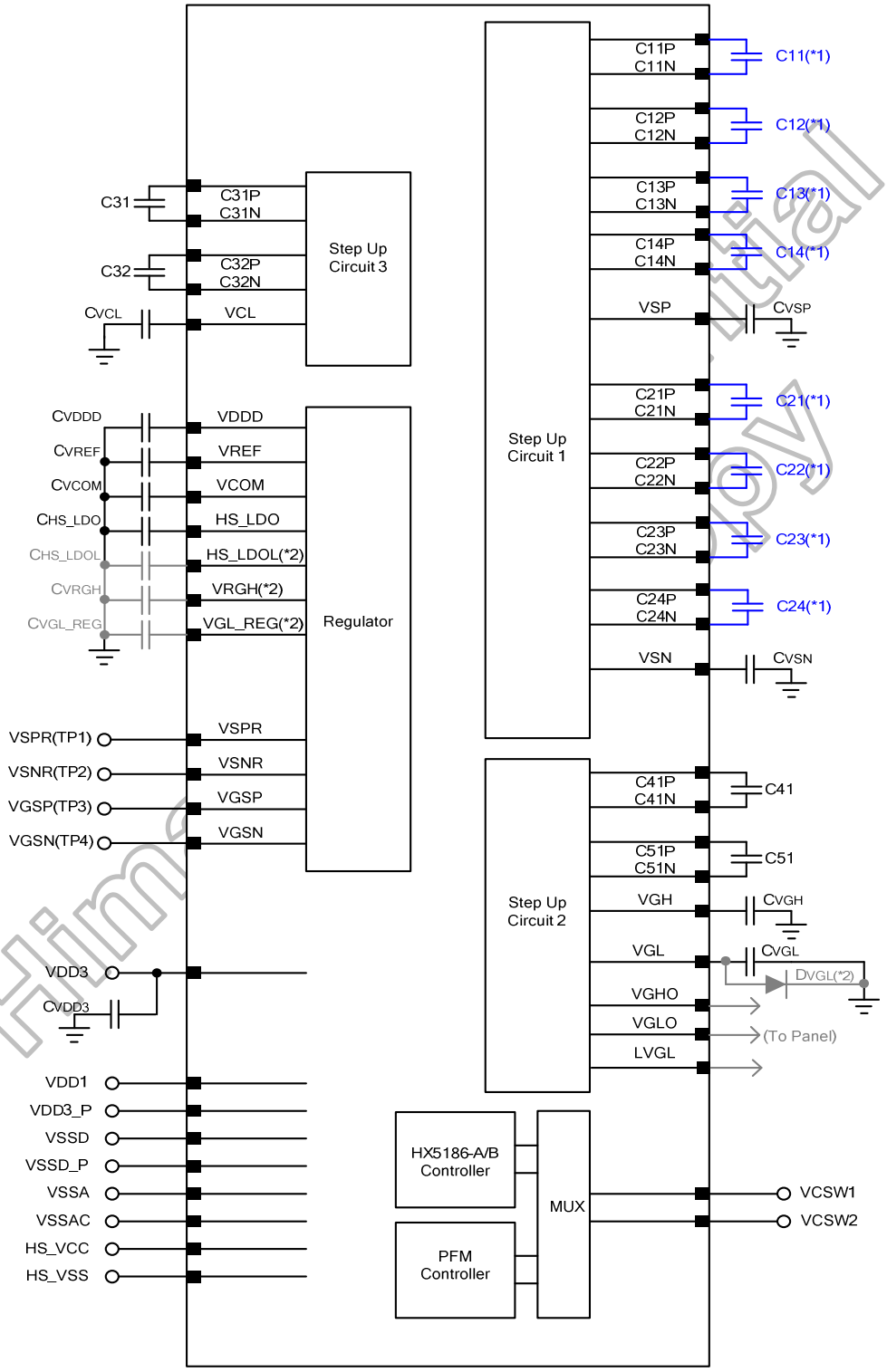
Table 5.2: Power Supply Mode

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5.5.2 Use internal charge pump

HX8379-C generates supply voltage for LCD panel driving and backlight control with internal charge pump.



Note: (1) C11, C12, C13,C14 are for VSP and C21, C22, C23,C24 are for VSN internal charge pump.
(2) The capacitors of VGH_REG, VGL_REG, HS_LDOL and the diode of VGL are optional.

Figure 5.13: Internal Charge Pump

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5.5.3 Use HX5186-A/B/C

The HX5186-A/B/C is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8379-C contains Charge Pump Controller for HX5186-A/B/C, including a comparator for VSP/VSN feedback control. HX5186-A/B/C can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 4.5 to 6.5 (VSP) and -4.5 to -6.5V (VSN)

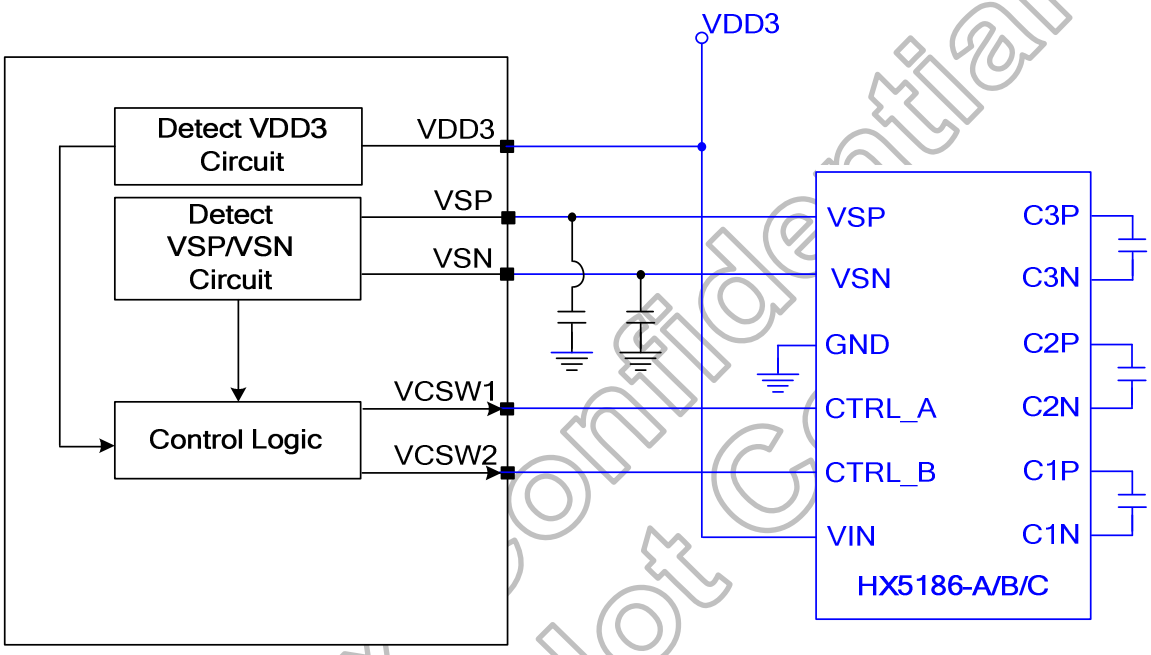


Figure 5.14: DC/DC Converter Circuit (HX5186-A/B/C)

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5.5.4 VSN and VSP from external charge pump

The HX8379-C can use external charge pump to provide VSN and VSP voltage.

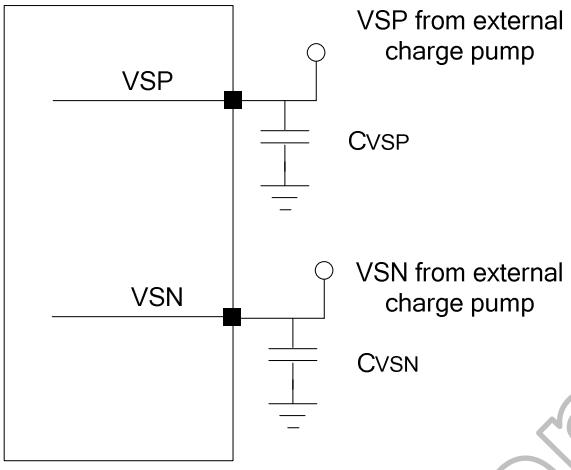


Figure 5.15: VSN and VSP by External Charge Pump

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5.6 Idle display

The HX8379-C supports an idle display mode. The grayscale level to be used is V0 and V255 with R7, G7, B7 decoding, and the other levels (V1-V254) are halted to reduce power consumption. In idle display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

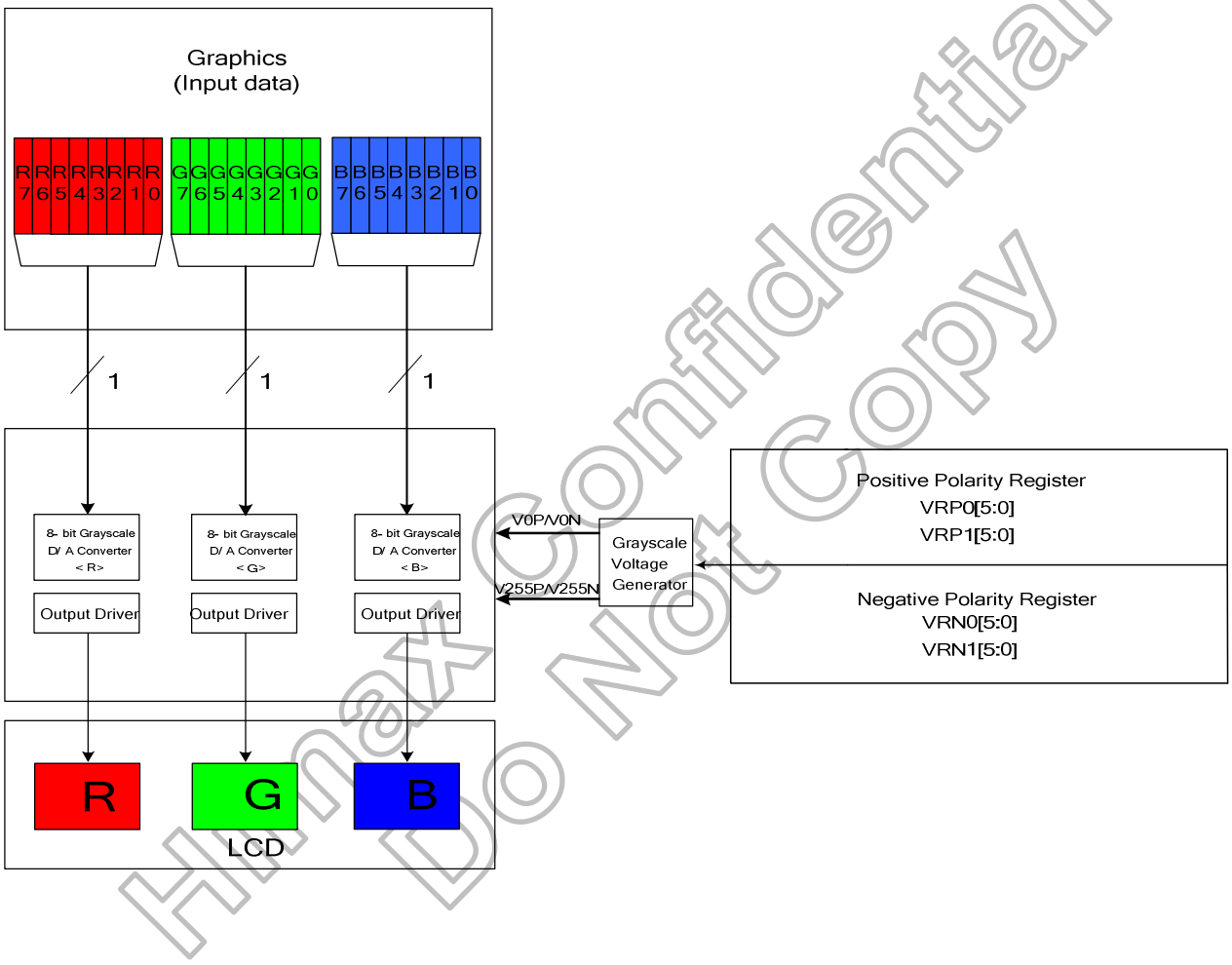
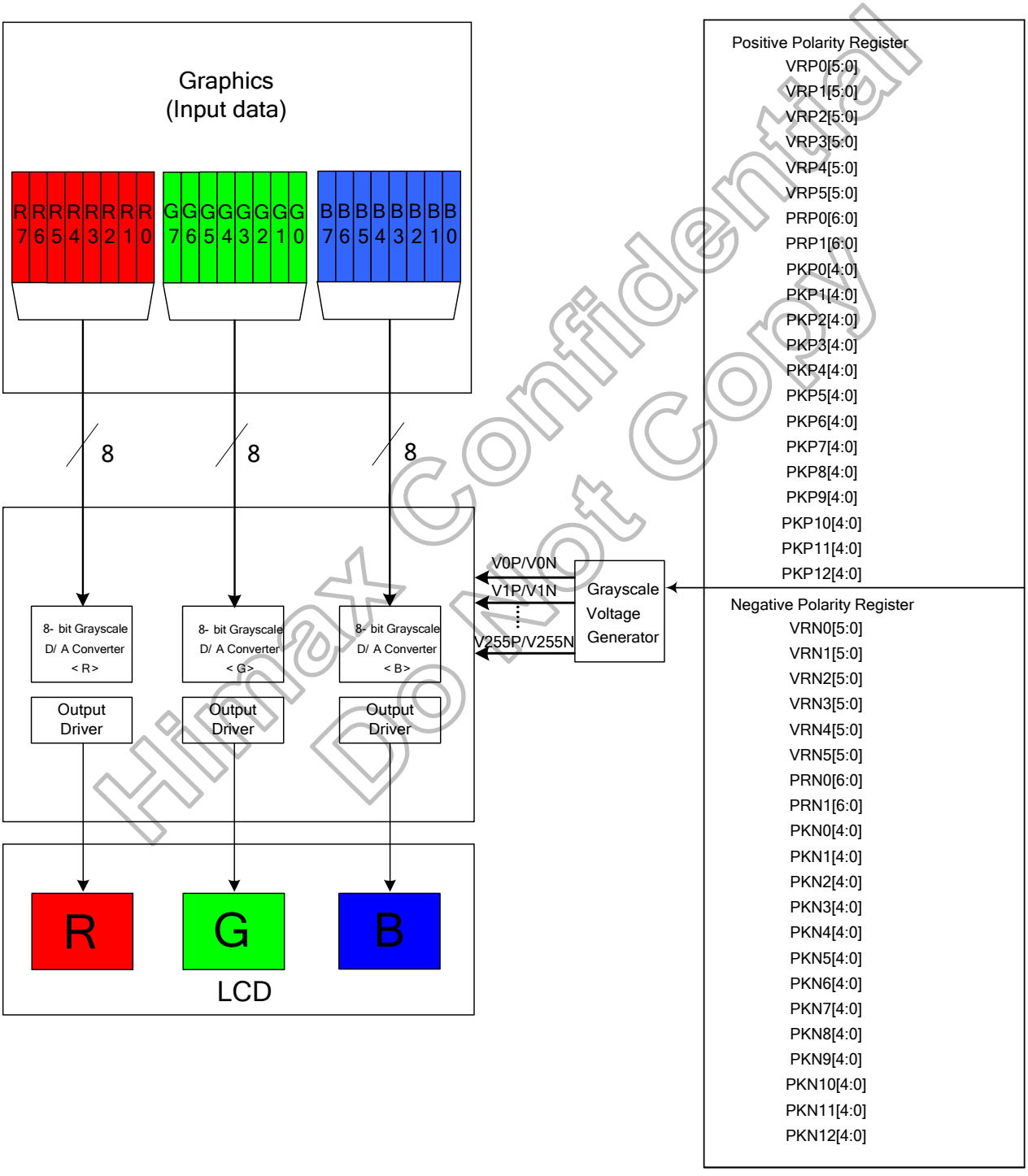


Figure 5.16: Idle Mode Grayscale Control

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5.7 Gamma characteristic correction function

The HX8379-C incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, and B color). Gamma adjustment operation is implemented by deciding the16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.



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Figure 5.17: Grayscale Control

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Gamma-Characteristics adjustment registers

This HX8379-C has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and micro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma micro adjustment registers

The gamma micro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~12), each of which has 5-bits input and generates one reference voltage output.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	88-to-1 selector (voltage level of grayscale 52)
	PRP1 6-0	PRN1 6-0	88-to-1 selector (voltage level of grayscale 204)
Micro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 12)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 40)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 76)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 100)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 132)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 156)
	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 180)
	PKP9 4-0	PKN9 4-0	32-to-1 selector (voltage level of grayscale 216)
	PKP10 4-0	PKN10 4-0	32-to-1 selector (voltage level of grayscale 228)
	PKP11 4-0	PKN11 4-0	32-to-1 selector (voltage level of grayscale 236)
	PKP12 4-0	PKN12 4-0	32-to-1 selector (voltage level of grayscale 243)
Offset Adjustment	VRP0 5-0	VRN0 5-0	64-to-1 selector (voltage level of grayscale 0)
	VRP1 5-0	VRN1 5-0	64-to-1 selector (voltage level of grayscale 4)
	VRP2 5-0	VRN2 5-0	64-to-1 selector (voltage level of grayscale 8)
	VRP3 5-0	VRN3 5-0	64-to-1 selector (voltage level of grayscale 247)
	VRP4 5-0	VRN4 5-0	64-to-1 selector (voltage level of grayscale 251)
	VRP5 5-0	VRN5 5-0	64-to-1 selector (voltage level of grayscale 255)

Table 5.3: Gamma Adjustment Registers

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Gamma resistor stream and selector

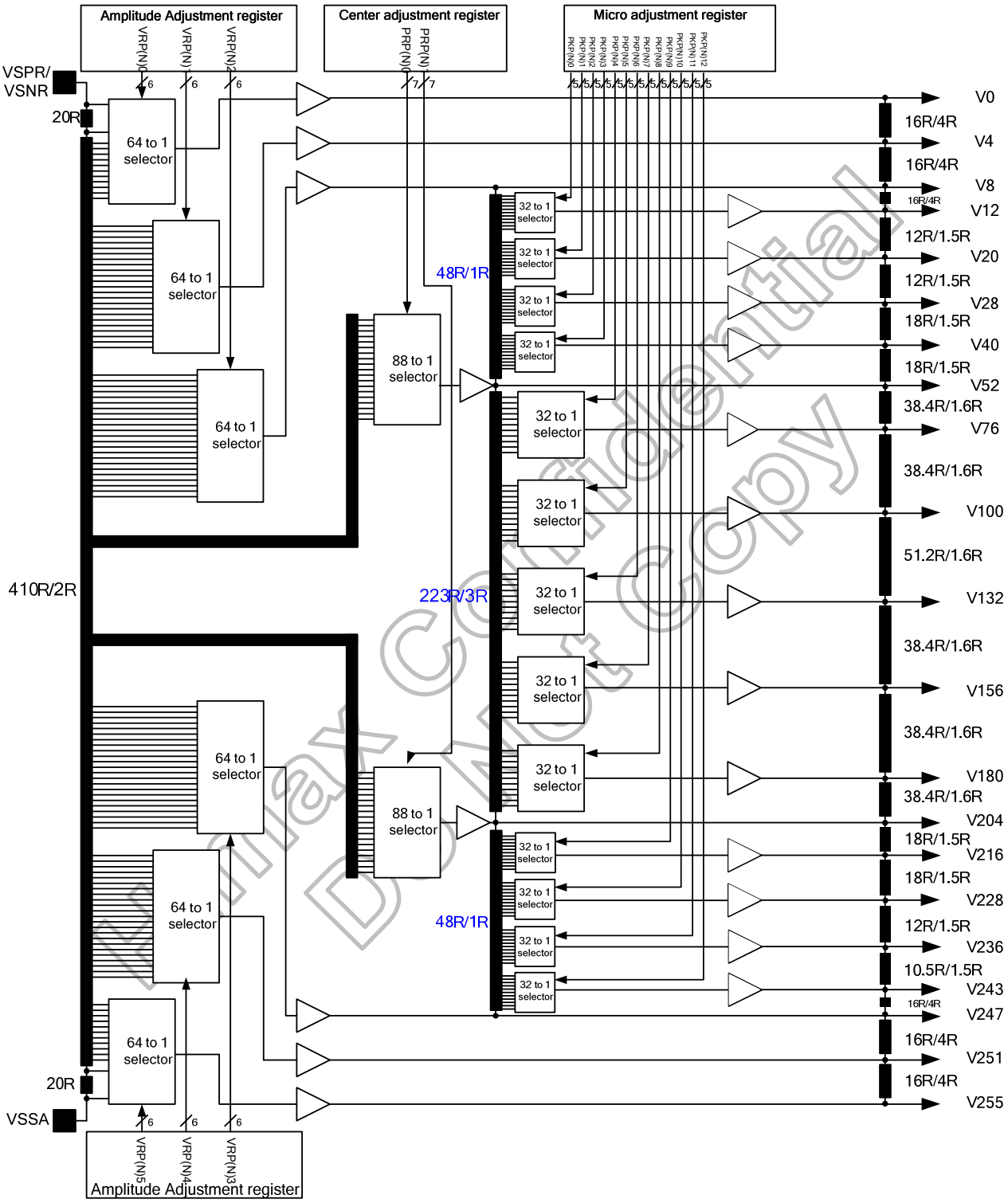


Figure 5.18: Gamma Resistor Stream and Gamma Reference Voltage

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Variable resistor

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0	Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1	Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	20R	000001	2R	000001	2R
000010	22R	000010	4R	000010	4R
000011	24R	000011	6R	000011	6R
•	•	•	•	•	•
•	•	•	•	•	•
011101	76R	011101	58R	011101	58R
011110	78R	011110	60R	011110	60R
011111	80R	011111	62R	011111	62R
100000	82R	100000	64R	100000	64R
100001	84R	100001	66R	100001	66R
100010	86R	100010	68R	100010	68R
•	•	•	•	•	•
•	•	•	•	•	•
111101	140R	111101	122R	111101	122R
111110	142R	111110	124R	111110	124R
111111	144R	111111	126R	111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3	Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4	Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	2R	000001	2R	000001	2R
000010	4R	000010	4R	000010	4R
•	•	•	•	•	•
•	•	•	•	•	•
011101	58R	011101	58R	011101	58R
011110	60R	011110	60R	011110	60R
011111	62R	011111	62R	011111	62R
100000	64R	100000	64R	100000	64R
100001	66R	100001	66R	100001	66R
100010	68R	100010	68R	100010	68R
•	•	•	•	•	•
•	•	•	•	•	•
111100	120R	111100	120R	111100	120R
111101	122R	111101	122R	111101	122R
111110	124R	111110	124R	111110	124R
111111	126R	111111	126R	111111	144R

Table 5.4: Offset Adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0	Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R	0000000	0R
0000001	2R	0000001	2R
0000010	4R	0000010	4R
•	•	•	•
•	•	•	•
1010101	170R	1010101	170R
1010110	172R	1010110	172R
1010111	174R	1010111	174R

Table 5.5: Center Adjustment

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The grayscale levels are determined by the following formulas:

Reference voltage	Micro adjustment value	VinP0 formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * VSPR
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * VSPR
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * VSPR
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * VSPR
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * VSPR
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * VSPR
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * VSPR
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * VSPR
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * VSPR
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * VSPR
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * VSPR
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * VSPR
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * VSPR
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * VSPR
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * VSPR
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * VSPR
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * VSPR
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * VSPR
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * VSPR
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * VSPR
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * VSPR
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * VSPR
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * VSPR
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * VSPR
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * VSPR
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * VSPR
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * VSPR
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * VSPR
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * VSPR
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * VSPR
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * VSPR
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * VSPR
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * VSPR
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * VSPR
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * VSPR
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * VSPR
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * VSPR
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * VSPR
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * VSPR
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * VSPR
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * VSPR
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * VSPR
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * VSPR
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * VSPR
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * VSPR
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * VSPR
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * VSPR
	VRP0 5-0 = 110000	((450R - 114R) / 450R) * VSPR
	VRP0 5-0 = 110001	((450R - 116R) / 450R) * VSPR
	VRP0 5-0 = 110010	((450R - 118R) / 450R) * VSPR
	VRP0 5-0 = 110011	((450R - 120R) / 450R) * VSPR
	VRP0 5-0 = 110100	((450R - 122R) / 450R) * VSPR
	VRP0 5-0 = 110101	((450R - 124R) / 450R) * VSPR
	VRP0 5-0 = 110110	((450R - 126R) / 450R) * VSPR
	VRP0 5-0 = 110111	((450R - 128R) / 450R) * VSPR
	VRP0 5-0 = 111000	((450R - 130R) / 450R) * VSPR
	VRP0 5-0 = 111001	((450R - 132R) / 450R) * VSPR
	VRP0 5-0 = 111010	((450R - 134R) / 450R) * VSPR
	VRP0 5-0 = 111011	((450R - 136R) / 450R) * VSPR
	VRP0 5-0 = 111100	((450R - 138R) / 450R) * VSPR
	VRP0 5-0 = 111101	((450R - 140R) / 450R) * VSPR
	VRP0 5-0 = 111110	((450R - 142R) / 450R) * VSPR
	VRP0 5-0 = 111111	((450R - 144R) / 450R) * VSPR

Table 5.6: VinP0

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Reference voltage	Micro adjustment value	VinP1 formula
VinP1	VRP1 5-0 = 000000	(430R / 450R) * VSPR
	VRP1 5-0 = 000001	((430R - 2R) / 450R) * VSPR
	VRP1 5-0 = 000010	((430R - 4R) / 450R) * VSPR
	VRP1 5-0 = 000011	((430R - 6R) / 450R) * VSPR
	VRP1 5-0 = 000100	((430R - 8R) / 450R) * VSPR
	VRP1 5-0 = 000101	((430R - 10R) / 450R) * VSPR
	VRP1 5-0 = 000110	((430R - 12R) / 450R) * VSPR
	VRP1 5-0 = 000111	((430R - 14R) / 450R) * VSPR
	VRP1 5-0 = 001000	((430R - 16R) / 450R) * VSPR
	VRP1 5-0 = 001001	((430R - 18R) / 450R) * VSPR
	VRP1 5-0 = 001010	((430R - 20R) / 450R) * VSPR
	VRP1 5-0 = 001011	((430R - 22R) / 450R) * VSPR
	VRP1 5-0 = 001100	((430R - 24R) / 450R) * VSPR
	VRP1 5-0 = 001101	((430R - 26R) / 450R) * VSPR
	VRP1 5-0 = 001110	((430R - 28R) / 450R) * VSPR
	VRP1 5-0 = 001111	((430R - 30R) / 450R) * VSPR
	VRP1 5-0 = 010000	((430R - 32R) / 450R) * VSPR
	VRP1 5-0 = 010001	((430R - 34R) / 450R) * VSPR
	VRP1 5-0 = 010010	((430R - 36R) / 450R) * VSPR
	VRP1 5-0 = 010011	((430R - 38R) / 450R) * VSPR
	VRP1 5-0 = 010100	((430R - 40R) / 450R) * VSPR
	VRP1 5-0 = 010101	((430R - 42R) / 450R) * VSPR
	VRP1 5-0 = 010110	((430R - 44R) / 450R) * VSPR
	VRP1 5-0 = 010111	((430R - 46R) / 450R) * VSPR
	VRP1 5-0 = 011000	((430R - 48R) / 450R) * VSPR
	VRP1 5-0 = 011001	((430R - 50R) / 450R) * VSPR
	VRP1 5-0 = 011010	((430R - 52R) / 450R) * VSPR
	VRP1 5-0 = 011011	((430R - 54R) / 450R) * VSPR
	VRP1 5-0 = 011100	((430R - 56R) / 450R) * VSPR
	VRP1 5-0 = 011101	((430R - 58R) / 450R) * VSPR
	VRP1 5-0 = 011110	((430R - 60R) / 450R) * VSPR
	VRP1 5-0 = 011111	((430R - 62R) / 450R) * VSPR
	VRP1 5-0 = 100000	((430R - 64R) / 450R) * VSPR
	VRP1 5-0 = 100001	((430R - 66R) / 450R) * VSPR
	VRP1 5-0 = 100010	((430R - 68R) / 450R) * VSPR
	VRP1 5-0 = 100011	((430R - 70R) / 450R) * VSPR
	VRP1 5-0 = 100100	((430R - 72R) / 450R) * VSPR
	VRP1 5-0 = 100101	((430R - 74R) / 450R) * VSPR
	VRP1 5-0 = 100110	((430R - 76R) / 450R) * VSPR
	VRP1 5-0 = 100111	((430R - 78R) / 450R) * VSPR
	VRP1 5-0 = 101000	((430R - 80R) / 450R) * VSPR
	VRP1 5-0 = 101001	((430R - 82R) / 450R) * VSPR
	VRP1 5-0 = 101010	((430R - 84R) / 450R) * VSPR
	VRP1 5-0 = 101011	((430R - 86R) / 450R) * VSPR
	VRP1 5-0 = 101100	((430R - 88R) / 450R) * VSPR
	VRP1 5-0 = 101101	((430R - 90R) / 450R) * VSPR
	VRP1 5-0 = 101110	((430R - 92R) / 450R) * VSPR
	VRP1 5-0 = 101111	((430R - 94R) / 450R) * VSPR
	VRP1 5-0 = 110000	((430R - 96R) / 450R) * VSPR
	VRP1 5-0 = 110001	((430R - 98R) / 450R) * VSPR
	VRP1 5-0 = 110010	((430R - 100R) / 450R) * VSPR
	VRP1 5-0 = 110011	((430R - 102R) / 450R) * VSPR
	VRP1 5-0 = 110100	((430R - 104R) / 450R) * VSPR
	VRP1 5-0 = 110101	((430R - 106R) / 450R) * VSPR
	VRP1 5-0 = 110110	((430R - 108R) / 450R) * VSPR
	VRP1 5-0 = 110111	((430R - 110R) / 450R) * VSPR
	VRP1 5-0 = 111000	((430R - 112R) / 450R) * VSPR
	VRP1 5-0 = 111001	((430R - 114R) / 450R) * VSPR
	VRP1 5-0 = 111010	((430R - 116R) / 450R) * VSPR
	VRP1 5-0 = 111011	((430R - 118R) / 450R) * VSPR
	VRP1 5-0 = 111100	((430R - 120R) / 450R) * VSPR
	VRP1 5-0 = 111101	((430R - 122R) / 450R) * VSPR
	VRP1 5-0 = 111110	((430R - 124R) / 450R) * VSPR
	VRP1 5-0 = 111111	((430R - 126R) / 450R) * VSPR

Table 5.7: VinP1

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Reference voltage	Micro adjustment value	VinP2 formula
VinP2	VRP2 5-0 = 000000	(420R / 450R) * VSPR
	VRP2 5-0 = 000001	((420R - 2R) / 450R) * VSPR
	VRP2 5-0 = 000010	((420R - 4R) / 450R) * VSPR
	VRP2 5-0 = 000011	((420R - 6R) / 450R) * VSPR
	VRP2 5-0 = 000100	((420R - 8R) / 450R) * VSPR
	VRP2 5-0 = 000101	((420R - 10R) / 450R) * VSPR
	VRP2 5-0 = 000110	((420R - 12R) / 450R) * VSPR
	VRP2 5-0 = 000111	((420R - 14R) / 450R) * VSPR
	VRP2 5-0 = 001000	((420R - 16R) / 450R) * VSPR
	VRP2 5-0 = 001001	((420R - 18R) / 450R) * VSPR
	VRP2 5-0 = 001010	((420R - 20R) / 450R) * VSPR
	VRP2 5-0 = 001011	((420R - 22R) / 450R) * VSPR
	VRP2 5-0 = 001100	((420R - 24R) / 450R) * VSPR
	VRP2 5-0 = 001101	((420R - 26R) / 450R) * VSPR
	VRP2 5-0 = 001110	((420R - 28R) / 450R) * VSPR
	VRP2 5-0 = 001111	((420R - 30R) / 450R) * VSPR
	VRP2 5-0 = 010000	((420R - 32R) / 450R) * VSPR
	VRP2 5-0 = 010001	((420R - 34R) / 450R) * VSPR
	VRP2 5-0 = 010010	((420R - 36R) / 450R) * VSPR
	VRP2 5-0 = 010011	((420R - 38R) / 450R) * VSPR
	VRP2 5-0 = 010100	((420R - 40R) / 450R) * VSPR
	VRP2 5-0 = 010101	((420R - 42R) / 450R) * VSPR
	VRP2 5-0 = 010110	((420R - 44R) / 450R) * VSPR
	VRP2 5-0 = 010111	((420R - 46R) / 450R) * VSPR
	VRP2 5-0 = 011000	((420R - 48R) / 450R) * VSPR
	VRP2 5-0 = 011001	((420R - 50R) / 450R) * VSPR
	VRP2 5-0 = 011010	((420R - 52R) / 450R) * VSPR
	VRP2 5-0 = 011011	((420R - 54R) / 450R) * VSPR
	VRP2 5-0 = 011100	((420R - 56R) / 450R) * VSPR
	VRP2 5-0 = 011101	((420R - 58R) / 450R) * VSPR
	VRP2 5-0 = 011110	((420R - 60R) / 450R) * VSPR
	VRP2 5-0 = 011111	((420R - 62R) / 450R) * VSPR
	VRP2 5-0 = 100000	((420R - 64R) / 450R) * VSPR
	VRP2 5-0 = 100001	((420R - 66R) / 450R) * VSPR
	VRP2 5-0 = 100010	((420R - 68R) / 450R) * VSPR
	VRP2 5-0 = 100011	((420R - 70R) / 450R) * VSPR
	VRP2 5-0 = 100100	((420R - 72R) / 450R) * VSPR
	VRP2 5-0 = 100101	((420R - 74R) / 450R) * VSPR
	VRP2 5-0 = 100110	((420R - 76R) / 450R) * VSPR
	VRP2 5-0 = 100111	((420R - 78R) / 450R) * VSPR
	VRP2 5-0 = 101000	((420R - 80R) / 450R) * VSPR
	VRP2 5-0 = 101001	((420R - 82R) / 450R) * VSPR
	VRP2 5-0 = 101010	((420R - 84R) / 450R) * VSPR
	VRP2 5-0 = 101011	((420R - 86R) / 450R) * VSPR
	VRP2 5-0 = 101100	((420R - 88R) / 450R) * VSPR
	VRP2 5-0 = 101101	((420R - 90R) / 450R) * VSPR
	VRP2 5-0 = 101110	((420R - 92R) / 450R) * VSPR
	VRP2 5-0 = 101111	((420R - 94R) / 450R) * VSPR
	VRP2 5-0 = 110000	((420R - 96R) / 450R) * VSPR
	VRP2 5-0 = 110001	((420R - 98R) / 450R) * VSPR
	VRP2 5-0 = 110010	((420R - 100R) / 450R) * VSPR
	VRP2 5-0 = 110011	((420R - 102R) / 450R) * VSPR
	VRP2 5-0 = 110100	((420R - 104R) / 450R) * VSPR
	VRP2 5-0 = 110101	((420R - 106R) / 450R) * VSPR
	VRP2 5-0 = 110110	((420R - 108R) / 450R) * VSPR
	VRP2 5-0 = 110111	((420R - 110R) / 450R) * VSPR
	VRP2 5-0 = 111000	((420R - 112R) / 450R) * VSPR
	VRP2 5-0 = 111001	((420R - 114R) / 450R) * VSPR
	VRP2 5-0 = 111010	((420R - 116R) / 450R) * VSPR
	VRP2 5-0 = 111011	((420R - 118R) / 450R) * VSPR
	VRP2 5-0 = 111100	((420R - 120R) / 450R) * VSPR
	VRP2 5-0 = 111101	((420R - 122R) / 450R) * VSPR
	VRP2 5-0 = 111110	((420R - 124R) / 450R) * VSPR
	VRP2 5-0 = 111111	((420R - 126R) / 450R) * VSPR

Table 5.8: VinP2

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Reference voltage	Micro adjustment value	VinP18 formula
VinP18	VRP3 5-0 = 000000	(156R / 450R) * VSPR
	VRP3 5-0 = 000001	((156R - 2R) / 450R) * VSPR
	VRP3 5-0 = 000010	((156R - 4R) / 450R) * VSPR
	VRP3 5-0 = 000011	((156R - 6R) / 450R) * VSPR
	VRP3 5-0 = 000100	((156R - 8R) / 450R) * VSPR
	VRP3 5-0 = 000101	((156R - 10R) / 450R) * VSPR
	VRP3 5-0 = 000110	((156R - 12R) / 450R) * VSPR
	VRP3 5-0 = 000111	((156R - 14R) / 450R) * VSPR
	VRP3 5-0 = 001000	((156R - 16R) / 450R) * VSPR
	VRP3 5-0 = 001001	((156R - 18R) / 450R) * VSPR
	VRP3 5-0 = 001010	((156R - 20R) / 450R) * VSPR
	VRP3 5-0 = 001011	((156R - 22R) / 450R) * VSPR
	VRP3 5-0 = 001100	((156R - 24R) / 450R) * VSPR
	VRP3 5-0 = 001101	((156R - 26R) / 450R) * VSPR
	VRP3 5-0 = 001110	((156R - 28R) / 450R) * VSPR
	VRP3 5-0 = 001111	((156R - 30R) / 450R) * VSPR
	VRP3 5-0 = 010000	((156R - 32R) / 450R) * VSPR
	VRP3 5-0 = 010001	((156R - 34R) / 450R) * VSPR
	VRP3 5-0 = 010010	((156R - 36R) / 450R) * VSPR
	VRP3 5-0 = 010011	((156R - 38R) / 450R) * VSPR
	VRP3 5-0 = 010100	((156R - 40R) / 450R) * VSPR
	VRP3 5-0 = 010101	((156R - 42R) / 450R) * VSPR
	VRP3 5-0 = 010110	((156R - 44R) / 450R) * VSPR
	VRP3 5-0 = 010111	((156R - 46R) / 450R) * VSPR
	VRP3 5-0 = 011000	((156R - 48R) / 450R) * VSPR
	VRP3 5-0 = 011001	((156R - 50R) / 450R) * VSPR
	VRP3 5-0 = 011010	((156R - 52R) / 450R) * VSPR
	VRP3 5-0 = 011011	((156R - 54R) / 450R) * VSPR
	VRP3 5-0 = 011100	((156R - 56R) / 450R) * VSPR
	VRP3 5-0 = 011101	((156R - 58R) / 450R) * VSPR
	VRP3 5-0 = 011110	((156R - 60R) / 450R) * VSPR
	VRP3 5-0 = 011111	((156R - 62R) / 450R) * VSPR
	VRP3 5-0 = 100000	((156R - 64R) / 450R) * VSPR
	VRP3 5-0 = 100001	((156R - 66R) / 450R) * VSPR
	VRP3 5-0 = 100010	((156R - 68R) / 450R) * VSPR
	VRP3 5-0 = 100011	((156R - 70R) / 450R) * VSPR
	VRP3 5-0 = 100100	((156R - 72R) / 450R) * VSPR
	VRP3 5-0 = 100101	((156R - 74R) / 450R) * VSPR
	VRP3 5-0 = 100110	((156R - 76R) / 450R) * VSPR
	VRP3 5-0 = 100111	((156R - 78R) / 450R) * VSPR
	VRP3 5-0 = 101000	((156R - 80R) / 450R) * VSPR
	VRP3 5-0 = 101001	((156R - 82R) / 450R) * VSPR
	VRP3 5-0 = 101010	((156R - 84R) / 450R) * VSPR
	VRP3 5-0 = 101011	((156R - 86R) / 450R) * VSPR
	VRP3 5-0 = 101100	((156R - 88R) / 450R) * VSPR
	VRP3 5-0 = 101101	((156R - 90R) / 450R) * VSPR
	VRP3 5-0 = 101110	((156R - 92R) / 450R) * VSPR
	VRP3 5-0 = 101111	((156R - 94R) / 450R) * VSPR
	VRP3 5-0 = 110000	((156R - 96R) / 450R) * VSPR
	VRP3 5-0 = 110001	((156R - 98R) / 450R) * VSPR
	VRP3 5-0 = 110010	((156R - 100R) / 450R) * VSPR
	VRP3 5-0 = 110011	((156R - 102R) / 450R) * VSPR
	VRP3 5-0 = 110100	((156R - 104R) / 450R) * VSPR
	VRP3 5-0 = 110101	((156R - 106R) / 450R) * VSPR
	VRP3 5-0 = 110110	((156R - 108R) / 450R) * VSPR
	VRP3 5-0 = 110111	((156R - 110R) / 450R) * VSPR
	VRP3 5-0 = 111000	((156R - 112R) / 450R) * VSPR
	VRP3 5-0 = 111001	((156R - 114R) / 450R) * VSPR
	VRP3 5-0 = 111010	((156R - 116R) / 450R) * VSPR
	VRP3 5-0 = 111011	((156R - 118R) / 450R) * VSPR
	VRP3 5-0 = 111100	((156R - 120R) / 450R) * VSPR
	VRP3 5-0 = 111101	((156R - 122R) / 450R) * VSPR
	VRP3 5-0 = 111110	((156R - 124R) / 450R) * VSPR
	VRP3 5-0 = 111111	((156R - 126R) / 450R) * VSPR

Table 5.9: VinP18

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Do Not Spread

Reference voltage	Micro adjustment value	VinP19 formula
VinP19	VRP4 5-0 = 000000	(146R / 450R) * VSPR
	VRP4 5-0 = 000001	((146R - 2R) / 450R) * VSPR
	VRP4 5-0 = 000010	((146R - 4R) / 450R) * VSPR
	VRP4 5-0 = 000011	((146R - 6R) / 450R) * VSPR
	VRP4 5-0 = 000100	((146R - 8R) / 450R) * VSPR
	VRP4 5-0 = 000101	((146R - 10R) / 450R) * VSPR
	VRP4 5-0 = 000110	((146R - 12R) / 450R) * VSPR
	VRP4 5-0 = 000111	((146R - 14R) / 450R) * VSPR
	VRP4 5-0 = 001000	((146R - 16R) / 450R) * VSPR
	VRP4 5-0 = 001001	((146R - 18R) / 450R) * VSPR
	VRP4 5-0 = 001010	((146R - 20R) / 450R) * VSPR
	VRP4 5-0 = 001011	((146R - 22R) / 450R) * VSPR
	VRP4 5-0 = 001100	((146R - 24R) / 450R) * VSPR
	VRP4 5-0 = 001101	((146R - 26R) / 450R) * VSPR
	VRP4 5-0 = 001110	((146R - 28R) / 450R) * VSPR
	VRP4 5-0 = 001111	((146R - 30R) / 450R) * VSPR
	VRP4 5-0 = 010000	((146R - 32R) / 450R) * VSPR
	VRP4 5-0 = 010001	((146R - 34R) / 450R) * VSPR
	VRP4 5-0 = 010010	((146R - 36R) / 450R) * VSPR
	VRP4 5-0 = 010011	((146R - 38R) / 450R) * VSPR
	VRP4 5-0 = 010100	((146R - 40R) / 450R) * VSPR
	VRP4 5-0 = 010101	((146R - 42R) / 450R) * VSPR
	VRP4 5-0 = 010110	((146R - 44R) / 450R) * VSPR
	VRP4 5-0 = 010111	((146R - 46R) / 450R) * VSPR
	VRP4 5-0 = 011000	((146R - 48R) / 450R) * VSPR
	VRP4 5-0 = 011001	((146R - 50R) / 450R) * VSPR
	VRP4 5-0 = 011010	((146R - 52R) / 450R) * VSPR
	VRP4 5-0 = 011011	((146R - 54R) / 450R) * VSPR
	VRP4 5-0 = 011100	((146R - 56R) / 450R) * VSPR
	VRP4 5-0 = 011101	((146R - 58R) / 450R) * VSPR
	VRP4 5-0 = 011110	((146R - 60R) / 450R) * VSPR
	VRP4 5-0 = 011111	((146R - 62R) / 450R) * VSPR
	VRP4 5-0 = 100000	((146R - 64R) / 450R) * VSPR
	VRP4 5-0 = 100001	((146R - 66R) / 450R) * VSPR
	VRP4 5-0 = 100010	((146R - 68R) / 450R) * VSPR
	VRP4 5-0 = 100011	((146R - 70R) / 450R) * VSPR
	VRP4 5-0 = 100100	((146R - 72R) / 450R) * VSPR
	VRP4 5-0 = 100101	((146R - 74R) / 450R) * VSPR
	VRP4 5-0 = 100110	((146R - 76R) / 450R) * VSPR
	VRP4 5-0 = 100111	((146R - 78R) / 450R) * VSPR
	VRP4 5-0 = 101000	((146R - 80R) / 450R) * VSPR
	VRP4 5-0 = 101001	((146R - 82R) / 450R) * VSPR
	VRP4 5-0 = 101010	((146R - 84R) / 450R) * VSPR
	VRP4 5-0 = 101011	((146R - 86R) / 450R) * VSPR
	VRP4 5-0 = 101100	((146R - 88R) / 450R) * VSPR
	VRP4 5-0 = 101101	((146R - 90R) / 450R) * VSPR
	VRP4 5-0 = 101110	((146R - 92R) / 450R) * VSPR
	VRP4 5-0 = 101111	((146R - 94R) / 450R) * VSPR
	VRP4 5-0 = 110000	((146R - 96R) / 450R) * VSPR
	VRP4 5-0 = 110001	((146R - 98R) / 450R) * VSPR
	VRP4 5-0 = 110010	((146R - 100R) / 450R) * VSPR
	VRP4 5-0 = 110011	((146R - 102R) / 450R) * VSPR
	VRP4 5-0 = 110100	((146R - 104R) / 450R) * VSPR
	VRP4 5-0 = 110101	((146R - 106R) / 450R) * VSPR
	VRP4 5-0 = 110110	((146R - 108R) / 450R) * VSPR
	VRP4 5-0 = 110111	((146R - 110R) / 450R) * VSPR
	VRP4 5-0 = 111000	((146R - 112R) / 450R) * VSPR
	VRP4 5-0 = 111001	((146R - 114R) / 450R) * VSPR
	VRP4 5-0 = 111010	((146R - 116R) / 450R) * VSPR
	VRP4 5-0 = 111011	((146R - 118R) / 450R) * VSPR
	VRP4 5-0 = 111100	((146R - 120R) / 450R) * VSPR
	VRP4 5-0 = 111101	((146R - 122R) / 450R) * VSPR
	VRP4 5-0 = 111110	((146R - 124R) / 450R) * VSPR
	VRP4 5-0 = 111111	((146R - 126R) / 450R) * VSPR

Table 5.10: VinP19

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Reference voltage	Micro adjustment value	VinP20 formula
VinP20	VRP5 5-0 = 000000	(144R / 450R) * VSPR
	VRP5 5-0 = 000001	((144R - 2R) / 450R) * VSPR
	VRP5 5-0 = 000010	((144R - 4R) / 450R) * VSPR
	VRP5 5-0 = 000011	((144R - 6R) / 450R) * VSPR
	VRP5 5-0 = 000100	((144R - 8R) / 450R) * VSPR
	VRP5 5-0 = 000101	((144R - 10R) / 450R) * VSPR
	VRP5 5-0 = 000110	((144R - 12R) / 450R) * VSPR
	VRP5 5-0 = 000111	((144R - 14R) / 450R) * VSPR
	VRP5 5-0 = 001000	((144R - 16R) / 450R) * VSPR
	VRP5 5-0 = 001001	((144R - 18R) / 450R) * VSPR
	VRP5 5-0 = 001010	((144R - 20R) / 450R) * VSPR
	VRP5 5-0 = 001011	((144R - 22R) / 450R) * VSPR
	VRP5 5-0 = 001100	((144R - 24R) / 450R) * VSPR
	VRP5 5-0 = 001101	((144R - 26R) / 450R) * VSPR
	VRP5 5-0 = 001110	((144R - 28R) / 450R) * VSPR
	VRP5 5-0 = 001111	((144R - 30R) / 450R) * VSPR
	VRP5 5-0 = 010000	((144R - 32R) / 450R) * VSPR
	VRP5 5-0 = 010001	((144R - 34R) / 450R) * VSPR
	VRP5 5-0 = 010010	((144R - 36R) / 450R) * VSPR
	VRP5 5-0 = 010011	((144R - 38R) / 450R) * VSPR
	VRP5 5-0 = 010100	((144R - 40R) / 450R) * VSPR
	VRP5 5-0 = 010101	((144R - 42R) / 450R) * VSPR
	VRP5 5-0 = 010110	((144R - 44R) / 450R) * VSPR
	VRP5 5-0 = 010111	((144R - 46R) / 450R) * VSPR
	VRP5 5-0 = 011000	((144R - 48R) / 450R) * VSPR
	VRP5 5-0 = 011001	((144R - 50R) / 450R) * VSPR
	VRP5 5-0 = 011010	((144R - 52R) / 450R) * VSPR
	VRP5 5-0 = 011011	((144R - 54R) / 450R) * VSPR
	VRP5 5-0 = 011100	((144R - 56R) / 450R) * VSPR
	VRP5 5-0 = 011101	((144R - 58R) / 450R) * VSPR
	VRP5 5-0 = 011110	((144R - 60R) / 450R) * VSPR
	VRP5 5-0 = 011111	((144R - 62R) / 450R) * VSPR
	VRP5 5-0 = 100000	((144R - 64R) / 450R) * VSPR
	VRP5 5-0 = 100001	((144R - 66R) / 450R) * VSPR
	VRP5 5-0 = 100010	((144R - 68R) / 450R) * VSPR
	VRP5 5-0 = 100011	((144R - 70R) / 450R) * VSPR
	VRP5 5-0 = 100100	((144R - 72R) / 450R) * VSPR
	VRP5 5-0 = 100101	((144R - 74R) / 450R) * VSPR
	VRP5 5-0 = 100110	((144R - 76R) / 450R) * VSPR
	VRP5 5-0 = 100111	((144R - 78R) / 450R) * VSPR
	VRP5 5-0 = 101000	((144R - 80R) / 450R) * VSPR
	VRP5 5-0 = 101001	((144R - 82R) / 450R) * VSPR
	VRP5 5-0 = 101010	((144R - 84R) / 450R) * VSPR
	VRP5 5-0 = 101011	((144R - 86R) / 450R) * VSPR
	VRP5 5-0 = 101100	((144R - 88R) / 450R) * VSPR
	VRP5 5-0 = 101101	((144R - 90R) / 450R) * VSPR
	VRP5 5-0 = 101110	((144R - 92R) / 450R) * VSPR
	VRP5 5-0 = 101111	((144R - 94R) / 450R) * VSPR
	VRP5 5-0 = 110000	((144R - 96R) / 450R) * VSPR
	VRP5 5-0 = 110001	((144R - 98R) / 450R) * VSPR
	VRP5 5-0 = 110010	((144R - 100R) / 450R) * VSPR
	VRP5 5-0 = 110011	((144R - 102R) / 450R) * VSPR
	VRP5 5-0 = 110100	((144R - 104R) / 450R) * VSPR
	VRP5 5-0 = 110101	((144R - 106R) / 450R) * VSPR
	VRP5 5-0 = 110110	((144R - 108R) / 450R) * VSPR
	VRP5 5-0 = 110111	((144R - 110R) / 450R) * VSPR
	VRP5 5-0 = 111000	((144R - 112R) / 450R) * VSPR
	VRP5 5-0 = 111001	((144R - 114R) / 450R) * VSPR
	VRP5 5-0 = 111010	((144R - 116R) / 450R) * VSPR
	VRP5 5-0 = 111011	((144R - 118R) / 450R) * VSPR
	VRP5 5-0 = 111100	((144R - 120R) / 450R) * VSPR
	VRP5 5-0 = 111101	((144R - 122R) / 450R) * VSPR
	VRP5 5-0 = 111110	((144R - 124R) / 450R) * VSPR
	VRP5 5-0 = 111111	VGSP

Table 5.11: VinP20

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Reference voltage	Micro adjustment value	VinP7 formula
VinP7	PRP0 6-0 = 0000000	(350R / 450R) VSPR
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * VSPR
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * VSPR
	PRP0 6-0 = 0000011	((350R – 6R) / 450R) * VSPR
	PRP0 6-0 = 0000100	((350R – 8R) / 450R) * VSPR
	PRP0 6-0 = 0000101	((350R – 10R) / 450R) * VSPR
	PRP0 6-0 = 0000110	((350R – 12R) / 450R) * VSPR
	PRP0 6-0 = 0000111	((350R - 14R) / 450R) * VSPR
	PRP0 6-0 = 0001000	((350R – 16R) / 450R) * VSPR
	PRP0 6-0 = 0001001	((350R – 18R) / 450R) * VSPR
	PRP0 6-0 = 0001010	((350R – 20R) / 450R) * VSPR
	PRP0 6-0 = 0001011	((350R – 22R) / 450R) * VSPR
	PRP0 6-0 = 0001100	((350R – 24R) / 450R) * VSPR
	PRP0 6-0 = 0001101	((350R – 26R) / 450R) * VSPR
	PRP0 6-0 = 0001110	((350R – 28R) / 450R) * VSPR
	PRP0 6-0 = 0001111	((350R – 30R) / 450R) * VSPR
	PRP0 6-0 = 0010000	((350R – 32R) / 450R) * VSPR
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * VSPR
	PRP0 6-0 = 0010010	((350R – 36R) / 450R) * VSPR
	PRP0 6-0 = 0010011	((350R – 38R) / 450R) * VSPR
	PRP0 6-0 = 0010100	((350R – 40R) / 450R) * VSPR
	PRP0 6-0 = 0010101	((350R – 42R) / 450R) * VSPR
	PRP0 6-0 = 0010110	((350R – 44R) / 450R) * VSPR
	PRP0 6-0 = 0010111	((350R – 46R) / 450R) * VSPR
	PRP0 6-0 = 0011000	((350R – 48R) / 450R) * VSPR
	PRP0 6-0 = 0011001	((350R – 50R) / 450R) * VSPR
	PRP0 6-0 = 0011010	((350R – 52R) / 450R) * VSPR
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * VSPR
	PRP0 6-0 = 0011100	((350R – 56R) / 450R) * VSPR
	PRP0 6-0 = 0011101	((350R – 58R) / 450R) * VSPR
	PRP0 6-0 = 0011110	((350R – 60R) / 450R) * VSPR
	PRP0 6-0 = 0011111	((350R – 62R) / 450R) * VSPR
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * VSPR
	PRP0 6-0 = 0100001	((350R – 66R) / 450R) * VSPR
	PRP0 6-0 = 0100010	((350R – 68R) / 450R) * VSPR
	PRP0 6-0 = 0100011	((350R – 70R) / 450R) * VSPR
	PRP0 6-0 = 0100100	((350R – 72R) / 450R) * VSPR
	PRP0 6-0 = 0100101	((350R – 74R) / 450R) * VSPR
	PRP0 6-0 = 0100110	((350R – 76R) / 450R) * VSPR
	PRP0 6-0 = 0100111	((350R – 78R) / 450R) * VSPR
	PRP0 6-0 = 0101000	((350R – 80R) / 450R) * VSPR
	PRP0 6-0 = 0101001	((350R – 82R) / 450R) * VSPR
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * VSPR
	PRP0 6-0 = 0101011	((350R – 86R) / 450R) * VSPR
	PRP0 6-0 = 0101100	((350R – 88R) / 450R) * VSPR
	PRP0 6-0 = 0101101	((350R – 90R) / 450R) * VSPR
	PRP0 6-0 = 0101110	((350R – 92R) / 450R) * VSPR
	PRP0 6-0 = 0101111	((350R – 94R) / 450R) * VSPR
	PRP0 6-0 = 0110000	((350R – 96R) / 450R) * VSPR
	PRP0 6-0 = 0110001	((350R – 98R) / 450R) * VSPR
	PRP0 6-0 = 0110010	((350R – 100R) / 450R) * VSPR
	PRP0 6-0 = 0110011	((350R – 102R) / 450R) * VSPR
	PRP0 6-0 = 0110100	((350R – 104R) / 450R) * VSPR
	PRP0 6-0 = 0110101	((350R – 106R) / 450R) * VSPR
	PRP0 6-0 = 0110110	((350R – 108R) / 450R) * VSPR
	PRP0 6-0 = 0110111	((350R – 110R) / 450R) * VSPR
	PRP0 6-0 = 0111000	((350R – 112R) / 450R) * VSPR
	PRP0 6-0 = 0111001	((350R – 114R) / 450R) * VSPR
	PRP0 6-0 = 0111010	((350R – 116R) / 450R) * VSPR
	PRP0 6-0 = 0111011	((350R – 118R) / 450R) * VSPR
	PRP0 6-0 = 0111100	((350R – 120R) / 450R) * VSPR
	PRP0 6-0 = 0111101	((350R – 122R) / 450R) * VSPR
	PRP0 6-0 = 0111110	((350R - 124R) / 450R) * VSPR
	PRP0 6-0 = 0111111	((350R – 126R) / 450R) * VSPR
	PRP0 6-0 = 1000000	((350R – 128R) / 450R) * VSPR
	PRP0 6-0 = 1000001	((350R – 130R) / 450R) * VSPR
	PRP0 6-0 = 1000010	((350R - 132R) / 450R) * VSPR
	PRP0 6-0 = 1000011	((350R – 134R) / 450R) * VSPR
	PRP0 6-0 = 1000100	((350R – 136R) / 450R) * VSPR

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Reference voltage	Micro adjustment value	VinP7 formula
	PRP0 6-0 = 1000101	((350R – 138R) / 450R) * VSPR
	PRP0 6-0 = 1000110	((350R – 140R) / 450R) * VSPR
	PRP0 6-0 = 1000111	((350R – 142R) / 450R) * VSPR
	PRP0 6-0 = 1001000	((350R – 144R) / 450R) * VSPR
	PRP0 6-0 = 1001001	((350R – 146R) / 450R) * VSPR
	PRP0 6-0 = 1001010	((350R – 148R) / 450R) * VSPR
	PRP0 6-0 = 1001011	((350R – 150R) / 450R) * VSPR
	PRP0 6-0 = 1001100	((350R - 152R) / 450R) * VSPR
	PRP0 6-0 = 1001101	((350R – 154R) / 450R) * VSPR
	PRP0 6-0 = 1001110	((350R – 156R) / 450R) * VSPR
	PRP0 6-0 = 1001111	((350R – 158R) / 450R) * VSPR
	PRP0 6-0 = 1010000	((350R – 160R) / 450R) * VSPR
	PRP0 6-0 = 1010001	((350R – 162R) / 450R) * VSPR
	PRP0 6-0 = 1010010	((350R – 164R) / 450R) * VSPR
	PRP0 6-0 = 1010011	((350R – 166R) / 450R) * VSPR
	PRP0 6-0 = 1010100	((350R – 168R) / 450R) * VSPR
	PRP0 6-0 = 1010101	((350R – 170R) / 450R) * VSPR
	PRP0 6-0 = 1010110	((350R – 172R) / 450R) * VSPR
	PRP0 6-0 = 1010111	((350R - 174R) / 450R) * VSPR
	PRP0 6-0 = 1011000	inhibit
	PRP0 6-0 = 1011001	inhibit
	PRP0 6-0 = 1011010	inhibit
	PRP0 6-0 = 1011011	inhibit
	PRP0 6-0 = 1011100	inhibit
	PRP0 6-0 = 1011101	inhibit
	PRP0 6-0 = 1011110	inhibit
	PRP0 6-0 = 1011111	inhibit
	PRP0 6-0 = 1100000	inhibit
	PRP0 6-0 = 1100001	inhibit
	PRP0 6-0 = 1100010	inhibit
	PRP0 6-0 = 1100011	inhibit
	PRP0 6-0 = 1100100	inhibit
	PRP0 6-0 = 1100101	inhibit
	PRP0 6-0 = 1100110	inhibit
	PRP0 6-0 = 1100111	inhibit
	PRP0 6-0 = 1101000	inhibit
	PRP0 6-0 = 1101001	inhibit
	PRP0 6-0 = 1101010	inhibit
	PRP0 6-0 = 1101011	inhibit
	PRP0 6-0 = 1101100	inhibit
	PRP0 6-0 = 1101101	inhibit
	PRP0 6-0 = 1101110	inhibit
	PRP0 6-0 = 1101111	inhibit
	PRP0 6-0 = 1110000	inhibit
	PRP0 6-0 = 1110001	inhibit
	PRP0 6-0 = 1110010	inhibit
	PRP0 6-0 = 1110011	inhibit
	PRP0 6-0 = 1110100	inhibit
	PRP0 6-0 = 1110101	inhibit
	PRP0 6-0 = 1110110	inhibit
	PRP0 6-0 = 1110111	inhibit
	PRP0 6-0 = 1111000	inhibit
	PRP0 6-0 = 1111001	inhibit
	PRP0 6-0 = 1111010	inhibit
	PRP0 6-0 = 1111011	inhibit
	PRP0 6-0 = 1111100	inhibit
	PRP0 6-0 = 1111101	inhibit
	PRP0 6-0 = 1111110	inhibit
	PRP0 6-0 = 1111111	inhibit

Table 5.12: VinP7

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Reference voltage	Micro adjustment value	VinP13 formula
VinP13	PRP1 6-0 = 0000000	(274R / 450R) VSPR
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * VSPR
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * VSPR
	PRP1 6-0 = 0000011	((274R – 6R) / 450R) * VSPR
	PRP1 6-0 = 0000100	((274R – 8R) / 450R) * VSPR
	PRP1 6-0 = 0000101	((274R – 10R) / 450R) * VSPR
	PRP1 6-0 = 0000110	((274R – 12R) / 450R) * VSPR
	PRP1 6-0 = 0000111	((274R - 14R) / 450R) * VSPR
	PRP1 6-0 = 0001000	((274R – 16R) / 450R) * VSPR
	PRP1 6-0 = 0001001	((274R – 18R) / 450R) * VSPR
	PRP1 6-0 = 0001010	((274R – 20R) / 450R) * VSPR
	PRP1 6-0 = 0001011	((274R – 22R) / 450R) * VSPR
	PRP1 6-0 = 0001100	((274R – 24R) / 450R) * VSPR
	PRP1 6-0 = 0001101	((274R – 26R) / 450R) * VSPR
	PRP1 6-0 = 0001110	((274R – 28R) / 450R) * VSPR
	PRP1 6-0 = 0001111	((274R – 30R) / 450R) * VSPR
	PRP1 6-0 = 0010000	((274R – 32R) / 450R) * VSPR
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * VSPR
	PRP1 6-0 = 0010010	((274R – 36R) / 450R) * VSPR
	PRP1 6-0 = 0010011	((274R – 38R) / 450R) * VSPR
	PRP1 6-0 = 0010100	((274R – 40R) / 450R) * VSPR
	PRP1 6-0 = 0010101	((274R – 42R) / 450R) * VSPR
	PRP1 6-0 = 0010110	((274R – 44R) / 450R) * VSPR
	PRP1 6-0 = 0010111	((274R – 46R) / 450R) * VSPR
	PRP1 6-0 = 0011000	((274R – 48R) / 450R) * VSPR
	PRP1 6-0 = 0011001	((274R – 50R) / 450R) * VSPR
	PRP1 6-0 = 0011010	((274R – 52R) / 450R) * VSPR
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * VSPR
	PRP1 6-0 = 0011100	((274R – 56R) / 450R) * VSPR
	PRP1 6-0 = 0011101	((274R – 58R) / 450R) * VSPR
	PRP1 6-0 = 0011110	((274R – 60R) / 450R) * VSPR
	PRP1 6-0 = 0011111	((274R – 62R) / 450R) * VSPR
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * VSPR
	PRP1 6-0 = 0100001	((274R – 66R) / 450R) * VSPR
	PRP1 6-0 = 0100010	((274R – 68R) / 450R) * VSPR
	PRP1 6-0 = 0100011	((274R – 70R) / 450R) * VSPR
	PRP1 6-0 = 0100100	((274R – 72R) / 450R) * VSPR
	PRP1 6-0 = 0100101	((274R – 74R) / 450R) * VSPR
	PRP1 6-0 = 0100110	((274R – 76R) / 450R) * VSPR
	PRP1 6-0 = 0100111	((274R – 78R) / 450R) * VSPR
	PRP1 6-0 = 0101000	((274R – 80R) / 450R) * VSPR
	PRP1 6-0 = 0101001	((274R – 82R) / 450R) * VSPR
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * VSPR
	PRP1 6-0 = 0101011	((274R – 86R) / 450R) * VSPR
	PRP1 6-0 = 0101100	((274R – 88R) / 450R) * VSPR
	PRP1 6-0 = 0101101	((274R – 90R) / 450R) * VSPR
	PRP1 6-0 = 0101110	((274R – 92R) / 450R) * VSPR
	PRP1 6-0 = 0101111	((274R – 94R) / 450R) * VSPR
	PRP1 6-0 = 0110000	((274R – 96R) / 450R) * VSPR
	PRP1 6-0 = 0110001	((274R – 98R) / 450R) * VSPR
	PRP1 6-0 = 0110010	((274R – 100R) / 450R) * VSPR
	PRP1 6-0 = 0110011	((274R – 102R) / 450R) * VSPR
	PRP1 6-0 = 0110100	((274R – 104R) / 450R) * VSPR
	PRP1 6-0 = 0110101	((274R – 106R) / 450R) * VSPR
	PRP1 6-0 = 0110110	((274R – 108R) / 450R) * VSPR
	PRP1 6-0 = 0110111	((274R – 110R) / 450R) * VSPR
	PRP1 6-0 = 0111000	((274R – 112R) / 450R) * VSPR
	PRP1 6-0 = 0111001	((274R – 114R) / 450R) * VSPR
	PRP1 6-0 = 0111010	((274R – 116R) / 450R) * VSPR
	PRP1 6-0 = 0111011	((274R – 118R) / 450R) * VSPR
	PRP1 6-0 = 0111100	((274R – 120R) / 450R) * VSPR
	PRP1 6-0 = 0111101	((274R – 122R) / 450R) * VSPR
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * VSPR
	PRP1 6-0 = 0111111	((274R – 126R) / 450R) * VSPR
	PRP1 6-0 = 1000000	((274R – 128R) / 450R) * VSPR
	PRP1 6-0 = 1000001	((274R – 130R) / 450R) * VSPR
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * VSPR
	PRP1 6-0 = 1000011	((274R – 134R) / 450R) * VSPR
	PRP1 6-0 = 1000100	((274R – 136R) / 450R) * VSPR

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Reference voltage	Micro adjustment value	VinP13 formula
	PRP1 6-0 = 1000101	((274R – 138R) / 450R) * VSPR
	PRP1 6-0 = 1000110	((274R – 140R) / 450R) * VSPR
	PRP1 6-0 = 1000111	((274R – 142R) / 450R) * VSPR
	PRP1 6-0 = 1001000	((274R – 144R) / 450R) * VSPR
	PRP1 6-0 = 1001001	((274R – 146R) / 450R) * VSPR
	PRP1 6-0 = 1001010	((274R – 148R) / 450R) * VSPR
	PRP1 6-0 = 1001011	((274R – 150R) / 450R) * VSPR
	PRP1 6-0 = 1001100	((274R - 152R) / 450R) * VSPR
	PRP1 6-0 = 1001101	((274R – 154R) / 450R) * VSPR
	PRP1 6-0 = 1001110	((274R – 156R) / 450R) * VSPR
	PRP1 6-0 = 1001111	((274R – 158R) / 450R) * VSPR
	PRP1 6-0 = 1010000	((274R – 160R) / 450R) * VSPR
	PRP1 6-0 = 1010001	((274R – 162R) / 450R) * VSPR
	PRP1 6-0 = 1010010	((274R – 164R) / 450R) * VSPR
	PRP1 6-0 = 1010011	((274R – 166R) / 450R) * VSPR
	PRP1 6-0 = 1010100	((274R – 168R) / 450R) * VSPR
	PRP1 6-0 = 1010101	((274R – 170R) / 450R) * VSPR
	PRP1 6-0 = 1010110	((274R – 172R) / 450R) * VSPR
	PRP1 6-0 = 1010111	((274R - 174R) / 450R) * VSPR
	PRP1 6-0 = 1011000	inhibit
	PRP1 6-0 = 1011001	inhibit
	PRP1 6-0 = 1011010	inhibit
	PRP1 6-0 = 1011011	inhibit
	PRP1 6-0 = 1011100	inhibit
	PRP1 6-0 = 1011101	inhibit
	PRP1 6-0 = 1011110	inhibit
	PRP1 6-0 = 1011111	inhibit
	PRP1 6-0 = 1100000	inhibit
	PRP1 6-0 = 1100001	inhibit
	PRP1 6-0 = 1100010	inhibit
	PRP1 6-0 = 1100011	inhibit
	PRP1 6-0 = 1100100	inhibit
	PRP1 6-0 = 1100101	inhibit
	PRP1 6-0 = 1100110	inhibit
	PRP1 6-0 = 1100111	inhibit
	PRP1 6-0 = 1101000	inhibit
	PRP1 6-0 = 1101001	inhibit
	PRP1 6-0 = 1101010	inhibit
	PRP1 6-0 = 1101011	inhibit
	PRP1 6-0 = 1101100	inhibit
	PRP1 6-0 = 1101101	inhibit
	PRP1 6-0 = 1101110	inhibit
	PRP1 6-0 = 1101111	inhibit
	PRP1 6-0 = 1110000	inhibit
	PRP1 6-0 = 1110001	inhibit
	PRP1 6-0 = 1110010	inhibit
	PRP1 6-0 = 1110011	inhibit
	PRP1 6-0 = 1110100	inhibit
	PRP1 6-0 = 1110101	inhibit
	PRP1 6-0 = 1110110	inhibit
	PRP1 6-0 = 1110111	inhibit
	PRP1 6-0 = 1111000	inhibit
	PRP1 6-0 = 1111001	inhibit
	PRP1 6-0 = 1111010	inhibit
	PRP1 6-0 = 1111011	inhibit
	PRP1 6-0 = 1111100	inhibit
	PRP1 6-0 = 1111101	inhibit
	PRP1 6-0 = 1111110	inhibit
	PRP1 6-0 = 1111111	inhibit

Table 5.13: VinP13

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Reference voltage	Micro adjustment value	VinP3 formula
VinP3	PKP0 4-0 = 00000	(47R / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00001	((47R – 1R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00010	((47R – 2R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00011	((47R – 3R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00100	((47R – 4R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00101	((47R – 5R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00110	((47R – 6R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 00111	((47R – 7R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01000	((47R – 8R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01001	((47R – 9R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01010	((47R - 10R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01011	((47R - 11R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01100	((47R - 12R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01101	((47R - 13R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01110	((47R - 14R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 01111	((47R - 15R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10000	((47R - 16R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10001	((47R - 17R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10010	((47R - 18R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10011	((47R - 19R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10100	((47R - 20R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10101	((47R - 21R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10110	((47R - 22R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 10111	((47R - 23R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11000	((47R - 24R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11001	((47R - 25R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11010	((47R - 26R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11011	((47R - 27R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11100	((47R - 28R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11101	((47R - 29R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11110	((47R - 30R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP0 4-0 = 11111	((47R - 31R) / 48R) * (VinP2 - VinP7) + VinP7

Table 5.14: VinP3

Reference voltage	Micro adjustment value	VinP4 formula
VinP4	PKP1 4-0 = 00000	(39R / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00001	((39R - 1R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00010	((39R - 2R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00011	((39R - 3R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00100	((39R - 4R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00101	((39R - 5R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00110	((39R - 6R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 00111	((39R - 7R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01000	((39R - 8R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01001	((39R - 9R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01010	((39R - 10R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01011	((39R - 11R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01100	((39R - 12R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01101	((39R - 13R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01110	((39R - 14R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 01111	((39R - 15R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10000	((39R - 16R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10001	((39R - 17R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10010	((39R - 18R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10011	((39R - 19R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10100	((39R - 20R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10101	((39R - 21R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10110	((39R - 22R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 10111	((39R - 23R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11000	((39R - 24R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11001	((39R - 25R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11010	((39R - 26R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11011	((39R - 27R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11100	((39R - 28R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11101	((39R - 29R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11110	((39R - 30R) / 48R) * (VinP2 - VinP7) + VinP7
	PKP1 4-0 = 11111	((39R - 31R) / 48R) * (VinP2 - VinP7) + VinP7

Table 5.15: VinP4

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Reference voltage	Micro adjustment value	VinP5 formula
VinP5	PKP2 4-0 = 00000	(32R / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00001	((32R – 1R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00010	((32R – 2R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00011	((32R – 3R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00100	((32R – 4R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00101	((32R – 5R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00110	((32R – 6R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 00111	((32R – 7R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01000	((32R – 8R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01001	((32R – 9R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01010	((32R – 10R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01011	((32R – 11R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01100	((32R – 12R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01101	((32R – 13R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01110	((32R – 14R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 01111	((32R – 15R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10000	((32R – 16R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10001	((32R – 17R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10010	((32R – 18R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10011	((32R – 19R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10100	((32R – 20R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10101	((32R – 21R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10110	((32R – 22R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 10111	((32R – 23R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11000	((32R – 24R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11001	((32R – 25R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11010	((32R – 26R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11011	((32R – 27R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11100	((32R – 28R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11101	((32R – 29R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11110	((32R – 30R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP2 4-0 = 11111	((32R – 31R) / 48R) * (VinP2 – VinP7) + VinP7

Table 5.16: VinP5

Reference voltage	Micro adjustment value	VinP6 formula
VinP6	PKP3 4-0 = 00000	(32R / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00001	((32R – 1R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00010	((32R – 2R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00011	((32R – 3R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00100	((32R – 4R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00101	((32R – 5R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00110	((32R – 6R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 00111	((32R – 7R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01000	((32R – 8R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01001	((32R – 9R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01010	((32R – 10R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01011	((32R – 11R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01100	((32R – 12R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01101	((32R – 13R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01110	((32R – 14R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 01111	((32R – 15R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10000	((32R – 16R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10001	((32R – 17R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10010	((32R – 18R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10011	((32R – 19R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10100	((32R – 20R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10101	((32R – 21R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10110	((32R – 22R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 10111	((32R – 23R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11000	((32R – 24R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11001	((32R – 25R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11010	((32R – 26R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11011	((32R – 27R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11100	((32R – 28R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11101	((32R – 29R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11110	((32R – 30R) / 48R) * (VinP2 – VinP7) + VinP7
	PKP3 4-0 = 11111	((32R – 31R) / 48R) * (VinP2 – VinP7) + VinP7

Table 5.17: VinP6

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Reference voltage	Micro adjustment value	VinP8 formula
VinP8	PKP4 4-0 = 00000	(220R / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00001	((220R - 3R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00010	((220R - 6R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00011	((220R - 9R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00100	((220R - 12R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00101	((220R - 15R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00110	((220R - 18R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 00111	((220R - 21R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01000	((220R - 24R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01001	((220R - 27R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01010	((220R - 30R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01011	((220R - 33R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01100	((220R - 36R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01101	((220R - 39R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01110	((220R - 42R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 01111	((220R - 45R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10000	((220R - 48R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10001	((220R - 51R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10010	((220R - 54R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10011	((220R - 57R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10100	((220R - 60R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10101	((220R - 63R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10110	((220R - 66R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 10111	((220R - 69R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11000	((220R - 72R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11001	((220R - 75R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11010	((220R - 78R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11011	((220R - 81R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11100	((220R - 84R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11101	((220R - 87R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11110	((220R - 90R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP4 4-0 = 11111	((220R - 93R) / 223R) * (VinP7 - VinP13) + VinP13

Table 5.18: VinP8

Reference voltage	Micro adjustment value	VinP9 formula
VinP9	PKP5 4-0 = 00000	(193R / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00001	((193R - 3R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00010	((193R - 6R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00011	((193R - 9R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00100	((193R - 12R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00101	((193R - 15R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00110	((193R - 18R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 00111	((193R - 21R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01000	((193R - 24R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01001	((193R - 27R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01010	((193R - 30R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01011	((193R - 33R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01100	((193R - 36R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01101	((193R - 39R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01110	((193R - 42R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 01111	((193R - 45R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10000	((193R - 48R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10001	((193R - 51R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10010	((193R - 54R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10011	((193R - 57R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10100	((193R - 60R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10101	((193R - 63R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10110	((193R - 66R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 10111	((193R - 69R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11000	((193R - 72R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11001	((193R - 75R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11010	((193R - 78R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11011	((193R - 81R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11100	((193R - 84R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11101	((193R - 87R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11110	((193R - 90R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP5 4-0 = 11111	((193R - 93R) / 223R) * (VinP7 - VinP13) + VinP13

Table 5.19: VinP9

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Reference voltage	Micro adjustment value	VinP10 formula
VinP10	PKP6 4-0 = 00000	(158R / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00001	((158R - 3R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00010	((158R - 6R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00011	((158R - 9R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00100	((158R - 12R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00101	((158R - 15R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00110	((158R - 18R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 00111	((158R - 21R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01000	((158R - 24R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01001	((158R - 27R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01010	((158R - 30R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01011	((158R - 33R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01100	((158R - 36R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01101	((158R - 39R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01110	((158R - 42R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 01111	((158R - 45R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10000	((158R - 48R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10001	((158R - 51R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10010	((158R - 54R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10011	((158R - 57R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10100	((158R - 60R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10101	((158R - 63R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10110	((158R - 66R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 10111	((158R - 69R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11000	((158R - 72R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11001	((158R - 75R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11010	((158R - 78R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11011	((158R - 81R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11100	((158R - 84R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11101	((158R - 87R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11110	((158R - 90R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP6 4-0 = 11111	((158R - 93R) / 223R) * (VinP7 - VinP13) + VinP13

Table 5.20: VinP10

Reference voltage	Micro adjustment value	VinP11 formula
VinP11	PKP7 4-0 = 00000	(123R / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00001	((123R - 3R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00010	((123R - 6R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00011	((123R - 9R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00100	((123R - 12R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00101	((123R - 15R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00110	((123R - 18R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 00111	((123R - 21R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01000	((123R - 24R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01001	((123R - 27R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01010	((123R - 30R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01011	((123R - 33R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01100	((123R - 36R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01101	((123R - 39R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01110	((123R - 42R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 01111	((123R - 45R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10000	((123R - 48R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10001	((123R - 51R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10010	((123R - 54R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10011	((123R - 57R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10100	((123R - 60R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10101	((123R - 63R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10110	((123R - 66R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 10111	((123R - 69R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11000	((123R - 72R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11001	((123R - 75R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11010	((123R - 78R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11011	((123R - 81R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11100	((123R - 84R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11101	((123R - 87R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11110	((123R - 90R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP7 4-0 = 11111	((123R - 93R) / 223R) * (VinP7 - VinP13) + VinP13

Table 5.21: VinP11

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Reference voltage	Micro adjustment value	VinP12 formula
VinP12	PKP8 4-0 = 00000	(96R / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00001	((96R - 3R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00010	((96R - 6R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00011	((96R - 9R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00100	((96R - 12R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00101	((96R - 15R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00110	((96R - 18R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 00111	((96R - 21R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01000	((96R - 24R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01001	((96R - 27R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01010	((96R - 30R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01011	((96R - 33R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01100	((96R - 36R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01101	((96R - 39R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01110	((96R - 42R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 01111	((96R - 45R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10000	((96R - 48R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10001	((96R - 51R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10010	((96R - 54R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10011	((96R - 57R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10100	((96R - 60R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10101	((96R - 63R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10110	((96R - 66R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 10111	((96R - 69R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11000	((96R - 72R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11001	((96R - 75R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11010	((96R - 78R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11011	((96R - 81R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11100	((96R - 84R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11101	((96R - 87R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11110	((96R - 90R) / 223R) * (VinP7 - VinP13) + VinP13
	PKP8 4-0 = 11111	((96R - 93R) / 223R) * (VinP7 - VinP13) + VinP13

Table 5.22: VinP12

Reference voltage	Micro adjustment value	VinP14 formula
VinP14	PKP9 4-0 = 00000	(47R / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00001	((47R - 1R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00010	((47R - 2R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00011	((47R - 3R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00100	((47R - 4R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00101	((47R - 5R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00110	((47R - 6R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 00111	((47R - 7R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01000	((47R - 8R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01001	((47R - 9R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01010	((47R - 10R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01011	((47R - 11R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01100	((47R - 12R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01101	((47R - 13R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01110	((47R - 14R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 01111	((47R - 15R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10000	((47R - 16R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10001	((47R - 17R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10010	((47R - 18R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10011	((47R - 19R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10100	((47R - 20R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10101	((47R - 21R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10110	((47R - 22R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 10111	((47R - 23R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11000	((47R - 24R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11001	((47R - 25R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11010	((47R - 26R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11011	((47R - 27R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11100	((47R - 28R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11101	((47R - 29R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11110	((47R - 30R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP9 4-0 = 11111	((47R - 31R) / 48R) * (VinP13 - VinP18) + VinP18

Table 5.23: VinP14

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Reference voltage	Micro adjustment value	VinP15 formula
VinP15	PKP10 4-0 = 00000	(47R / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00001	((47R – 1R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00010	((47R – 2R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00011	((47R – 3R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00100	((47R – 4R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00101	((47R – 5R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00110	((47R – 6R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 00111	((47R – 7R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01000	((47R – 8R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01001	((47R – 9R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01010	((47R – 10R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01011	((47R – 11R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01100	((47R – 12R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01101	((47R – 13R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01110	((47R – 14R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 01111	((47R – 15R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10000	((47R – 16R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10001	((47R – 17R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10010	((47R – 18R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10011	((47R – 19R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10100	((47R – 20R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10101	((47R – 21R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10110	((47R – 22R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 10111	((47R – 23R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11000	((47R – 24R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11001	((47R – 25R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11010	((47R – 26R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11011	((47R – 27R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11100	((47R – 28R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11101	((47R – 29R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11110	((47R – 30R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP10 4-0 = 11111	((47R – 31R) / 48R) * (VinP13 – VinP18) + VinP18

Table 5.24: VinP15

Reference voltage	Micro adjustment value	VinP16 formula
VinP16	PKP11 4-0 = 00000	(39R / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00001	((39R – 1R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00010	((39R – 2R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00011	((39R – 3R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00100	((39R – 4R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00101	((39R – 5R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00110	((39R – 6R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 00111	((39R – 7R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01000	((39R – 8R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01001	((39R – 9R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01010	((39R – 10R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01011	((39R – 11R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01100	((39R – 12R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01101	((39R – 13R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01110	((39R – 14R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 01111	((39R – 15R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10000	((39R – 16R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10001	((39R – 17R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10010	((39R – 18R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10011	((39R – 19R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10100	((39R – 20R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10101	((39R – 21R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10110	((39R – 22R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 10111	((39R – 23R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11000	((39R – 24R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11001	((39R – 25R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11010	((39R – 26R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11011	((39R – 27R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11100	((39R – 28R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11101	((39R – 29R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11110	((39R – 30R) / 48R) * (VinP13 – VinP18) + VinP18
	PKP11 4-0 = 11111	((39R – 31R) / 48R) * (VinP13 – VinP18) + VinP18

Table 5.25: VinP16

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Reference voltage	Micro adjustment value	VinP17 formula
VinP17	PKP12 4-0 = 00000	(32R / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00001	((32R - 1R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00010	((32R - 2R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00011	((32R - 3R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00100	((32R - 4R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00101	((32R - 5R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00110	((32R - 6R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 00111	((32R - 7R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01000	((32R - 8R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01001	((32R - 9R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01010	((32R - 10R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01011	((32R - 11R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01100	((32R - 12R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01101	((32R - 13R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01110	((32R - 14R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 01111	((32R - 15R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10000	((32R - 16R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10001	((32R - 17R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10010	((32R - 18R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10011	((32R - 19R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10100	((32R - 20R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10101	((32R - 21R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10110	((32R - 22R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 10111	((32R - 23R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11000	((32R - 24R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11001	((32R - 25R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11010	((32R - 26R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11011	((32R - 27R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11100	((32R - 28R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11101	((32R - 29R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11110	((32R - 30R) / 48R) * (VinP13 - VinP18) + VinP18
	PKP12 4-0 = 11111	((32R - 31R) / 48R) * (VinP13 - VinP18) + VinP18

Table 5.26: VinP17

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Reference voltage	Micro adjustment value	VinN0 formula
VinN0	VRN0 5-0 = 000000	VSNR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * VSNR
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * VSNR
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * VSNR
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * VSNR
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * VSNR
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * VSNR
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * VSNR
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * VSNR
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * VSNR
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * VSNR
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * VSNR
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * VSNR
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * VSNR
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * VSNR
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * VSNR
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * VSNR
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * VSNR
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * VSNR
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * VSNR
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * VSNR
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * VSNR
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * VSNR
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * VSNR
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * VSNR
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * VSNR
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * VSNR
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * VSNR
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * VSNR
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * VSNR
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * VSNR
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * VSNR
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * VSNR
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * VSNR
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * VSNR
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * VSNR
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * VSNR
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * VSNR
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * VSNR
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * VSNR
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * VSNR
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * VSNR
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * VSNR
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * VSNR
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * VSNR
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * VSNR
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * VSNR
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * VSNR
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * VSNR
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * VSNR
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * VSNR
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * VSNR
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * VSNR
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * VSNR
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * VSNR
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * VSNR
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * VSNR
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * VSNR
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * VSNR
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * VSNR
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * VSNR
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * VSNR
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * VSNR
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * VSNR

Table 5.27: VinN0

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Reference voltage	Micro adjustment value	VinN1 formula
VinN1	VRN1 5-0 = 000000	(430R / 450R) * VSNR
	VRN1 5-0 = 000001	((430R - 2R) / 450R) * VSNR
	VRN1 5-0 = 000010	((430R - 4R) / 450R) * VSNR
	VRN1 5-0 = 000011	((430R - 6R) / 450R) * VSNR
	VRN1 5-0 = 000100	((430R - 8R) / 450R) * VSNR
	VRN1 5-0 = 000101	((430R - 10R) / 450R) * VSNR
	VRN1 5-0 = 000110	((430R - 12R) / 450R) * VSNR
	VRN1 5-0 = 000111	((430R - 14R) / 450R) * VSNR
	VRN1 5-0 = 001000	((430R - 16R) / 450R) * VSNR
	VRN1 5-0 = 001001	((430R - 18R) / 450R) * VSNR
	VRN1 5-0 = 001010	((430R - 20R) / 450R) * VSNR
	VRN1 5-0 = 001011	((430R - 22R) / 450R) * VSNR
	VRN1 5-0 = 001100	((430R - 24R) / 450R) * VSNR
	VRN1 5-0 = 001101	((430R - 26R) / 450R) * VSNR
	VRN1 5-0 = 001110	((430R - 28R) / 450R) * VSNR
	VRN1 5-0 = 001111	((430R - 30R) / 450R) * VSNR
	VRN1 5-0 = 010000	((430R - 32R) / 450R) * VSNR
	VRN1 5-0 = 010001	((430R - 34R) / 450R) * VSNR
	VRN1 5-0 = 010010	((430R - 36R) / 450R) * VSNR
	VRN1 5-0 = 010011	((430R - 38R) / 450R) * VSNR
	VRN1 5-0 = 010100	((430R - 40R) / 450R) * VSNR
	VRN1 5-0 = 010101	((430R - 42R) / 450R) * VSNR
	VRN1 5-0 = 010110	((430R - 44R) / 450R) * VSNR
	VRN1 5-0 = 010111	((430R - 46R) / 450R) * VSNR
	VRN1 5-0 = 011000	((430R - 48R) / 450R) * VSNR
	VRN1 5-0 = 011001	((430R - 50R) / 450R) * VSNR
	VRN1 5-0 = 011010	((430R - 52R) / 450R) * VSNR
	VRN1 5-0 = 011011	((430R - 54R) / 450R) * VSNR
	VRN1 5-0 = 011100	((430R - 56R) / 450R) * VSNR
	VRN1 5-0 = 011101	((430R - 58R) / 450R) * VSNR
	VRN1 5-0 = 011110	((430R - 60R) / 450R) * VSNR
	VRN1 5-0 = 011111	((430R - 62R) / 450R) * VSNR
	VRN1 5-0 = 100000	((430R - 64R) / 450R) * VSNR
	VRN1 5-0 = 100001	((430R - 66R) / 450R) * VSNR
	VRN1 5-0 = 100010	((430R - 68R) / 450R) * VSNR
	VRN1 5-0 = 100011	((430R - 70R) / 450R) * VSNR
	VRN1 5-0 = 100100	((430R - 72R) / 450R) * VSNR
	VRN1 5-0 = 100101	((430R - 74R) / 450R) * VSNR
	VRN1 5-0 = 100110	((430R - 76R) / 450R) * VSNR
	VRN1 5-0 = 100111	((430R - 78R) / 450R) * VSNR
	VRN1 5-0 = 101000	((430R - 80R) / 450R) * VSNR
	VRN1 5-0 = 101001	((430R - 82R) / 450R) * VSNR
	VRN1 5-0 = 101010	((430R - 84R) / 450R) * VSNR
	VRN1 5-0 = 101011	((430R - 86R) / 450R) * VSNR
	VRN1 5-0 = 101100	((430R - 88R) / 450R) * VSNR
	VRN1 5-0 = 101101	((430R - 90R) / 450R) * VSNR
	VRN1 5-0 = 101110	((430R - 92R) / 450R) * VSNR
	VRN1 5-0 = 101111	((430R - 94R) / 450R) * VSNR
	VRN1 5-0 = 110000	((430R - 96R) / 450R) * VSNR
	VRN1 5-0 = 110001	((430R - 98R) / 450R) * VSNR
	VRN1 5-0 = 110010	((430R - 100R) / 450R) * VSNR
	VRN1 5-0 = 110011	((430R - 102R) / 450R) * VSNR
	VRN1 5-0 = 110100	((430R - 104R) / 450R) * VSNR
	VRN1 5-0 = 110101	((430R - 106R) / 450R) * VSNR
	VRN1 5-0 = 110110	((430R - 108R) / 450R) * VSNR
	VRN1 5-0 = 110111	((430R - 110R) / 450R) * VSNR
	VRN1 5-0 = 111000	((430R - 112R) / 450R) * VSNR
	VRN1 5-0 = 111001	((430R - 114R) / 450R) * VSNR
	VRN1 5-0 = 111010	((430R - 116R) / 450R) * VSNR
	VRN1 5-0 = 111011	((430R - 118R) / 450R) * VSNR
	VRN1 5-0 = 111100	((430R - 120R) / 450R) * VSNR
	VRN1 5-0 = 111101	((430R - 122R) / 450R) * VSNR
	VRN1 5-0 = 111110	((430R - 124R) / 450R) * VSNR
	VRN1 5-0 = 111111	((430R - 126R) / 450R) * VSNR

Table 5.28: VinN1

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Reference voltage	Micro adjustment value	VinN2 formula
VinN2	VRN2 5-0 = 000000	(420R / 450R) * VSNR
	VRN2 5-0 = 000001	((420R - 2R) / 450R) * VSNR
	VRN2 5-0 = 000010	((420R - 4R) / 450R) * VSNR
	VRN2 5-0 = 000011	((420R - 6R) / 450R) * VSNR
	VRN2 5-0 = 000100	((420R - 8R) / 450R) * VSNR
	VRN2 5-0 = 000101	((420R - 10R) / 450R) * VSNR
	VRN2 5-0 = 000110	((420R - 12R) / 450R) * VSNR
	VRN2 5-0 = 000111	((420R - 14R) / 450R) * VSNR
	VRN2 5-0 = 001000	((420R - 16R) / 450R) * VSNR
	VRN2 5-0 = 001001	((420R - 18R) / 450R) * VSNR
	VRN2 5-0 = 001010	((420R - 20R) / 450R) * VSNR
	VRN2 5-0 = 001011	((420R - 22R) / 450R) * VSNR
	VRN2 5-0 = 001100	((420R - 24R) / 450R) * VSNR
	VRN2 5-0 = 001101	((420R - 26R) / 450R) * VSNR
	VRN2 5-0 = 001110	((420R - 28R) / 450R) * VSNR
	VRN2 5-0 = 001111	((420R - 30R) / 450R) * VSNR
	VRN2 5-0 = 010000	((420R - 32R) / 450R) * VSNR
	VRN2 5-0 = 010001	((420R - 34R) / 450R) * VSNR
	VRN2 5-0 = 010010	((420R - 36R) / 450R) * VSNR
	VRN2 5-0 = 010011	((420R - 38R) / 450R) * VSNR
	VRN2 5-0 = 010100	((420R - 40R) / 450R) * VSNR
	VRN2 5-0 = 010101	((420R - 42R) / 450R) * VSNR
	VRN2 5-0 = 010110	((420R - 44R) / 450R) * VSNR
	VRN2 5-0 = 010111	((420R - 46R) / 450R) * VSNR
	VRN2 5-0 = 011000	((420R - 48R) / 450R) * VSNR
	VRN2 5-0 = 011001	((420R - 50R) / 450R) * VSNR
	VRN2 5-0 = 011010	((420R - 52R) / 450R) * VSNR
	VRN2 5-0 = 011011	((420R - 54R) / 450R) * VSNR
	VRN2 5-0 = 011100	((420R - 56R) / 450R) * VSNR
	VRN2 5-0 = 011101	((420R - 58R) / 450R) * VSNR
	VRN2 5-0 = 011110	((420R - 60R) / 450R) * VSNR
	VRN2 5-0 = 011111	((420R - 62R) / 450R) * VSNR
	VRN2 5-0 = 100000	((420R - 64R) / 450R) * VSNR
	VRN2 5-0 = 100001	((420R - 66R) / 450R) * VSNR
	VRN2 5-0 = 100010	((420R - 68R) / 450R) * VSNR
	VRN2 5-0 = 100011	((420R - 70R) / 450R) * VSNR
	VRN2 5-0 = 100100	((420R - 72R) / 450R) * VSNR
	VRN2 5-0 = 100101	((420R - 74R) / 450R) * VSNR
	VRN2 5-0 = 100110	((420R - 76R) / 450R) * VSNR
	VRN2 5-0 = 100111	((420R - 78R) / 450R) * VSNR
	VRN2 5-0 = 101000	((420R - 80R) / 450R) * VSNR
	VRN2 5-0 = 101001	((420R - 82R) / 450R) * VSNR
	VRN2 5-0 = 101010	((420R - 84R) / 450R) * VSNR
	VRN2 5-0 = 101011	((420R - 86R) / 450R) * VSNR
	VRN2 5-0 = 101100	((420R - 88R) / 450R) * VSNR
	VRN2 5-0 = 101101	((420R - 90R) / 450R) * VSNR
	VRN2 5-0 = 101110	((420R - 92R) / 450R) * VSNR
	VRN2 5-0 = 101111	((420R - 94R) / 450R) * VSNR
	VRN2 5-0 = 110000	((420R - 96R) / 450R) * VSNR
	VRN2 5-0 = 110001	((420R - 98R) / 450R) * VSNR
	VRN2 5-0 = 110010	((420R - 100R) / 450R) * VSNR
	VRN2 5-0 = 110011	((420R - 102R) / 450R) * VSNR
	VRN2 5-0 = 110100	((420R - 104R) / 450R) * VSNR
	VRN2 5-0 = 110101	((420R - 106R) / 450R) * VSNR
	VRN2 5-0 = 110110	((420R - 108R) / 450R) * VSNR
	VRN2 5-0 = 110111	((420R - 110R) / 450R) * VSNR
	VRN2 5-0 = 111000	((420R - 112R) / 450R) * VSNR
	VRN2 5-0 = 111001	((420R - 114R) / 450R) * VSNR
	VRN2 5-0 = 111010	((420R - 116R) / 450R) * VSNR
	VRN2 5-0 = 111011	((420R - 118R) / 450R) * VSNR
	VRN2 5-0 = 111100	((420R - 120R) / 450R) * VSNR
	VRN2 5-0 = 111101	((420R - 122R) / 450R) * VSNR
	VRN2 5-0 = 111110	((420R - 124R) / 450R) * VSNR
	VRN2 5-0 = 111111	((420R - 126R) / 450R) * VSNR

Table 5.29: VinN2

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Reference voltage	Micro adjustment value	VinN18 formula
VinN18	VRN3 5-0 = 000000	(156R / 450R) * VSNR
	VRN3 5-0 = 000001	((156R - 2R) / 450R) * VSNR
	VRN3 5-0 = 000010	((156R - 4R) / 450R) * VSNR
	VRN3 5-0 = 000011	((156R - 6R) / 450R) * VSNR
	VRN3 5-0 = 000100	((156R - 8R) / 450R) * VSNR
	VRN3 5-0 = 000101	((156R - 10R) / 450R) * VSNR
	VRN3 5-0 = 000110	((156R - 12R) / 450R) * VSNR
	VRN3 5-0 = 000111	((156R - 14R) / 450R) * VSNR
	VRN3 5-0 = 001000	((156R - 16R) / 450R) * VSNR
	VRN3 5-0 = 001001	((156R - 18R) / 450R) * VSNR
	VRN3 5-0 = 001010	((156R - 20R) / 450R) * VSNR
	VRN3 5-0 = 001011	((156R - 22R) / 450R) * VSNR
	VRN3 5-0 = 001100	((156R - 24R) / 450R) * VSNR
	VRN3 5-0 = 001101	((156R - 26R) / 450R) * VSNR
	VRN3 5-0 = 001110	((156R - 28R) / 450R) * VSNR
	VRN3 5-0 = 001111	((156R - 30R) / 450R) * VSNR
	VRN3 5-0 = 010000	((156R - 32R) / 450R) * VSNR
	VRN3 5-0 = 010001	((156R - 34R) / 450R) * VSNR
	VRN3 5-0 = 010010	((156R - 36R) / 450R) * VSNR
	VRN3 5-0 = 010011	((156R - 38R) / 450R) * VSNR
	VRN3 5-0 = 010100	((156R - 40R) / 450R) * VSNR
	VRN3 5-0 = 010101	((156R - 42R) / 450R) * VSNR
	VRN3 5-0 = 010110	((156R - 44R) / 450R) * VSNR
	VRN3 5-0 = 010111	((156R - 46R) / 450R) * VSNR
	VRN3 5-0 = 011000	((156R - 48R) / 450R) * VSNR
	VRN3 5-0 = 011001	((156R - 50R) / 450R) * VSNR
	VRN3 5-0 = 011010	((156R - 52R) / 450R) * VSNR
	VRN3 5-0 = 011011	((156R - 54R) / 450R) * VSNR
	VRN3 5-0 = 011100	((156R - 56R) / 450R) * VSNR
	VRN3 5-0 = 011101	((156R - 58R) / 450R) * VSNR
	VRN3 5-0 = 011110	((156R - 60R) / 450R) * VSNR
	VRN3 5-0 = 011111	((156R - 62R) / 450R) * VSNR
	VRN3 5-0 = 100000	((156R - 64R) / 450R) * VSNR
	VRN3 5-0 = 100001	((156R - 66R) / 450R) * VSNR
	VRN3 5-0 = 100010	((156R - 68R) / 450R) * VSNR
	VRN3 5-0 = 100011	((156R - 70R) / 450R) * VSNR
	VRN3 5-0 = 100100	((156R - 72R) / 450R) * VSNR
	VRN3 5-0 = 100101	((156R - 74R) / 450R) * VSNR
	VRN3 5-0 = 100110	((156R - 76R) / 450R) * VSNR
	VRN3 5-0 = 100111	((156R - 78R) / 450R) * VSNR
	VRN3 5-0 = 101000	((156R - 80R) / 450R) * VSNR
	VRN3 5-0 = 101001	((156R - 82R) / 450R) * VSNR
	VRN3 5-0 = 101010	((156R - 84R) / 450R) * VSNR
	VRN3 5-0 = 101011	((156R - 86R) / 450R) * VSNR
	VRN3 5-0 = 101100	((156R - 88R) / 450R) * VSNR
	VRN3 5-0 = 101101	((156R - 90R) / 450R) * VSNR
	VRN3 5-0 = 101110	((156R - 92R) / 450R) * VSNR
	VRN3 5-0 = 101111	((156R - 94R) / 450R) * VSNR
	VRN3 5-0 = 110000	((156R - 96R) / 450R) * VSNR
	VRN3 5-0 = 110001	((156R - 98R) / 450R) * VSNR
	VRN3 5-0 = 110010	((156R - 100R) / 450R) * VSNR
	VRN3 5-0 = 110011	((156R - 102R) / 450R) * VSNR
	VRN3 5-0 = 110100	((156R - 104R) / 450R) * VSNR
	VRN3 5-0 = 110101	((156R - 106R) / 450R) * VSNR
	VRN3 5-0 = 110110	((156R - 108R) / 450R) * VSNR
	VRN3 5-0 = 110111	((156R - 110R) / 450R) * VSNR
	VRN3 5-0 = 111000	((156R - 112R) / 450R) * VSNR
	VRN3 5-0 = 111001	((156R - 114R) / 450R) * VSNR
	VRN3 5-0 = 111010	((156R - 116R) / 450R) * VSNR
	VRN3 5-0 = 111011	((156R - 118R) / 450R) * VSNR
	VRN3 5-0 = 111100	((156R - 120R) / 450R) * VSNR
	VRN3 5-0 = 111101	((156R - 122R) / 450R) * VSNR
	VRN3 5-0 = 111110	((156R - 124R) / 450R) * VSNR
	VRN3 5-0 = 111111	((156R - 126R) / 450R) * VSNR

Table 5.30: VinN18

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Reference voltage	Micro adjustment value	VinN19 formula
VinN19	VRN4 5-0 = 000000	(146R / 450R) * VSNR
	VRN4 5-0 = 000001	((146R - 2R) / 450R) * VSNR
	VRN4 5-0 = 000010	((146R - 4R) / 450R) * VSNR
	VRN4 5-0 = 000011	((146R - 6R) / 450R) * VSNR
	VRN4 5-0 = 000100	((146R - 8R) / 450R) * VSNR
	VRN4 5-0 = 000101	((146R - 10R) / 450R) * VSNR
	VRN4 5-0 = 000110	((146R - 12R) / 450R) * VSNR
	VRN4 5-0 = 000111	((146R - 14R) / 450R) * VSNR
	VRN4 5-0 = 001000	((146R - 16R) / 450R) * VSNR
	VRN4 5-0 = 001001	((146R - 18R) / 450R) * VSNR
	VRN4 5-0 = 001010	((146R - 20R) / 450R) * VSNR
	VRN4 5-0 = 001011	((146R - 22R) / 450R) * VSNR
	VRN4 5-0 = 001100	((146R - 24R) / 450R) * VSNR
	VRN4 5-0 = 001101	((146R - 26R) / 450R) * VSNR
	VRN4 5-0 = 001110	((146R - 28R) / 450R) * VSNR
	VRN4 5-0 = 001111	((146R - 30R) / 450R) * VSNR
	VRN4 5-0 = 010000	((146R - 32R) / 450R) * VSNR
	VRN4 5-0 = 010001	((146R - 34R) / 450R) * VSNR
	VRN4 5-0 = 010010	((146R - 36R) / 450R) * VSNR
	VRN4 5-0 = 010011	((146R - 38R) / 450R) * VSNR
	VRN4 5-0 = 010100	((146R - 40R) / 450R) * VSNR
	VRN4 5-0 = 010101	((146R - 42R) / 450R) * VSNR
	VRN4 5-0 = 010110	((146R - 44R) / 450R) * VSNR
	VRN4 5-0 = 010111	((146R - 46R) / 450R) * VSNR
	VRN4 5-0 = 011000	((146R - 48R) / 450R) * VSNR
	VRN4 5-0 = 011001	((146R - 50R) / 450R) * VSNR
	VRN4 5-0 = 011010	((146R - 52R) / 450R) * VSNR
	VRN4 5-0 = 011011	((146R - 54R) / 450R) * VSNR
	VRN4 5-0 = 011100	((146R - 56R) / 450R) * VSNR
	VRN4 5-0 = 011101	((146R - 58R) / 450R) * VSNR
	VRN4 5-0 = 011110	((146R - 60R) / 450R) * VSNR
	VRN4 5-0 = 011111	((146R - 62R) / 450R) * VSNR
	VRN4 5-0 = 100000	((146R - 64R) / 450R) * VSNR
	VRN4 5-0 = 100001	((146R - 66R) / 450R) * VSNR
	VRN4 5-0 = 100010	((146R - 68R) / 450R) * VSNR
	VRN4 5-0 = 100011	((146R - 70R) / 450R) * VSNR
	VRN4 5-0 = 100100	((146R - 72R) / 450R) * VSNR
	VRN4 5-0 = 100101	((146R - 74R) / 450R) * VSNR
	VRN4 5-0 = 100110	((146R - 76R) / 450R) * VSNR
	VRN4 5-0 = 100111	((146R - 78R) / 450R) * VSNR
	VRN4 5-0 = 101000	((146R - 80R) / 450R) * VSNR
	VRN4 5-0 = 101001	((146R - 82R) / 450R) * VSNR
	VRN4 5-0 = 101010	((146R - 84R) / 450R) * VSNR
	VRN4 5-0 = 101011	((146R - 86R) / 450R) * VSNR
	VRN4 5-0 = 101100	((146R - 88R) / 450R) * VSNR
	VRN4 5-0 = 101101	((146R - 90R) / 450R) * VSNR
	VRN4 5-0 = 101110	((146R - 92R) / 450R) * VSNR
	VRN4 5-0 = 101111	((146R - 94R) / 450R) * VSNR
	VRN4 5-0 = 110000	((146R - 96R) / 450R) * VSNR
	VRN4 5-0 = 110001	((146R - 98R) / 450R) * VSNR
	VRN4 5-0 = 110010	((146R - 100R) / 450R) * VSNR
	VRN4 5-0 = 110011	((146R - 102R) / 450R) * VSNR
	VRN4 5-0 = 110100	((146R - 104R) / 450R) * VSNR
	VRN4 5-0 = 110101	((146R - 106R) / 450R) * VSNR
	VRN4 5-0 = 110110	((146R - 108R) / 450R) * VSNR
	VRN4 5-0 = 110111	((146R - 110R) / 450R) * VSNR
	VRN4 5-0 = 111000	((146R - 112R) / 450R) * VSNR
	VRN4 5-0 = 111001	((146R - 114R) / 450R) * VSNR
	VRN4 5-0 = 111010	((146R - 116R) / 450R) * VSNR
	VRN4 5-0 = 111011	((146R - 118R) / 450R) * VSNR
	VRN4 5-0 = 111100	((146R - 120R) / 450R) * VSNR
	VRN4 5-0 = 111101	((146R - 122R) / 450R) * VSNR
	VRN4 5-0 = 111110	((146R - 124R) / 450R) * VSNR
	VRN4 5-0 = 111111	((146R - 126R) / 450R) * VSNR

Table 5.31: VinN19

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Reference voltage	Micro adjustment value	VinN20 formula
VinN20	VRN5 5-0 = 000000	(144R / 450R) * VSNR
	VRN5 5-0 = 000001	((144R - 2R) / 450R) * VSNR
	VRN5 5-0 = 000010	((144R - 4R) / 450R) * VSNR
	VRN5 5-0 = 000011	((144R - 6R) / 450R) * VSNR
	VRN5 5-0 = 000100	((144R - 8R) / 450R) * VSNR
	VRN5 5-0 = 000101	((144R - 10R) / 450R) * VSNR
	VRN5 5-0 = 000110	((144R - 12R) / 450R) * VSNR
	VRN5 5-0 = 000111	((144R - 14R) / 450R) * VSNR
	VRN5 5-0 = 001000	((144R - 16R) / 450R) * VSNR
	VRN5 5-0 = 001001	((144R - 18R) / 450R) * VSNR
	VRN5 5-0 = 001010	((144R - 20R) / 450R) * VSNR
	VRN5 5-0 = 001011	((144R - 22R) / 450R) * VSNR
	VRN5 5-0 = 001100	((144R - 24R) / 450R) * VSNR
	VRN5 5-0 = 001101	((144R - 26R) / 450R) * VSNR
	VRN5 5-0 = 001110	((144R - 28R) / 450R) * VSNR
	VRN5 5-0 = 001111	((144R - 30R) / 450R) * VSNR
	VRN5 5-0 = 010000	((144R - 32R) / 450R) * VSNR
	VRN5 5-0 = 010001	((144R - 34R) / 450R) * VSNR
	VRN5 5-0 = 010010	((144R - 36R) / 450R) * VSNR
	VRN5 5-0 = 010011	((144R - 38R) / 450R) * VSNR
	VRN5 5-0 = 010100	((144R - 40R) / 450R) * VSNR
	VRN5 5-0 = 010101	((144R - 42R) / 450R) * VSNR
	VRN5 5-0 = 010110	((144R - 44R) / 450R) * VSNR
	VRN5 5-0 = 010111	((144R - 46R) / 450R) * VSNR
	VRN5 5-0 = 011000	((144R - 48R) / 450R) * VSNR
	VRN5 5-0 = 011001	((144R - 50R) / 450R) * VSNR
	VRN5 5-0 = 011010	((144R - 52R) / 450R) * VSNR
	VRN5 5-0 = 011011	((144R - 54R) / 450R) * VSNR
	VRN5 5-0 = 011100	((144R - 56R) / 450R) * VSNR
	VRN5 5-0 = 011101	((144R - 58R) / 450R) * VSNR
	VRN5 5-0 = 011110	((144R - 60R) / 450R) * VSNR
	VRN5 5-0 = 011111	((144R - 62R) / 450R) * VSNR
	VRN5 5-0 = 100000	((144R - 64R) / 450R) * VSNR
	VRN5 5-0 = 100001	((144R - 66R) / 450R) * VSNR
	VRN5 5-0 = 100010	((144R - 68R) / 450R) * VSNR
	VRN5 5-0 = 100011	((144R - 70R) / 450R) * VSNR
	VRN5 5-0 = 100100	((144R - 72R) / 450R) * VSNR
	VRN5 5-0 = 100101	((144R - 74R) / 450R) * VSNR
	VRN5 5-0 = 100110	((144R - 76R) / 450R) * VSNR
	VRN5 5-0 = 100111	((144R - 78R) / 450R) * VSNR
	VRN5 5-0 = 101000	((144R - 80R) / 450R) * VSNR
	VRN5 5-0 = 101001	((144R - 82R) / 450R) * VSNR
	VRN5 5-0 = 101010	((144R - 84R) / 450R) * VSNR
	VRN5 5-0 = 101011	((144R - 86R) / 450R) * VSNR
	VRN5 5-0 = 101100	((144R - 88R) / 450R) * VSNR
	VRN5 5-0 = 101101	((144R - 90R) / 450R) * VSNR
	VRN5 5-0 = 101110	((144R - 92R) / 450R) * VSNR
	VRN5 5-0 = 101111	((144R - 94R) / 450R) * VSNR
	VRN5 5-0 = 110000	((144R - 96R) / 450R) * VSNR
	VRN5 5-0 = 110001	((144R - 98R) / 450R) * VSNR
	VRN5 5-0 = 110010	((144R - 100R) / 450R) * VSNR
	VRN5 5-0 = 110011	((144R - 102R) / 450R) * VSNR
	VRN5 5-0 = 110100	((144R - 104R) / 450R) * VSNR
	VRN5 5-0 = 110101	((144R - 106R) / 450R) * VSNR
	VRN5 5-0 = 110110	((144R - 108R) / 450R) * VSNR
	VRN5 5-0 = 110111	((144R - 110R) / 450R) * VSNR
	VRN5 5-0 = 111000	((144R - 112R) / 450R) * VSNR
	VRN5 5-0 = 111001	((144R - 114R) / 450R) * VSNR
	VRN5 5-0 = 111010	((144R - 116R) / 450R) * VSNR
	VRN5 5-0 = 111011	((144R - 118R) / 450R) * VSNR
	VRN5 5-0 = 111100	((144R - 120R) / 450R) * VSNR
	VRN5 5-0 = 111101	((144R - 122R) / 450R) * VSNR
	VRN5 5-0 = 111110	((144R - 124R) / 450R) * VSNR
	VRN5 5-0 = 111111	VGSP

Table 5.32: VinN20

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Reference voltage	Micro adjustment value	VinN7 formula
VinN7	PRN0 6-0 = 0000000	(350R / 450R) VSPR
	PRN0 6-0 = 0000001	((350R - 2R) / 450R) * VSPR
	PRN0 6-0 = 0000010	((350R - 4R) / 450R) * VSPR
	PRN0 6-0 = 0000011	((350R – 6R) / 450R) * VSPR
	PRN0 6-0 = 0000100	((350R – 8R) / 450R) * VSPR
	PRN0 6-0 = 0000101	((350R – 10R) / 450R) * VSPR
	PRN0 6-0 = 0000110	((350R – 12R) / 450R) * VSPR
	PRN0 6-0 = 0000111	((350R - 14R) / 450R) * VSPR
	PRN0 6-0 = 0001000	((350R – 16R) / 450R) * VSPR
	PRN0 6-0 = 0001001	((350R – 18R) / 450R) * VSPR
	PRN0 6-0 = 0001010	((350R – 20R) / 450R) * VSPR
	PRN0 6-0 = 0001011	((350R – 22R) / 450R) * VSPR
	PRN0 6-0 = 0001100	((350R – 24R) / 450R) * VSPR
	PRN0 6-0 = 0001101	((350R – 26R) / 450R) * VSPR
	PRN0 6-0 = 0001110	((350R – 28R) / 450R) * VSPR
	PRN0 6-0 = 0001111	((350R – 30R) / 450R) * VSPR
	PRN0 6-0 = 0010000	((350R – 32R) / 450R) * VSPR
	PRN0 6-0 = 0010001	((350R - 34R) / 450R) * VSPR
	PRN0 6-0 = 0010010	((350R – 36R) / 450R) * VSPR
	PRN0 6-0 = 0010011	((350R – 38R) / 450R) * VSPR
	PRN0 6-0 = 0010100	((350R – 40R) / 450R) * VSPR
	PRN0 6-0 = 0010101	((350R – 42R) / 450R) * VSPR
	PRN0 6-0 = 0010110	((350R – 44R) / 450R) * VSPR
	PRN0 6-0 = 0010111	((350R – 46R) / 450R) * VSPR
	PRN0 6-0 = 0011000	((350R – 48R) / 450R) * VSPR
	PRN0 6-0 = 0011001	((350R – 50R) / 450R) * VSPR
	PRN0 6-0 = 0011010	((350R – 52R) / 450R) * VSPR
	PRN0 6-0 = 0011011	((350R - 54R) / 450R) * VSPR
	PRN0 6-0 = 0011100	((350R – 56R) / 450R) * VSPR
	PRN0 6-0 = 0011101	((350R – 58R) / 450R) * VSPR
	PRN0 6-0 = 0011110	((350R – 60R) / 450R) * VSPR
	PRN0 6-0 = 0011111	((350R – 62R) / 450R) * VSPR
	PRN0 6-0 = 0100000	((350R - 64R) / 450R) * VSPR
	PRN0 6-0 = 0100001	((350R – 66R) / 450R) * VSPR
	PRN0 6-0 = 0100010	((350R – 68R) / 450R) * VSPR
	PRN0 6-0 = 0100011	((350R – 70R) / 450R) * VSPR
	PRN0 6-0 = 0100100	((350R – 72R) / 450R) * VSPR
	PRN0 6-0 = 0100101	((350R – 74R) / 450R) * VSPR
	PRN0 6-0 = 0100110	((350R – 76R) / 450R) * VSPR
	PRN0 6-0 = 0100111	((350R – 78R) / 450R) * VSPR
	PRN0 6-0 = 0101000	((350R – 80R) / 450R) * VSPR
	PRN0 6-0 = 0101001	((350R – 82R) / 450R) * VSPR
	PRN0 6-0 = 0101010	((350R - 84R) / 450R) * VSPR
	PRN0 6-0 = 0101011	((350R – 86R) / 450R) * VSPR
	PRN0 6-0 = 0101100	((350R – 88R) / 450R) * VSPR
	PRN0 6-0 = 0101101	((350R – 90R) / 450R) * VSPR
	PRN0 6-0 = 0101110	((350R – 92R) / 450R) * VSPR
	PRN0 6-0 = 0101111	((350R – 94R) / 450R) * VSPR
	PRN0 6-0 = 0110000	((350R – 96R) / 450R) * VSPR
	PRN0 6-0 = 0110001	((350R – 98R) / 450R) * VSPR
	PRN0 6-0 = 0110010	((350R – 100R) / 450R) * VSPR
	PRN0 6-0 = 0110011	((350R – 102R) / 450R) * VSPR
	PRN0 6-0 = 0110100	((350R – 104R) / 450R) * VSPR
	PRN0 6-0 = 0110101	((350R – 106R) / 450R) * VSPR
	PRN0 6-0 = 0110110	((350R – 108R) / 450R) * VSPR
	PRN0 6-0 = 0110111	((350R – 110R) / 450R) * VSPR
	PRN0 6-0 = 0111000	((350R – 112R) / 450R) * VSPR
	PRN0 6-0 = 0111001	((350R – 114R) / 450R) * VSPR
	PRN0 6-0 = 0111010	((350R – 116R) / 450R) * VSPR
	PRN0 6-0 = 0111011	((350R – 118R) / 450R) * VSPR
	PRN0 6-0 = 0111100	((350R – 120R) / 450R) * VSPR
	PRN0 6-0 = 0111101	((350R – 122R) / 450R) * VSPR
	PRN0 6-0 = 0111110	((350R - 124R) / 450R) * VSPR
	PRN0 6-0 = 0111111	((350R – 126R) / 450R) * VSPR
	PRN0 6-0 = 1000000	((350R – 128R) / 450R) * VSPR
	PRN0 6-0 = 1000001	((350R – 130R) / 450R) * VSPR
	PRN0 6-0 = 1000010	((350R - 132R) / 450R) * VSPR
	PRN0 6-0 = 1000011	((350R – 134R) / 450R) * VSPR
	PRN0 6-0 = 1000100	((350R – 136R) / 450R) * VSPR

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Reference voltage	Micro adjustment value	VinN7 formula
	PRN0 6-0 = 1000101	((350R – 138R) / 450R) * VSPR
	PRN0 6-0 = 1000110	((350R – 140R) / 450R) * VSPR
	PRN0 6-0 = 1000111	((350R – 142R) / 450R) * VSPR
	PRN0 6-0 = 1001000	((350R – 144R) / 450R) * VSPR
	PRN0 6-0 = 1001001	((350R – 146R) / 450R) * VSPR
	PRN0 6-0 = 1001010	((350R – 148R) / 450R) * VSPR
	PRN0 6-0 = 1001011	((350R – 150R) / 450R) * VSPR
	PRN0 6-0 = 1001100	((350R - 152R) / 450R) * VSPR
	PRN0 6-0 = 1001101	((350R – 154R) / 450R) * VSPR
	PRN0 6-0 = 1001110	((350R – 156R) / 450R) * VSPR
	PRN0 6-0 = 1001111	((350R – 158R) / 450R) * VSPR
	PRN0 6-0 = 1010000	((350R – 160R) / 450R) * VSPR
	PRN0 6-0 = 1010001	((350R – 162R) / 450R) * VSPR
	PRN0 6-0 = 1010010	((350R – 164R) / 450R) * VSPR
	PRN0 6-0 = 1010011	((350R – 166R) / 450R) * VSPR
	PRN0 6-0 = 1010100	((350R – 168R) / 450R) * VSPR
	PRN0 6-0 = 1010101	((350R – 170R) / 450R) * VSPR
	PRN0 6-0 = 1010110	((350R – 172R) / 450R) * VSPR
	PRN0 6-0 = 1010111	((350R - 174R) / 450R) * VSPR
	PRN0 6-0 = 1011000	inhibit
	PRN0 6-0 = 1011001	inhibit
	PRN0 6-0 = 1011010	inhibit
	PRN0 6-0 = 1011011	inhibit
	PRN0 6-0 = 1011100	inhibit
	PRN0 6-0 = 1011101	inhibit
	PRN0 6-0 = 1011110	inhibit
	PRN0 6-0 = 1011111	inhibit
	PRN0 6-0 = 1100000	inhibit
	PRN0 6-0 = 1100001	inhibit
	PRN0 6-0 = 1100010	inhibit
	PRN0 6-0 = 1100011	inhibit
	PRN0 6-0 = 1100100	inhibit
	PRN0 6-0 = 1100101	inhibit
	PRN0 6-0 = 1100110	inhibit
	PRN0 6-0 = 1100111	inhibit
	PRN0 6-0 = 1101000	inhibit
	PRN0 6-0 = 1101001	inhibit
	PRN0 6-0 = 1101010	inhibit
	PRN0 6-0 = 1101011	inhibit
	PRN0 6-0 = 1101100	inhibit
	PRN0 6-0 = 1101101	inhibit
	PRN0 6-0 = 1101110	inhibit
	PRN0 6-0 = 1101111	inhibit
	PRN0 6-0 = 1110000	inhibit
	PRN0 6-0 = 1110001	inhibit
	PRN0 6-0 = 1110010	inhibit
	PRN0 6-0 = 1110011	inhibit
	PRN0 6-0 = 1110100	inhibit
	PRN0 6-0 = 1110101	inhibit
	PRN0 6-0 = 1110110	inhibit
	PRN0 6-0 = 1110111	inhibit
	PRN0 6-0 = 1111000	inhibit
	PRN0 6-0 = 1111001	inhibit
	PRN0 6-0 = 1111010	inhibit
	PRN0 6-0 = 1111011	inhibit
	PRN0 6-0 = 1111100	inhibit
	PRN0 6-0 = 1111101	inhibit
	PRN0 6-0 = 1111110	inhibit
	PRN0 6-0 = 1111111	inhibit

Table 5.33: VinN7

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Reference voltage	Micro adjustment value	VinN13 formula
VinN13	PRN1 6-0 = 0000000	(274R / 450R) VSPR
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * VSPR
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * VSPR
	PRN1 6-0 = 0000011	((274R – 6R) / 450R) * VSPR
	PRN1 6-0 = 0000100	((274R – 8R) / 450R) * VSPR
	PRN1 6-0 = 0000101	((274R – 10R) / 450R) * VSPR
	PRN1 6-0 = 0000110	((274R – 12R) / 450R) * VSPR
	PRN1 6-0 = 0000111	((274R - 14R) / 450R) * VSPR
	PRN1 6-0 = 0001000	((274R – 16R) / 450R) * VSPR
	PRN1 6-0 = 0001001	((274R – 18R) / 450R) * VSPR
	PRN1 6-0 = 0001010	((274R – 20R) / 450R) * VSPR
	PRN1 6-0 = 0001011	((274R – 22R) / 450R) * VSPR
	PRN1 6-0 = 0001100	((274R – 24R) / 450R) * VSPR
	PRN1 6-0 = 0001101	((274R – 26R) / 450R) * VSPR
	PRN1 6-0 = 0001110	((274R – 28R) / 450R) * VSPR
	PRN1 6-0 = 0001111	((274R – 30R) / 450R) * VSPR
	PRN1 6-0 = 0010000	((274R – 32R) / 450R) * VSPR
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * VSPR
	PRN1 6-0 = 0010010	((274R – 36R) / 450R) * VSPR
	PRN1 6-0 = 0010011	((274R – 38R) / 450R) * VSPR
	PRN1 6-0 = 0010100	((274R – 40R) / 450R) * VSPR
	PRN1 6-0 = 0010101	((274R – 42R) / 450R) * VSPR
	PRN1 6-0 = 0010110	((274R – 44R) / 450R) * VSPR
	PRN1 6-0 = 0010111	((274R – 46R) / 450R) * VSPR
	PRN1 6-0 = 0011000	((274R – 48R) / 450R) * VSPR
	PRN1 6-0 = 0011001	((274R – 50R) / 450R) * VSPR
	PRN1 6-0 = 0011010	((274R – 52R) / 450R) * VSPR
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * VSPR
	PRN1 6-0 = 0011100	((274R – 56R) / 450R) * VSPR
	PRN1 6-0 = 0011101	((274R – 58R) / 450R) * VSPR
	PRN1 6-0 = 0011110	((274R – 60R) / 450R) * VSPR
	PRN1 6-0 = 0011111	((274R – 62R) / 450R) * VSPR
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * VSPR
	PRN1 6-0 = 0100001	((274R – 66R) / 450R) * VSPR
	PRN1 6-0 = 0100010	((274R – 68R) / 450R) * VSPR
	PRN1 6-0 = 0100011	((274R – 70R) / 450R) * VSPR
	PRN1 6-0 = 0100100	((274R – 72R) / 450R) * VSPR
	PRN1 6-0 = 0100101	((274R – 74R) / 450R) * VSPR
	PRN1 6-0 = 0100110	((274R – 76R) / 450R) * VSPR
	PRN1 6-0 = 0100111	((274R – 78R) / 450R) * VSPR
	PRN1 6-0 = 0101000	((274R – 80R) / 450R) * VSPR
	PRN1 6-0 = 0101001	((274R – 82R) / 450R) * VSPR
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * VSPR
	PRN1 6-0 = 0101011	((274R – 86R) / 450R) * VSPR
	PRN1 6-0 = 0101100	((274R – 88R) / 450R) * VSPR
	PRN1 6-0 = 0101101	((274R – 90R) / 450R) * VSPR
	PRN1 6-0 = 0101110	((274R – 92R) / 450R) * VSPR
	PRN1 6-0 = 0101111	((274R – 94R) / 450R) * VSPR
	PRN1 6-0 = 0110000	((274R – 96R) / 450R) * VSPR
	PRN1 6-0 = 0110001	((274R – 98R) / 450R) * VSPR
	PRN1 6-0 = 0110010	((274R – 100R) / 450R) * VSPR
	PRN1 6-0 = 0110011	((274R – 102R) / 450R) * VSPR
	PRN1 6-0 = 0110100	((274R – 104R) / 450R) * VSPR
	PRN1 6-0 = 0110101	((274R – 106R) / 450R) * VSPR
	PRN1 6-0 = 0110110	((274R – 108R) / 450R) * VSPR
	PRN1 6-0 = 0110111	((274R – 110R) / 450R) * VSPR
	PRN1 6-0 = 0111000	((274R – 112R) / 450R) * VSPR
	PRN1 6-0 = 0111001	((274R – 114R) / 450R) * VSPR
	PRN1 6-0 = 0111010	((274R – 116R) / 450R) * VSPR
	PRN1 6-0 = 0111011	((274R – 118R) / 450R) * VSPR
	PRN1 6-0 = 0111100	((274R – 120R) / 450R) * VSPR
	PRN1 6-0 = 0111101	((274R – 122R) / 450R) * VSPR
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * VSPR
	PRN1 6-0 = 0111111	((274R – 126R) / 450R) * VSPR
	PRN1 6-0 = 1000000	((274R – 128R) / 450R) * VSPR
	PRN1 6-0 = 1000001	((274R – 130R) / 450R) * VSPR
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * VSPR
	PRN1 6-0 = 1000011	((274R – 134R) / 450R) * VSPR
	PRN1 6-0 = 1000100	((274R – 136R) / 450R) * VSPR

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Reference voltage	Micro adjustment value	VinN13 formula
	PRN1 6-0 = 1000101	((274R – 138R) / 450R) * VSPR
	PRN1 6-0 = 1000110	((274R – 140R) / 450R) * VSPR
	PRN1 6-0 = 1000111	((274R – 142R) / 450R) * VSPR
	PRN1 6-0 = 1001000	((274R – 144R) / 450R) * VSPR
	PRN1 6-0 = 1001001	((274R – 146R) / 450R) * VSPR
	PRN1 6-0 = 1001010	((274R – 148R) / 450R) * VSPR
	PRN1 6-0 = 1001011	((274R – 150R) / 450R) * VSPR
	PRN1 6-0 = 1001100	((274R - 152R) / 450R) * VSPR
	PRN1 6-0 = 1001101	((274R – 154R) / 450R) * VSPR
	PRN1 6-0 = 1001110	((274R – 156R) / 450R) * VSPR
	PRN1 6-0 = 1001111	((274R – 158R) / 450R) * VSPR
	PRN1 6-0 = 1010000	((274R – 160R) / 450R) * VSPR
	PRN1 6-0 = 1010001	((274R – 162R) / 450R) * VSPR
	PRN1 6-0 = 1010010	((274R – 164R) / 450R) * VSPR
	PRN1 6-0 = 1010011	((274R – 166R) / 450R) * VSPR
	PRN1 6-0 = 1010100	((274R – 168R) / 450R) * VSPR
	PRN1 6-0 = 1010101	((274R – 170R) / 450R) * VSPR
	PRN1 6-0 = 1010110	((274R – 172R) / 450R) * VSPR
	PRN1 6-0 = 1010111	((274R - 174R) / 450R) * VSPR
	PRN1 6-0 = 1011000	inhibit
	PRN1 6-0 = 1011001	inhibit
	PRN1 6-0 = 1011010	inhibit
	PRN1 6-0 = 1011011	inhibit
	PRN1 6-0 = 1011100	inhibit
	PRN1 6-0 = 1011101	inhibit
	PRN1 6-0 = 1011110	inhibit
	PRN1 6-0 = 1011111	inhibit
	PRN1 6-0 = 1100000	inhibit
	PRN1 6-0 = 1100001	inhibit
	PRN1 6-0 = 1100010	inhibit
	PRN1 6-0 = 1100011	inhibit
	PRN1 6-0 = 1100100	inhibit
	PRN1 6-0 = 1100101	inhibit
	PRN1 6-0 = 1100110	inhibit
	PRN1 6-0 = 1100111	inhibit
	PRN1 6-0 = 1101000	inhibit
	PRN1 6-0 = 1101001	inhibit
	PRN1 6-0 = 1101010	inhibit
	PRN1 6-0 = 1101011	inhibit
	PRN1 6-0 = 1101100	inhibit
	PRN1 6-0 = 1101101	inhibit
	PRN1 6-0 = 1101110	inhibit
	PRN1 6-0 = 1101111	inhibit
	PRN1 6-0 = 1110000	inhibit
	PRN1 6-0 = 1110001	inhibit
	PRN1 6-0 = 1110010	inhibit
	PRN1 6-0 = 1110011	inhibit
	PRN1 6-0 = 1110100	inhibit
	PRN1 6-0 = 1110101	inhibit
	PRN1 6-0 = 1110110	inhibit
	PRN1 6-0 = 1110111	inhibit
	PRN1 6-0 = 1111000	inhibit
	PRN1 6-0 = 1111001	inhibit
	PRN1 6-0 = 1111010	inhibit
	PRN1 6-0 = 1111011	inhibit
	PRN1 6-0 = 1111100	inhibit
	PRN1 6-0 = 1111101	inhibit
	PRN1 6-0 = 1111110	inhibit
	PRN1 6-0 = 1111111	inhibit

Table 5.34: VinN13

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Reference voltage	Micro adjustment value	VinN3 formula
VinN3	PKN0 4-0 = 00000	(47R / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00001	((47R – 1R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00010	((47R – 2R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00011	((47R – 3R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00100	((47R – 4R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00101	((47R – 5R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00110	((47R – 6R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 00111	((47R – 7R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01000	((47R – 8R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01001	((47R – 9R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01010	((47R - 10R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01011	((47R - 11R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01100	((47R - 12R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01101	((47R - 13R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01110	((47R - 14R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 01111	((47R - 15R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10000	((47R - 16R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10001	((47R - 17R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10010	((47R - 18R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10011	((47R - 19R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10100	((47R - 20R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10101	((47R - 21R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10110	((47R - 22R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 10111	((47R - 23R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11000	((47R - 24R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11001	((47R - 25R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11010	((47R - 26R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11011	((47R - 27R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11100	((47R - 28R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11101	((47R - 29R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11110	((47R - 30R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN0 4-0 = 11111	((47R - 31R) / 48R) * (VinN2 - VinN7) + VinN7

Table 5.35: VinN3

Reference voltage	Micro adjustment value	VinN4 formula
VinN4	PKN1 4-0 = 00000	(39R / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00001	((39R - 1R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00010	((39R - 2R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00011	((39R - 3R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00100	((39R - 4R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00101	((39R - 5R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00110	((39R - 6R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 00111	((39R - 7R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01000	((39R - 8R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01001	((39R - 9R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01010	((39R - 10R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01011	((39R - 11R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01100	((39R - 12R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01101	((39R - 13R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01110	((39R - 14R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 01111	((39R - 15R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10000	((39R - 16R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10001	((39R - 17R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10010	((39R - 18R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10011	((39R - 19R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10100	((39R - 20R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10101	((39R - 21R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10110	((39R - 22R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 10111	((39R - 23R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11000	((39R - 24R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11001	((39R - 25R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11010	((39R - 26R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11011	((39R - 27R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11100	((39R - 28R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11101	((39R - 29R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11110	((39R - 30R) / 48R) * (VinN2 - VinN7) + VinN7
	PKN1 4-0 = 11111	((39R - 31R) / 48R) * (VinN2 - VinN7) + VinN7

Table 5.36: VinN4

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Reference voltage	Micro adjustment value	VinN5 formula
VinN5	PKN2 4-0 = 00000	(32R / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00001	((32R – 1R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00010	((32R – 2R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00011	((32R – 3R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00100	((32R – 4R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00101	((32R – 5R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00110	((32R – 6R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 00111	((32R – 7R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01000	((32R – 8R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01001	((32R – 9R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01010	((32R – 10R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01011	((32R – 11R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01100	((32R – 12R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01101	((32R – 13R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01110	((32R – 14R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 01111	((32R – 15R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10000	((32R – 16R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10001	((32R – 17R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10010	((32R – 18R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10011	((32R – 19R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10100	((32R – 20R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10101	((32R – 21R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10110	((32R – 22R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 10111	((32R – 23R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11000	((32R – 24R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11001	((32R – 25R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11010	((32R – 26R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11011	((32R – 27R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11100	((32R – 28R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11101	((32R – 29R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11110	((32R – 30R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN2 4-0 = 11111	((32R – 31R) / 48R) * (VinN2 – VinN7) + VinN7

Table 5.37: VinN5

Reference voltage	Micro adjustment value	VinN6 formula
VinN6	PKN3 4-0 = 00000	(32R / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00001	((32R – 1R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00010	((32R – 2R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00011	((32R – 3R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00100	((32R – 4R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00101	((32R – 5R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00110	((32R – 6R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 00111	((32R – 7R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01000	((32R – 8R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01001	((32R – 9R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01010	((32R – 10R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01011	((32R – 11R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01100	((32R – 12R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01101	((32R – 13R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01110	((32R – 14R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 01111	((32R – 15R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10000	((32R – 16R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10001	((32R – 17R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10010	((32R – 18R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10011	((32R – 19R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10100	((32R – 20R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10101	((32R – 21R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10110	((32R – 22R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 10111	((32R – 23R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11000	((32R – 24R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11001	((32R – 25R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11010	((32R – 26R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11011	((32R – 27R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11100	((32R – 28R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11101	((32R – 29R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11110	((32R – 30R) / 48R) * (VinN2 – VinN7) + VinN7
	PKN3 4-0 = 11111	((32R – 31R) / 48R) * (VinN2 – VinN7) + VinN7

Table 5.38: VinN6

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Reference voltage	Micro adjustment value	VinN8 formula
VinN8	PKN4 4-0 = 00000	(220R / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00001	((220R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00010	((220R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00011	((220R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00100	((220R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00101	((220R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00110	((220R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 00111	((220R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01000	((220R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01001	((220R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01010	((220R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01011	((220R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01100	((220R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01101	((220R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01110	((220R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 01111	((220R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10000	((220R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10001	((220R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10010	((220R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10011	((220R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10100	((220R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10101	((220R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10110	((220R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 10111	((220R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11000	((220R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11001	((220R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11010	((220R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11011	((220R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11100	((220R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11101	((220R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11110	((220R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN4 4-0 = 11111	((220R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.39: VinN8

Reference voltage	Micro adjustment value	VinN9 formula
VinN9	PKN5 4-0 = 00000	(193R / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00001	((193R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00010	((193R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00011	((193R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00100	((193R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00101	((193R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00110	((193R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 00111	((193R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01000	((193R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01001	((193R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01010	((193R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01011	((193R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01100	((193R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01101	((193R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01110	((193R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 01111	((193R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10000	((193R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10001	((193R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10010	((193R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10011	((193R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10100	((193R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10101	((193R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10110	((193R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 10111	((193R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11000	((193R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11001	((193R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11010	((193R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11011	((193R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11100	((193R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11101	((193R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11110	((193R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN5 4-0 = 11111	((193R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.40: VinN9

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Reference voltage	Micro adjustment value	VinN10 formula
VinN10	PKN6 4-0 = 00000	(158R / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00001	((158R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00010	((158R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00011	((158R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00100	((158R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00101	((158R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00110	((158R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 00111	((158R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01000	((158R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01001	((158R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01010	((158R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01011	((158R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01100	((158R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01101	((158R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01110	((158R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 01111	((158R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10000	((158R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10001	((158R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10010	((158R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10011	((158R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10100	((158R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10101	((158R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10110	((158R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 10111	((158R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11000	((158R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11001	((158R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11010	((158R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11011	((158R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11100	((158R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11101	((158R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11110	((158R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN6 4-0 = 11111	((158R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.41: VinN10

Reference voltage	Micro adjustment value	VinN11 formula
VinN11	PKN7 4-0 = 00000	(123R / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00001	((123R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00010	((123R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00011	((123R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00100	((123R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00101	((123R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00110	((123R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 00111	((123R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01000	((123R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01001	((123R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01010	((123R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01011	((123R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01100	((123R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01101	((123R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01110	((123R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 01111	((123R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10000	((123R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10001	((123R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10010	((123R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10011	((123R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10100	((123R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10101	((123R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10110	((123R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 10111	((123R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11000	((123R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11001	((123R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11010	((123R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11011	((123R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11100	((123R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11101	((123R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11110	((123R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN7 4-0 = 11111	((123R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.42: VinN11

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Reference voltage	Micro adjustment value	VinN12 formula
VinN12	PKN8 4-0 = 00000	(96R / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00001	((96R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00010	((96R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00011	((96R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00100	((96R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00101	((96R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00110	((96R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00111	((96R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01000	((96R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01001	((96R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01010	((96R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01011	((96R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01100	((96R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01101	((96R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01110	((96R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01111	((96R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10000	((96R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10001	((96R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10010	((96R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10011	((96R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10100	((96R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10101	((96R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10110	((96R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10111	((96R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11000	((96R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11001	((96R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11010	((96R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11011	((96R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11100	((96R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11101	((96R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11110	((96R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11111	((96R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.43: VinN12

Reference voltage	Micro adjustment value	VinN14 formula
VinN14	PKN9 4-0 = 00000	(47R / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00001	((47R - 1R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00010	((47R - 2R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00011	((47R - 3R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00100	((47R - 4R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00101	((47R - 5R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00110	((47R - 6R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00111	((47R - 7R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01000	((47R - 8R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01001	((47R - 9R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01010	((47R - 10R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01011	((47R - 11R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01100	((47R - 12R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01101	((47R - 13R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01110	((47R - 14R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01111	((47R - 15R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10000	((47R - 16R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10001	((47R - 17R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10010	((47R - 18R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10011	((47R - 19R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10100	((47R - 20R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10101	((47R - 21R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10110	((47R - 22R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10111	((47R - 23R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11000	((47R - 24R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11001	((47R - 25R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11010	((47R - 26R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11011	((47R - 27R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11100	((47R - 28R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11101	((47R - 29R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11110	((47R - 30R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11111	((47R - 31R) / 48R) * (VinN13 - VinN18) + VinN18

Table 5.44: VinN14

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Reference voltage	Micro adjustment value	VinN15 formula
VinN15	PKN10 4-0 = 00000	(47R / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00001	((47R – 1R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00010	((47R – 2R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00011	((47R – 3R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00100	((47R – 4R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00101	((47R – 5R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00110	((47R – 6R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 00111	((47R – 7R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01000	((47R – 8R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01001	((47R – 9R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01010	((47R – 10R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01011	((47R – 11R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01100	((47R – 12R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01101	((47R – 13R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01110	((47R – 14R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 01111	((47R – 15R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10000	((47R – 16R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10001	((47R – 17R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10010	((47R – 18R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10011	((47R – 19R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10100	((47R – 20R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10101	((47R – 21R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10110	((47R – 22R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 10111	((47R – 23R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11000	((47R – 24R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11001	((47R – 25R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11010	((47R – 26R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11011	((47R – 27R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11100	((47R – 28R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11101	((47R – 29R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11110	((47R – 30R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN10 4-0 = 11111	((47R – 31R) / 48R) * (VinN13 – VinN18) + VinN18

Table 5.45: VinN15

Reference voltage	Micro adjustment value	VinN16 formula
VinN16	PKN11 4-0 = 00000	(39R / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00001	((39R – 1R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00010	((39R – 2R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00011	((39R – 3R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00100	((39R – 4R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00101	((39R – 5R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00110	((39R – 6R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 00111	((39R – 7R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01000	((39R – 8R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01001	((39R – 9R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01010	((39R – 10R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01011	((39R – 11R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01100	((39R – 12R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01101	((39R – 13R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01110	((39R – 14R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 01111	((39R – 15R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10000	((39R – 16R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10001	((39R – 17R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10010	((39R – 18R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10011	((39R – 19R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10100	((39R – 20R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10101	((39R – 21R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10110	((39R – 22R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 10111	((39R – 23R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11000	((39R – 24R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11001	((39R – 25R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11010	((39R – 26R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11011	((39R – 27R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11100	((39R – 28R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11101	((39R – 29R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11110	((39R – 30R) / 48R) * (VinN13 – VinN18) + VinN18
	PKN11 4-0 = 11111	((39R – 31R) / 48R) * (VinN13 – VinN18) + VinN18

Table 5.46: VinN16

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Reference voltage	Micro adjustment value	VinN17 formula
VinN17	PKN12 4-0 = 00000	(32R / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00001	((32R - 1R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00010	((32R - 2R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00011	((32R - 3R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00100	((32R - 4R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00101	((32R - 5R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00110	((32R - 6R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 00111	((32R - 7R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01000	((32R - 8R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01001	((32R - 9R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01010	((32R - 10R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01011	((32R - 11R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01100	((32R - 12R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01101	((32R - 13R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01110	((32R - 14R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 01111	((32R - 15R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10000	((32R - 16R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10001	((32R - 17R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10010	((32R - 18R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10011	((32R - 19R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10100	((32R - 20R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10101	((32R - 21R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10110	((32R - 22R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 10111	((32R - 23R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11000	((32R - 24R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11001	((32R - 25R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11010	((32R - 26R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11011	((32R - 27R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11100	((32R - 28R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11101	((32R - 29R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11110	((32R - 30R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN12 4-0 = 11111	((32R - 31R) / 48R) * (VinN13 - VinN18) + VinN18

Table 5.47: VinN17

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Grayscale voltage	Formula
V0	VinP/N0
V1	VinP/N0 - (VinP/N0 - VinP/N1)*(4R/16R)
V2	VinP/N0 - (VinP/N0 - VinP/N1)*(8R/16R)
V3	VinP/N0 - (VinP/N0 - VinP/N1)*(12R/16R)
V4	VinP/N1
V5	VinP/N1 - (VinP/N1 - VinP/N2)*(4R/16R)
V6	VinP/N1 - (VinP/N1 - VinP/N2)*(8R/16R)
V7	VinP/N1 - (VinP/N1 - VinP/N2)*(12R/16R)
V8	VinP/N2
V9	VinP/N2 - (VinP/N2 - VinP/N3)*(4R/16R)
V10	VinP/N2 - (VinP/N2 - VinP/N3)*(8R/16R)
V11	VinP/N2 - (VinP/N2 - VinP/N3)*(12R/16R)
V12	VinP/N3
V13	VinP/N3 - (VinP/N3 - VinP/N4)*(1.5R/12R)
V14	VinP/N3 - (VinP/N3 - VinP/N4)*(3R/12R)
V15	VinP/N3 - (VinP/N3 - VinP/N4)*(4.5R/12R)
V16	VinP/N3 - (VinP/N3 - VinP/N4)*(6R/12R)
V17	VinP/N3 - (VinP/N3 - VinP/N4)*(7.5R/12R)
V18	VinP/N3 - (VinP/N3 - VinP/N4)*(9R/12R)
V19	VinP/N3 - (VinP/N3 - VinP/N4)*(10.5R/12R)
V20	VinP/N4
V21	VinP/N4 - (VinP/N4 - VinP/N5)*(1.5R/12R)
V22	VinP/N4 - (VinP/N4 - VinP/N5)*(3R/12R)
V23	VinP/N4 - (VinP/N4 - VinP/N5)*(4.5R/12R)
V24	VinP/N4 - (VinP/N4 - VinP/N5)*(6R/12R)
V25	VinP/N4 - (VinP/N4 - VinP/N5)*(7.5R/12R)
V26	VinP/N4 - (VinP/N4 - VinP/N5)*(9R/12R)
V27	VinP/N4 - (VinP/N4 - VinP/N5)*(10.5R/12R)
V28	VinP/N5
V29	VinP/N5 - (VinP/N5 - VinP/N6)*(1.5R/18R)
V30	VinP/N5 - (VinP/N5 - VinP/N6)*(3R/18R)
V31	VinP/N5 - (VinP/N5 - VinP/N6)*(4.5R/18R)
V32	VinP/N5 - (VinP/N5 - VinP/N6)*(6R/18R)
V33	VinP/N5 - (VinP/N5 - VinP/N6)*(7.5R/18R)
V34	VinP/N5 - (VinP/N5 - VinP/N6)*(9R/18R)
V35	VinP/N5 - (VinP/N5 - VinP/N6)*(10.5R/18R)
V36	VinP/N5 - (VinP/N5 - VinP/N6)*(12R/18R)
V37	VinP/N5 - (VinP/N5 - VinP/N6)*(13.5R/18R)
V38	VinP/N5 - (VinP/N5 - VinP/N6)*(15R/18R)
V39	VinP/N5 - (VinP/N5 - VinP/N6)*(16.5R/18R)
V40	VinP/N6
V41	VinP/N6 - (VinP/N6 - VinP/N7)*(1.5R/18R)
V42	VinP/N6 - (VinP/N6 - VinP/N7)*(3R/18R)
V43	VinP/N6 - (VinP/N6 - VinP/N7*(4.5R/18R)

Grayscale voltage	Formula
V44	VinP/N6 - (VinP/N6 - VinP/N7)*(6R/18R)
V45	VinP/N6 - (VinP/N6 - VinP/N7)*(7.5R/18R)
V46	VinP/N6 - (VinP/N6 - VinP/N7)*(9R/18R)
V47	VinP/N6 - (VinP/N6 - VinP/N7)*(10.5R/18R)
V48	VinP/N6 - (VinP/N6 - VinP/N7)*(12R/18R)
V49	VinP/N6 - (VinP/N6 - VinP/N7)*(13.5R/18R)
V50	VinP/N6 - (VinP/N6 - VinP/N7)*(15R/18R)
V51	VinP/N6 - (VinP/N6 - VinP/N7)*(16.5R/18R)
V52	VinP/N7
V53	VinP/N7 - (VinP/N7 - VinP/N8)*(1.6R/38.4R)
V54	VinP/N7 - (VinP/N7 - VinP/N8)*(3.2R/38.4R)
V55	VinP/N7 - (VinP/N7 - VinP/N8)*(4.8R/38.4R)
V56	VinP/N7 - (VinP/N7 - VinP/N8)*(6.4R/38.4R)
V57	VinP/N7 - (VinP/N7 - VinP/N8)*(8R/38.4R)
V58	VinP/N7 - (VinP/N7 - VinP/N8)*(9.6R/38.4R)
V59	VinP/N7 - (VinP/N7 - VinP/N8)*(11.2R/38.4R)
V60	VinP/N7 - (VinP/N7 - VinP/N8)*(12.8R/38.4R)
V61	VinP/N7 - (VinP/N7 - VinP/N8)*(14.4R/38.4R)
V62	VinP/N7 - (VinP/N7 - VinP/N8)*(16R/38.4R)
V63	VinP/N7 - (VinP/N7 - VinP/N8)*(17.6R/38.4R)
V64	VinP/N7 - (VinP/N7 - VinP/N8)*(19.2R/38.4R)
V65	VinP/N7 - (VinP/N7 - VinP/N8)*(20.8R/38.4R)
V66	VinP/N7 - (VinP/N7 - VinP/N8)*(22.4R/38.4R)
V67	VinP/N7 - (VinP/N7 - VinP/N8)*(24R/38.4R)
V68	VinP/N7 - (VinP/N7 - VinP/N8)*(25.6R/38.4R)
V69	VinP/N7 - (VinP/N7 - VinP/N8)*(27.2R/38.4R)
V70	VinP/N7 - (VinP/N7 - VinP/N8)*(28.8R/38.4R)
V71	VinP/N7 - (VinP/N7 - VinP/N8)*(30.4R/38.4R)
V72	VinP/N7 - (VinP/N7 - VinP/N8)*(32R/38.4R)
V73	VinP/N7 - (VinP/N7 - VinP/N8)*(33.6R/38.4R)
V74	VinP/N7 - (VinP/N7 - VinP/N8)*(35.2R/38.4R)
V75	VinP/N7 - (VinP/N7 - VinP/N8)*(36.8R/38.4R)
V76	VinP/N8
V77	VinP/N8 - (VinP/N8 - VinP/N9)* (1.6R/38.4R)
V78	VinP/N8 - (VinP/N8 - VinP/N9)* (3.2R/38.4R)
V79	VinP/N8 - (VinP/N8 - VinP/N9)* (4.8R/38.4R)
V80	VinP/N8 - (VinP/N8 - VinP/N9)* (6.4R/38.4R)
V81	VinP/N8 - (VinP/N8 - VinP/N9)* (8R/38.4R)
V82	VinP/N8 - (VinP/N8 - VinP/N9)* (9.6R/38.4R)
V83	VinP/N8 - (VinP/N8 - VinP/N9)* (11.2R/38.4R)
V84	VinP/N8 - (VinP/N8 - VinP/N9)* (12.8R/38.4R)
V85	VinP/N8 - (VinP/N8 - VinP/N9)* (14.4R/38.4R)
V86	VinP/N8 - (VinP/N8 - VinP/N9)* (16R/38.4R)
V87	VinP/N8 - (VinP/N8 - VinP/N9)* (17.6R/38.4R)

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Grayscale voltage	Formula
V88	VinP/N8 - (VinP/N8 - VinP/N9)* (19.2R/38.4R)
V89	VinP/N8 - (VinP/N8 - VinP/N9)* (20.8R/38.4R)
V90	VinP/N8 - (VinP/N8 - VinP/N9)* (22.4R/38.4R)
V91	VinP/N8 - (VinP/N8 - VinP/N9)* (24R/38.4R)
V92	VinP/N8 - (VinP/N8 - VinP/N9)* (25.6R/38.4R)
V93	VinP/N8 - (VinP/N8 - VinP/N9)* (27.2R/38.4R)
V94	VinP/N8 - (VinP/N8 - VinP/N9)* (28.8R/38.4R)
V95	VinP/N8 - (VinP/N8 - VinP/N9)* (30.4R/38.4R)
V96	VinP/N8 - (VinP/N8 - VinP/N9)* (32R/38.4R)
V97	VinP/N8 - (VinP/N8 - VinP/N9)* (33.6R/38.4R)
V98	VinP/N8 - (VinP/N8 - VinP/N9)* (35.2R/38.4R)
V99	VinP/N8 - (VinP/N8 - VinP/N9)* (36.8R/38.4R)
V100	VinP/N9
V101	VinP/N9 - (VinP/N9 - VinP/N10)*(1.6R/51.2R)
V102	VinP/N9 - (VinP/N9 - VinP/N10)*(3.2R/51.2R)
V103	VinP/N9 - (VinP/N9 - VinP/N10)*(4.8R/51.2R)
V104	VinP/N9 - (VinP/N9 - VinP/N10)*(6.4R/51.2R)
V105	VinP/N9 - (VinP/N9 - VinP/N10)*(8R/51.2R)
V106	VinP/N9 - (VinP/N9 - VinP/N10)*(9.6R/51.2R)
V107	VinP/N9 - (VinP/N9 - VinP/N10)*(11.2R/51.2R)
V108	VinP/N9 - (VinP/N9 - VinP/N10)*(12.8R/51.2R)
V109	VinP/N9 - (VinP/N9 - VinP/N10)*(14.4R/51.2R)
V110	VinP/N9 - (VinP/N9 - VinP/N10)*(16R/51.2R)
V111	VinP/N9 - (VinP/N9 - VinP/N10)*(17.6R/51.2R)
V112	VinP/N9 - (VinP/N9 - VinP/N10)*(19.2R/51.2R)
V113	VinP/N9 - (VinP/N9 - VinP/N10)*(20.8R/51.2R)
V114	VinP/N9 - (VinP/N9 - VinP/N10)*(22.4R/51.2R)
V115	VinP/N9 - (VinP/N9 - VinP/N10)*(24R/51.2R)
V116	VinP/N9 - (VinP/N9 - VinP/N10)*(25.6R/51.2R)
V117	VinP/N9 - (VinP/N9 - VinP/N10)*(27.2R/51.2R)
V118	VinP/N9 - (VinP/N9 - VinP/N10)*(28.8R/51.2R)
V119	VinP/N9 - (VinP/N9 - VinP/N10)*(30.4R/51.2R)
V120	VinP/N9 - (VinP/N9 - VinP/N10)*(32R/51.2R)
V121	VinP/N9 - (VinP/N9 - VinP/N10)*(33.6R/51.2R)
V122	VinP/N9 - (VinP/N9 - VinP/N10)*(35.2R/51.2R)
V123	VinP/N9 - (VinP/N9 - VinP/N10)*(36.8R/51.2R)
V124	VinP/N9 - (VinP/N9 - VinP/N10)*(38.4R/51.2R)
V125	VinP/N9 - (VinP/N9 - VinP/N10)*(40R/51.2R)
V126	VinP/N9 - (VinP/N9 - VinP/N10)*(41.6R/51.2R)
V127	VinP/N9 - (VinP/N9 - VinP/N10)*(43.2R/51.2R)
V128	VinP/N9 - (VinP/N9 - VinP/N10)*(44.8R/51.2R)
V129	VinP/N9 - (VinP/N9 - VinP/N10)*(46.4R/51.2R)
V130	VinP/N9 - (VinP/N9 - VinP/N10)*(48R/51.2R)
V131	VinP/N9 - (VinP/N9 - VinP/N10)*(49.6R/51.2R)

Grayscale voltage	Formula
V132	VinP/N10
V133	VinP/N10 - (VinP/N10 - VinP/N11)*(1.6R/38.4R)
V134	VinP/N10 - (VinP/N10 - VinP/N11)*(3.2R/38.4R)
V135	VinP/N10 - (VinP/N10 - VinP/N11)*(4.8R/38.4R)
V136	VinP/N10 - (VinP/N10 - VinP/N11)*(6.4R/38.4R)
V137	VinP/N10 - (VinP/N10 - VinP/N11)*(8R/38.4R)
V138	VinP/N10 - (VinP/N10 - VinP/N11)*(9.6R/38.4R)
V139	VinP/N10 - (VinP/N10 - VinP/N11)*(11.2R/38.4R)
V140	VinP/N10 - (VinP/N10 - VinP/N11)*(12.8R/38.4R)
V141	VinP/N10 - (VinP/N10 - VinP/N11)*(14.4R/38.4R)
V142	VinP/N10 - (VinP/N10 - VinP/N11)*(16R/38.4R)
V143	VinP/N10 - (VinP/N10 - VinP/N11)*(17.6R/38.4R)
V144	VinP/N10 - (VinP/N10 - VinP/N11)*(19.2R/38.4R)
V145	VinP/N10 - (VinP/N10 - VinP/N11)*(20.8R/38.4R)
V146	VinP/N10 - (VinP/N10 - VinP/N11)*(22.4R/38.4R)
V147	VinP/N10 - (VinP/N10 - VinP/N11)*(24R/38.4R)
V148	VinP/N10 - (VinP/N10 - VinP/N11)*(25.6R/38.4R)
V149	VinP/N10 - (VinP/N10 - VinP/N11)*(27.2R/38.4R)
V150	VinP/N10 - (VinP/N10 - VinP/N11)*(28.8R/38.4R)
V151	VinP/N10 - (VinP/N10 - VinP/N11)*(30.4R/38.4R)
V152	VinP/N10 - (VinP/N10 - VinP/N11)*(32R/38.4R)
V153	VinP/N10 - (VinP/N10 - VinP/N11)*(33.6R/38.4R)
V154	VinP/N10 - (VinP/N10 - VinP/N11)*(35.2R/38.4R)
V155	VinP/N10 - (VinP/N10 - VinP/N11)*(36.8R/38.4R)
V156	VinP/N11
V157	VinP/N11 - (VinP/N11 - VinP/N12)*(1.6R/38.4R)
V158	VinP/N11 - (VinP/N11 - VinP/N12)*(3.2R/38.4R)
V159	VinP/N11 - (VinP/N11 - VinP/N12)*(4.8R/38.4R)
V160	VinP/N11 - (VinP/N11 - VinP/N12)*(6.4R/38.4R)
V161	VinP/N11 - (VinP/N11 - VinP/N12)*(8R/38.4R)
V162	VinP/N11 - (VinP/N11 - VinP/N12)*(9.6R/38.4R)
V163	VinP/N11 - (VinP/N11 - VinP/N12)*(11.2R/38.4R)
V164	VinP/N11 - (VinP/N11 - VinP/N12)*(12.8R/38.4R)
V165	VinP/N11 - (VinP/N11 - VinP/N12)*(14.4R/38.4R)
V166	VinP/N11 - (VinP/N11 - VinP/N12)*(16R/38.4R)
V167	VinP/N11 - (VinP/N11 - VinP/N12)*(17.6R/38.4R)
V168	VinP/N11 - (VinP/N11 - VinP/N12)*(19.2R/38.4R)
V169	VinP/N11 - (VinP/N11 - VinP/N12)*(20.8R/38.4R)
V170	VinP/N11 - (VinP/N11 - VinP/N12)*(22.4R/38.4R)
V171	VinP/N11 - (VinP/N11 - VinP/N12)*(24R/38.4R)
V172	VinP/N11 - (VinP/N11 - VinP/N12)*(25.6R/38.4R)
V173	VinP/N11 - (VinP/N11 - VinP/N12)*(27.2R/38.4R)
V174	VinP/N11 - (VinP/N11 - VinP/N12)*(28.8R/38.4R)
V175	VinP/N11 - (VinP/N11 - VinP/N12)*(30.4R/38.4R)

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Grayscale voltage	Formula
V176	VinP/N11 - (VinP/N11 - VinP/N12)*(32R/38.4R)
V177	VinP/N11 - (VinP/N11 - VinP/N12)*(33.6R/38.4R)
V178	VinP/N11 - (VinP/N11 - VinP/N12)*(35.2R/38.4R)
V179	VinP/N11 - (VinP/N11 - VinP/N12)*(36.8R/38.4R)
V180	VinP/N12
V181	VinP/N12 - (VinP/N12 - VinP/N13)*(1.6R/38.4R)
V182	VinP/N12 - (VinP/N12 - VinP/N13)*(3.2R/38.4R)
V183	VinP/N12 - (VinP/N12 - VinP/N13)*(4.8R/38.4R)
V184	VinP/N12 - (VinP/N12 - VinP/N13)*(6.4R/38.4R)
V185	VinP/N12 - (VinP/N12 - VinP/N13)*(8R/38.4R)
V186	VinP/N12 - (VinP/N12 - VinP/N13)*(9.6R/38.4R)
V187	VinP/N12 - (VinP/N12 - VinP/N13)*(11.2R/38.4R)
V188	VinP/N12 - (VinP/N12 - VinP/N13)*(12.8R/38.4R)
V189	VinP/N12 - (VinP/N12 - VinP/N13)*(14.4R/38.4R)
V190	VinP/N12 - (VinP/N12 - VinP/N13)*(16R/38.4R)
V191	VinP/N12 - (VinP/N12 - VinP/N13)*(17.6R/38.4R)
V192	VinP/N12 - (VinP/N12 - VinP/N13)*(19.2R/38.4R)
V193	VinP/N12 - (VinP/N12 - VinP/N13)*(20.8R/38.4R)
V194	VinP/N12 - (VinP/N12 - VinP/N13)*(22.4R/38.4R)
V195	VinP/N12 - (VinP/N12 - VinP/N13)*(24R/38.4R)
V196	VinP/N12 - (VinP/N12 - VinP/N13)*(25.6R/38.4R)
V197	VinP/N12 - (VinP/N12 - VinP/N13)*(27.2R/38.4R)
V198	VinP/N12 - (VinP/N12 - VinP/N13)*(28.8R/38.4R)
V199	VinP/N12 - (VinP/N12 - VinP/N13)*(30.4R/38.4R)
V200	VinP/N12 - (VinP/N12 - VinP/N13)*(32R/38.4R)
V201	VinP/N12 - (VinP/N12 - VinP/N13)*(33.6R/38.4R)
V202	VinP/N12 - (VinP/N12 - VinP/N13)*(35.2R/38.4R)
V203	VinP/N12 - (VinP/N12 - VinP/N13)*(36.8R/38.4R)
V204	VinP/N13
V205	VinP/N13 - (VinP/N13 - VinP/N14)*(1.5R/18R)
V206	VinP/N13 - (VinP/N13 - VinP/N14)*(3R/18R)
V207	VinP/N13 - (VinP/N13 - VinP/N14)*(4.5R/18R)
V208	VinP/N13 - (VinP/N13 - VinP/N14)*(6R/18R)
V209	VinP/N13 - (VinP/N13 - VinP/N14)*(7.5R/18R)
V210	VinP/N13 - (VinP/N13 - VinP/N14)*(9R/18R)
V211	VinP/N13 - (VinP/N13 - VinP/N14)*(10.5R/18R)
V212	VinP/N13 - (VinP/N13 - VinP/N14)*(12R/18R)
V213	VinP/N13 - (VinP/N13 - VinP/N14)*(13.5R/18R)
V214	VinP/N13 - (VinP/N13 - VinP/N14)*(15R/18R)
V215	VinP/N13 - (VinP/N13 - VinP/N14)*(16.5R/18R)
V216	VinP/N14
V217	VinP/N14 - (VinP/N14 - VinP/N15)*(1.5R/18R)
V218	VinP/N14 - (VinP/N14 - VinP/N15)*(3R/18R)
V219	VinP/N14 - (VinP/N14 - VinP/N15*(4.5R/18R)
V220	VinP/N14 - (VinP/N14 - VinP/N15)*(6R/18R)
V221	VinP/N14 - (VinP/N14 - VinP/N15)*(7.5R/18R)
V222	VinP/N14 - (VinP/N14 - VinP/N15)*(9R/18R)
V223	VinP/N14 - (VinP/N14 - VinP/N15)*(10.5R/18R)
V224	VinP/N14 - (VinP/N14 - VinP/N15)*(12R/18R)
V225	VinP/N14 - (VinP/N14 - VinP/N15)*(13.5R/18R)
V226	VinP/N14 - (VinP/N14 - VinP/N15)*(15R/18R)
V227	VinP/N14 - (VinP/N14 - VinP/N15)*(16.5R/18R)
V228	VinP/N15
V229	VinP/N15 - (VinP/N15 - VinP/N16)*(1.5R/12R)
V230	VinP/N15 - (VinP/N15 - VinP/N16)*(3R/12R)
V231	VinP/N15 - (VinP/N15 - VinP/N16)*(4.5R/12R)
V232	VinP/N15 - (VinP/N15 - VinP/N16)*(6R/12R)
V233	VinP/N15 - (VinP/N15 - VinP/N16)*(7.5R/12R)
V234	VinP/N15 - (VinP/N15 - VinP/N16)*(9R/12R)
V235	VinP/N15 - (VinP/N15 - VinP/N16)*(10.5R/12R)
V236	VinP/N16
V237	VinP/N16 - (VinP/N16 - VinP/N17)*(1.5R/10.5R)
V238	VinP/N16 - (VinP/N16 - VinP/N17)*(3R10.5R)
V239	VinP/N16 - (VinP/N16 - VinP/N17)*(4.5R/10.5R)
V240	VinP/N16 - (VinP/N16 - VinP/N17)*(6R/10.5R)
V241	VinP/N16 - (VinP/N16 - VinP/N17)*(7.5R/10.5R)
V242	VinP/N16 - (VinP/N16 - VinP/N17)*(9R/10.5R)
V243	VinP/N17
V244	VinP/N17 - (VinP/N17 - VinP/N18)*(4R/16R)
V245	VinP/N17 - (VinP/N17 - VinP/N18)*(8R/16R)
V246	VinP/N17 - (VinP/N17 - VinP/N18)*(12R/16R)
V247	VinP/N18
V248	VinP/N18 - (VinP/N18 - VinP/N19)*(4R/16R)
V249	VinP/N18 - (VinP/N18 - VinP/N19)*(8R/16R)
V250	VinP/N18 - (VinP/N18 - VinP/N19)*(12R/16R)
V251	VinP/N19
V252	VinP/N19 - (VinP/N19 - VinP/N20)*(4R/16R)
V253	VinP/N19 - (VinP/N19 - VinP/N20)*(8R/16R)
V254	VinP/N19 - (VinP/N19 - VinP/N20)*(12R/16R)
V255	VinP/N20

Table 5.48: Calculation Formula of 256-Grayscale Voltage (Positive/Negative Polarity)

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5.7.1 Gray voltage generator for digital gamma correction

The HX8379-C digital gamma correction can reach the independent gamma curve of RGB. HX8379-C utilizes DGC_LUT (Digital Gamma Correction Look-up Table) to change input data from 8-bit into 10-bit and sends 10-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

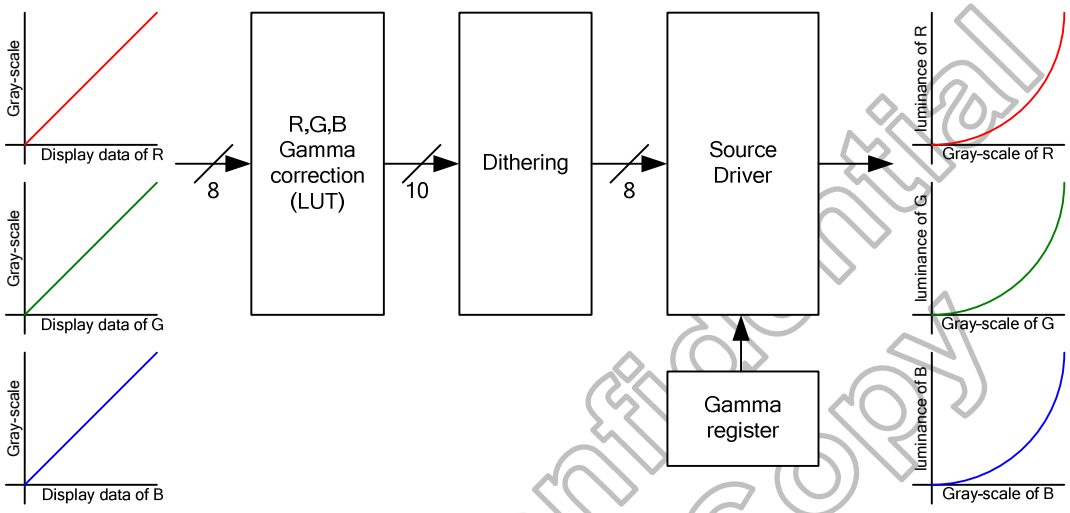


Figure 5.19: Block Diagram of Digital Gamma Correction

The HX8379-C builds one 126-bytes DGC_LUT (Digital Gamma Correction Look-Up Table) to transfer every display data of Dithering circuit input and setting by DGC_LUT register in CMD RC1h.

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By setting the independent R/G/B 33 sets of DGC_LUT[9:0], the corresponding source data can be extended to 1023 levels.

DGC_LUT[9:0] (10-bit)				Default Output Grayscale Voltage (8-bit)
DGC_LUT[9:2] (8-bit)	Default Value	DGC_LUT[1:0] (2-bit)	Default Value	
R00_/ G00_/ B00_[9:2]	00h	R00_/ G00_/ B00_[1:0]	0h	data_000
R01_/ G01_/ B01_[9:2]	08h	R01_/ G01_/ B01_[1:0]	0h	data_008
R02_/ G02_/ B02_[9:2]	10h	R02_/ G02_/ B02_[1:0]	0h	data_016
R03_/ G03_/ B03_[9:2]	18h	R03_/ G03_/ B03_[1:0]	0h	data_024
R04_/ G04_/ B04_[9:2]	20h	R04_/ G04_/ B04_[1:0]	0h	data_032
R05_/ G05_/ B05_[9:2]	28h	R05_/ G05_/ B05_[1:0]	0h	data_040
R06_/ G06_/ B06_[9:2]	30h	R06_/ G06_/ B06_[1:0]	0h	data_048
R07_/ G07_/ B07_[9:2]	38h	R07_/ G07_/ B07_[1:0]	0h	data_056
R08_/ G08_/ B08_[9:2]	40h	R08_/ G08_/ B08_[1:0]	0h	data_064
R09_/ G09_/ B09_[9:2]	48h	R09_/ G09_/ B09_[1:0]	0h	data_072
R10_/ G10_/ B10_[9:2]	50h	R10_/ G10_/ B10_[1:0]	0h	data_080
R11_/ G11_/ B11_[9:2]	58h	R11_/ G11_/ B11_[1:0]	0h	data_088
R12_/ G12_/ B12_[9:2]	60h	R12_/ G12_/ B12_[1:0]	0h	data_096
R13_/ G13_/ B13_[9:2]	68h	R13_/ G13_/ B13_[1:0]	0h	data_104
R14_/ G14_/ B14_[9:2]	70h	R14_/ G14_/ B14_[1:0]	0h	data_112
R15_/ G15_/ B15_[9:2]	78h	R15_/ G15_/ B15_[1:0]	0h	data_120
R16_/ G16_/ B16_[9:2]	80h	R16_/ G16_/ B16_[1:0]	0h	data_128
R17_/ G17_/ B17_[9:2]	88h	R17_/ G17_/ B17_[1:0]	0h	data_136
R18_/ G18_/ B18_[9:2]	90h	R18_/ G18_/ B18_[1:0]	0h	data_144
R19_/ G19_/ B19_[9:2]	98h	R19_/ G19_/ B19_[1:0]	0h	data_152
R20_/ G20_/ B20_[9:2]	A0h	R20_/ G20_/ B20_[1:0]	0h	data_160
R21_/ G21_/ B21_[9:2]	A8h	R21_/ G21_/ B21_[1:0]	0h	data_168
R22_/ G22_/ B22_[9:2]	B0h	R22_/ G22_/ B22_[1:0]	0h	data_176
R23_/ G23_/ B23_[9:2]	B8h	R23_/ G23_/ B23_[1:0]	0h	data_184
R24_/ G24_/ B24_[9:2]	C0h	R24_/ G24_/ B24_[1:0]	0h	data_192
R25_/ G25_/ B25_[9:2]	C8h	R25_/ G25_/ B25_[1:0]	0h	data_200
R26_/ G26_/ B26_[9:2]	D0h	R26_/ G26_/ B26_[1:0]	0h	data_208
R27_/ G27_/ B27_[9:2]	D8h	R27_/ G27_/ B27_[1:0]	0h	data_216
R28_/ G28_/ B28_[9:2]	E0h	R28_/ G28_/ B28_[1:0]	0h	data_224
R29_/ G29_/ B29_[9:2]	E8h	R29_/ G29_/ B29_[1:0]	0h	data_232
R30_/ G30_/ B30_[9:2]	F0h	R30_/ G30_/ B30_[1:0]	0h	data_240
R31_/ G31_/ B31_[9:2]	F8h	R31_/ G31_/ B31_[1:0]	0h	data_248
R32_/ G32_/ B32_[9:2]	FFh	R32_/ G32_/ B32_[1:0]	0h	data_255

Table 5.49: DGC-LUT

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5.8 Characteristics of I/O

5.8.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE_L	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low
CABC_LED_ON	Low	Low	Low
LED1 / LED2	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Table 5.50: Characteristics of Output or Bi-directional (I/O) Pins

5.8.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Setion.5.11	Input valid	Input valid	Input valid	Setion.5.11
CSX	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DCX	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
SCL_I2C_SCL	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DB[23:0]	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
SDI_I2C_SDA	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
HS	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
VS	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
PCLK	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DE	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
OSC	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
IM[3:0]	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
TEST[3:0]	Low	Low	Low	Low	Low

Table 5.51: Characteristics of Input Pins

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5.9 GIP control signal

HX8379-C is a single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display. There are many GIP/ASG type TFT panels that correspond to different GIP timing. Therefore, the GIP setting must be setup to the correct GIP/ASG timing for the normal display. The GIP timing adjustment is related to internal register.

The GIP control signals (CGOUT0_L/R ~ CGOUT15_L/R) are for panel used. The assignment of each panel type is specified on the application note. Regarding the GIP/ASG timing, please refer to HX8379-C application note.

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5.10 Sleep Out –command and self-diagnostic functions of the display module

5.10.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1). The flowchart for this internal function is shown as below.

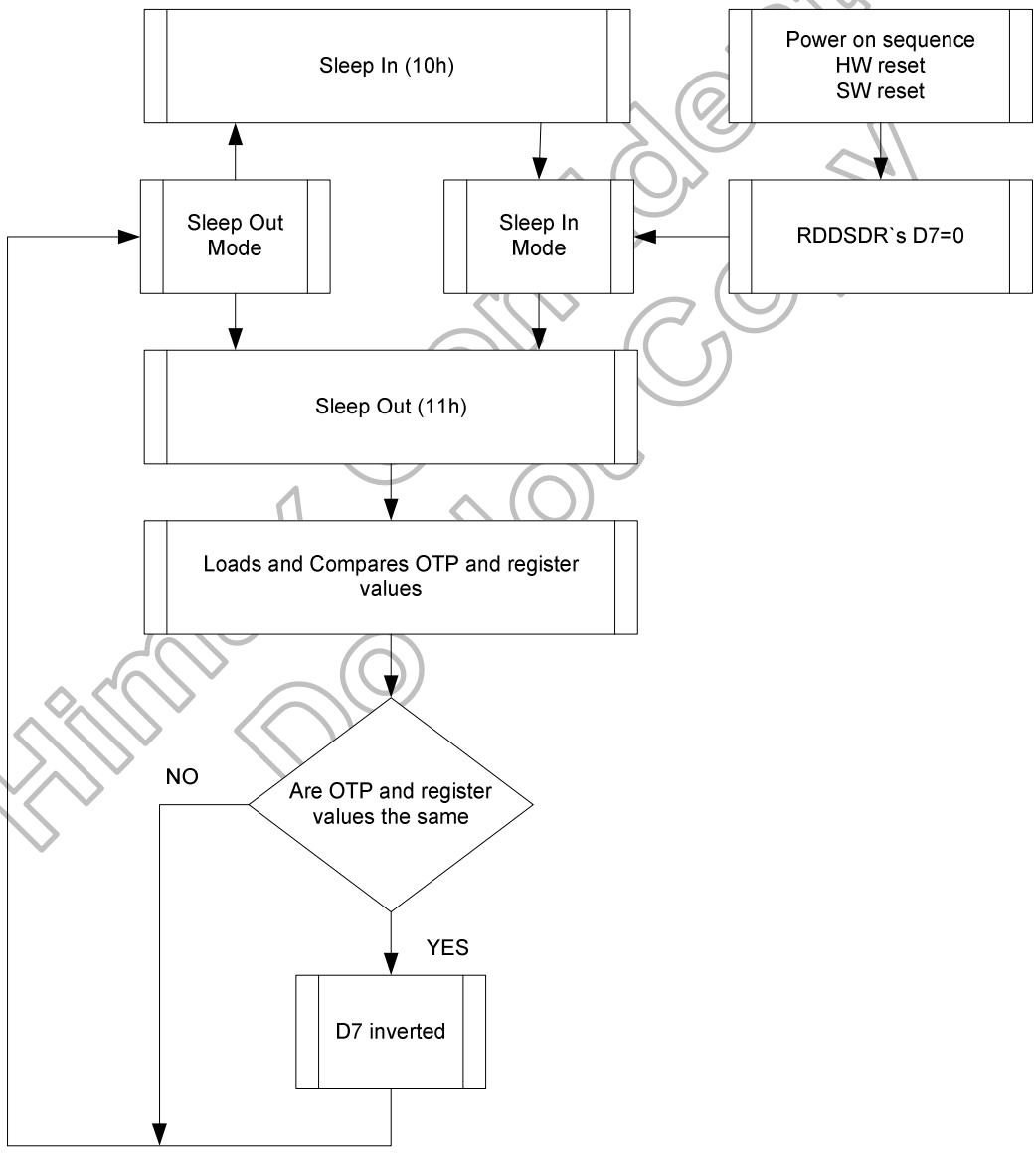
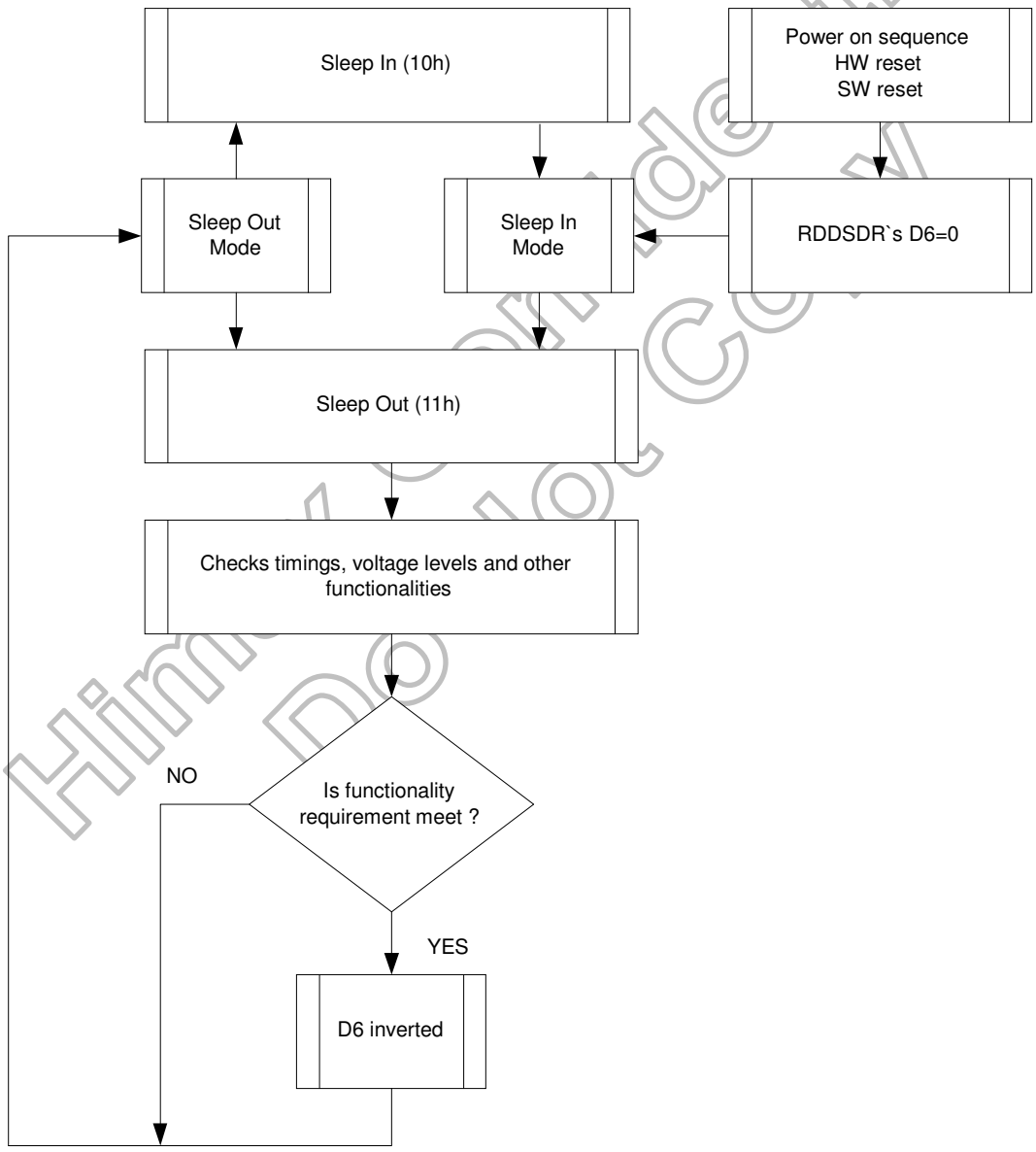


Figure 5.20: Sleep Out Flowchart–Command and Self-diagnostic Functions

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5.10.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.
The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flowchart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In–mode to Sleep Out -mode, before there is possible to check if Customer’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.21: Sleep Out Flowchart Internal Function Detection

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5.11 Power on/off sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down by minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down by minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power-On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power-On Sequence as defined in Sections 5.11.1 and 5.11.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power-On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

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5.11.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

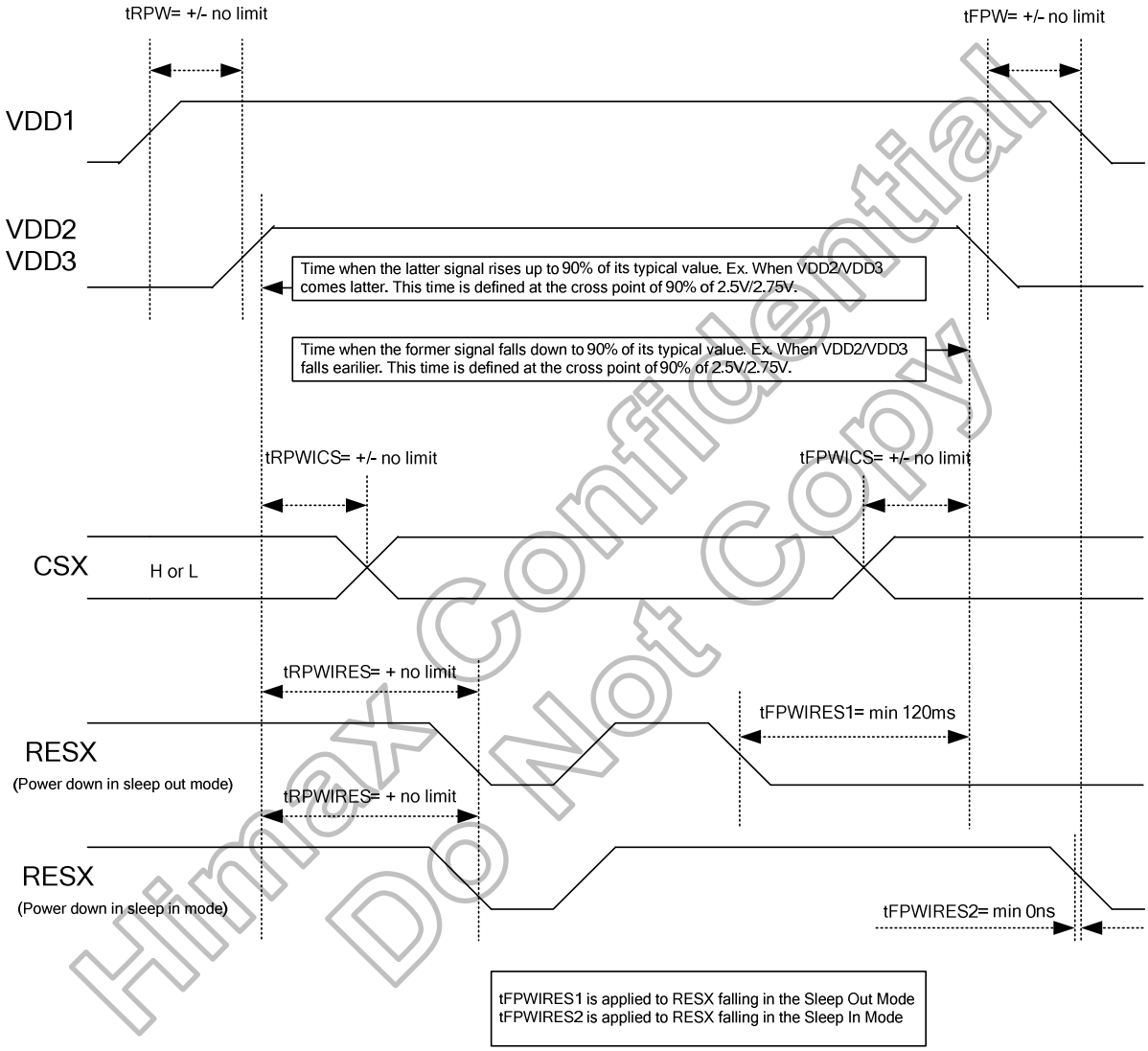


Figure 5.22: Case 1: RESX Line is Held High or Unstable by Host at Power On

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5.11.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.

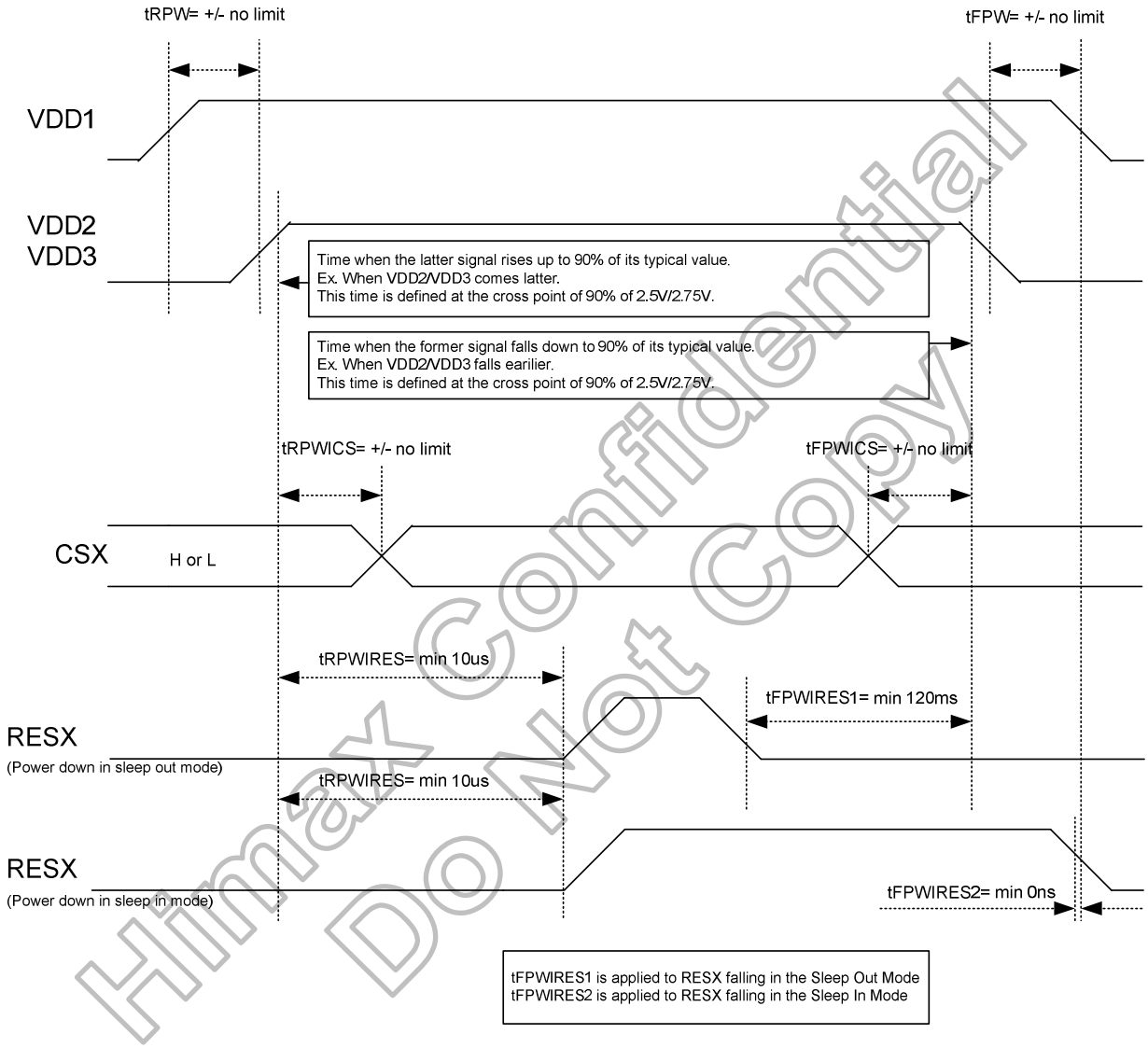


Figure 5.23: Case 2: RESX Line is Held Low by Host at Power On

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5.12 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power-On Sequence” powers it up.

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5.13 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

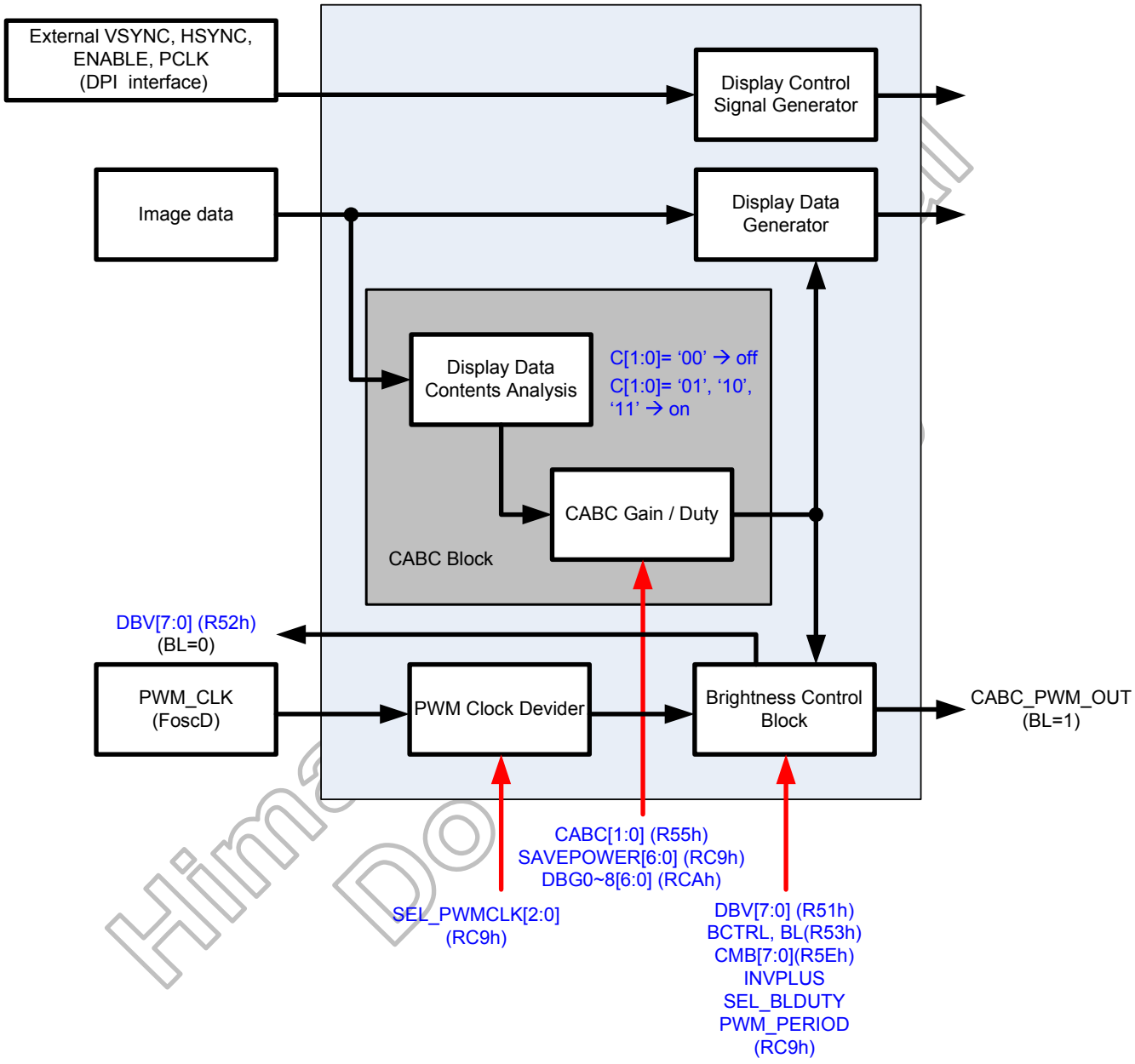


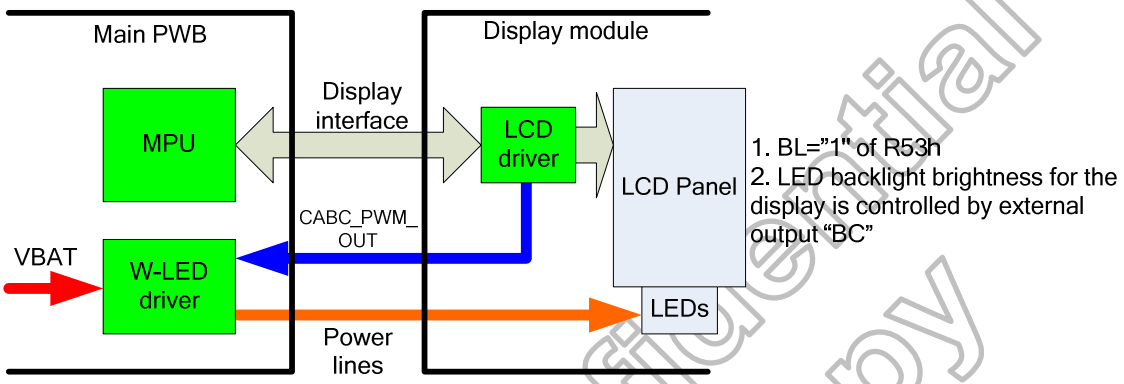
Figure 5.24: CABC Block Diagram

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5.13.1 Module architectures

The HX8379-C can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



- Architecture II

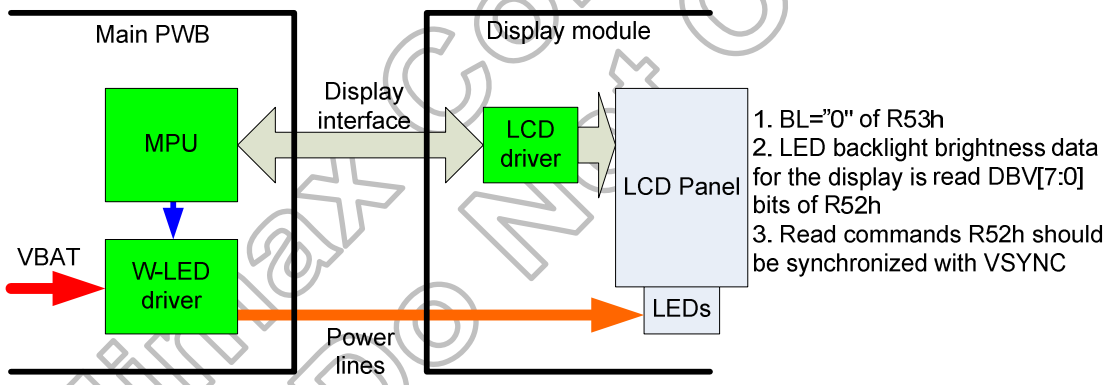


Figure 5.25: Module Architecture

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5.13.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value settings.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGx[6:0].

Please note that : Duty (valid level period (LED on) / one complete period)=1/ gain.

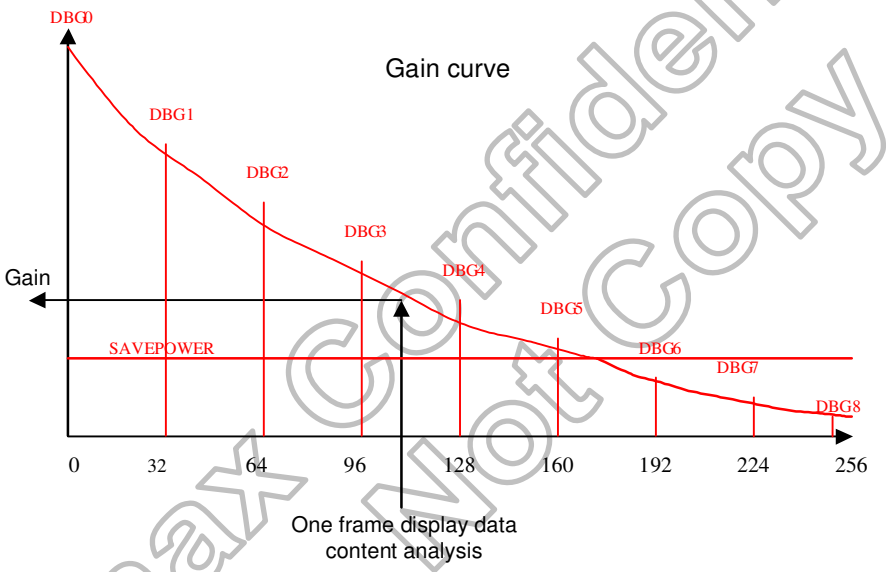


Figure 5.26: CABC Gain / CABC Duty Generation

For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

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5.13.3 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV[7:0]) / 255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty= (228) / 255 x 74.42% ≡ 66.54%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT = 0.99ms.

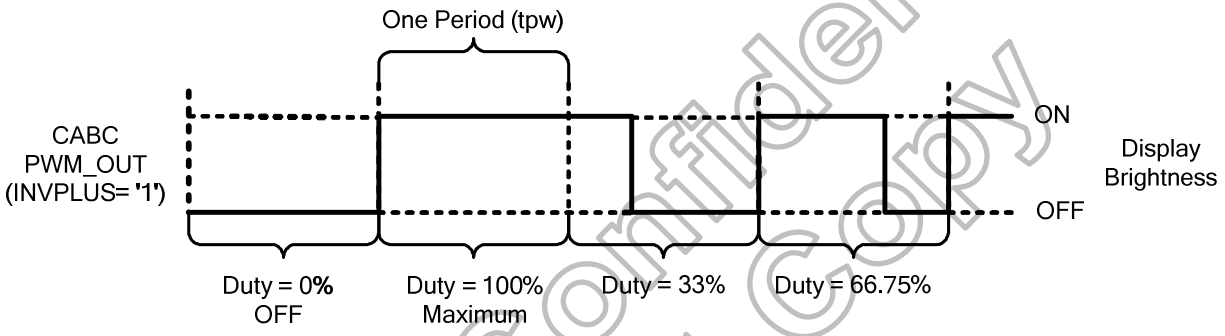


Figure 5.27: CABC_PWM_OUT Output Duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Table 5.52: CABC Timing Table

Note: (1) The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
(2) The pulse width range by setting CABC related registers is located between 0.0333ms to 8.33ms.

When Architecture II module is used (BL='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R51h) will be read a value as 169_{DEC} ((169) / 255 ≡ 66.27%).

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5.13.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL='0' of R53h), CABC minimum brightness setting is ignored. "CMB[7:0], Read CABC minimum brightness (R5Fh)" always read the setting value of "CMB[7:0], Write CABC minimum brightness (R5Eh)"

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5.14 OTP programming

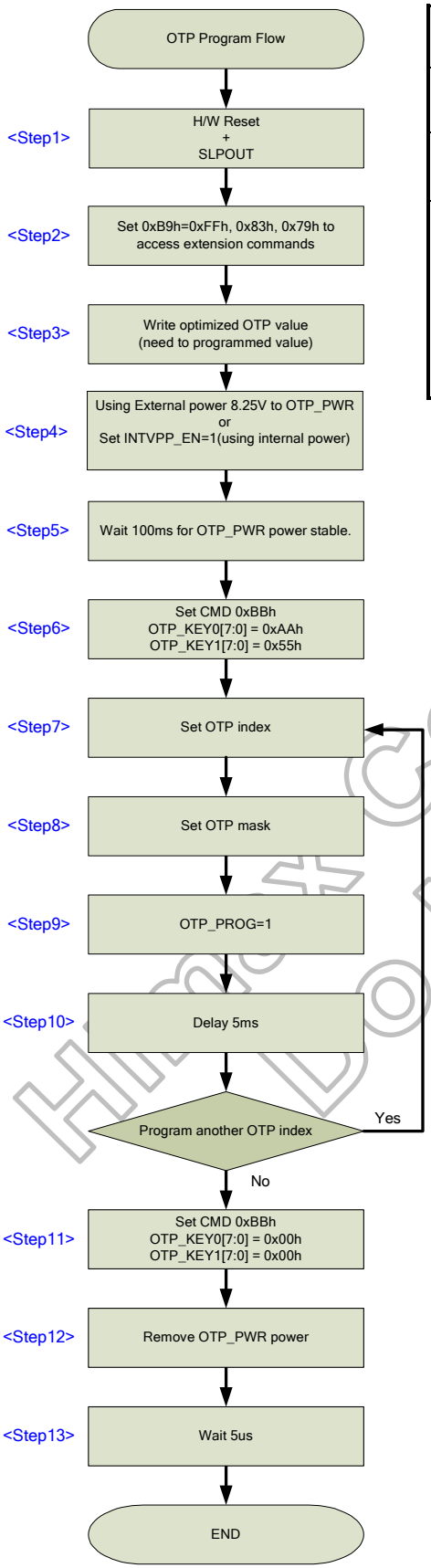
5.14.1 OTP table

OTP_INDEX (HEX)	CMD_REG	B7	B6	B5	B4	B3	B2	B1	B0
00	C3	ID1_1[7:0]							
01	C3	ID2_1[7:0]							
02	C3	ID3_1[7:0]							
03	C3	ID4_1[7:0]							
04	C3	ID1_2[7:0]							
05	C3	ID2_2[7:0]							
06	C3	ID3_2[7:0]							
07	C3	ID4_2[7:0]							
08	C3	ID1_3[7:0]							
09	C3	ID2_3[7:0]							
0A	C3	ID3_3[7:0]							
0B	C3	ID4_3[7:0]							
0C	C3	NVALID_ID1	NVALID_ID2	NVALID_ID3	-	-	-	-	-
0D	B6	VCMC_F1[7:0]							
0E	B6	VCMC_B1[7:0]							
0F	B6	VCMC_F2[7:0]							
10	B6	VCMC_B2[7:0]							
11	B6	VCMC_F3[7:0]							
12	B6	VCMC_B3[7:0]							
13	B6	-	-	VCMC_B38	VCMC_B38	VCMC_B28	VCMC_B28	VCMC_B18	VCMC_B18
14	B6	NVALID_VCMC1	NVALID_VCMC2	NVALID_VCMC3	-	-	-	-	-
15	CC	NVALID_PANEL	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL

Note: (1) The default value of OTP memory bits are all "1".
(2) NVALID bit decide the OTP reload Enable/Disable, the default value is "1". If the own OTP area of NVALID bit had been programmed, the NVALID bit will be changed to "0" automatically and execute the OTP reload.
(3) There are some conditions that HX8379-C can reload OTP.
a. Hardware reset.
b. Software reset.
c. SLPOUT command.

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5.14.2 OTP programming flow



OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	1. If HX8379-C operate on OTP program mode, then keep on OTP program mode. 2. If HX8379-C operate on non-OTP program mode, then keep on non-OTP program mode.

Figure 5.28: OTP Programming Sequence

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5.14.3 Programming sequence

Step	External Power OTP Program Sequence
1	Power on and reset the module.
2	SLPOUT and set 0xB9h = 0xFFh, 0x83h, 0x79h to access the extension commands.
3	Write optimized values to related registers.
4	Using the external power 8.25V to OTP_PWR.
5	Wait 100ms for OTP_PWR power stable.
6	Set CMD RBBh: OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to enter OTP program mode.
7	Specify OTP_index, please refer to the OTP table.
8	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
9	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
10	Wait 5 ms(1)
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (7). Otherwise, Set CMD RBBh: OTP_KEY0[7:0]=0x00h and OTP_KEY1[7:0]=0x00h to leave OTP program mode.
12	Remove the external power on OTP_PWR pin.
13	Wait 5us

Step	Internal Power OTP Program Sequence
1	Power on and reset the module.
2	Set RB9h = 0xFFh, 0x83h, 0x79h to access the extension commands.
3	Set RB1h, the value should be same as initial code setting
4	Set RD5h and RD6h PA 1th to PA 32th value to 0x88. Other parameters are same as initial code setting.
5	Set INTVPP_EN=1 for OTP programming state for using internal power mode.
6	Set CMD R11h SLP OUT to boost VGH to 8.25V for internal OTP power
7	Wait 100ms for OTP_PWR power stable.
8	Write optimized values to related registers.
9	Set CMD RBBh: OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to enter OTP program mode.
10	Specify OTP_index, please refer to the OTP table.
11	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
12	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
13	Wait 5 ms (**Note 1**)
14	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (7). Otherwise, Set CMD RBBh: OTP_KEY0[7:0]=0x00h and OTP_KEY1[7:0]=0x00h to leave OTP program mode.
15	Set INTVPP_EN=0 to disable internal OTP_PWR.
16	Wait 5us

Note: (1) During the OTP programming process, it must be added 5ms delay time after setting OTP_PROG=1.
(2) During the OTP program on VCMC setting: VCMC(SET1), VCMC(SET2), VCMC(SET3), user just need to specify the OTP index 0Dh. All settings of SETVCOM will be programmed to VCMC(SET1), VCMC(SET2), and VCMC(SET3) automatically.
(3) During the OTP program on ID1~4 setting: ID1~4(SET1): 00h~03h, ID1~4(SET2): 04h~07h, and ID1~4(SET3): 08h~0Bh, user just need to specify the OTP index 00h. All settings of ID1~4 will be programmed to ID1~4(SET1), ID1~4(SET2) and ID1~4(SET3) automatically.

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5.14.4 OTP programming example of VCOM setting VCMC

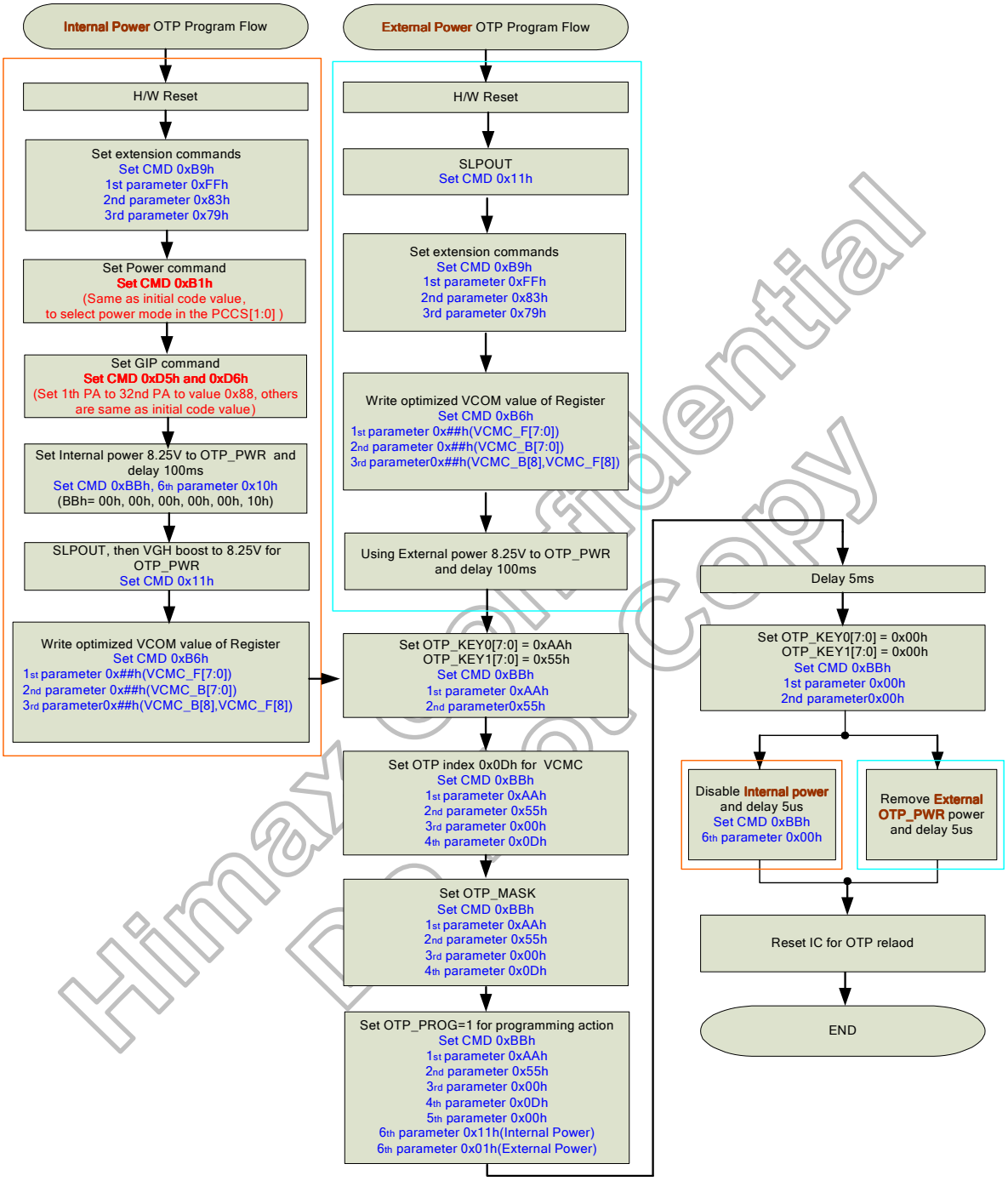


Figure 5.29: OTP Programming Sequence Example 1

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5.14.5 OTP programming example of ID1, ID2, ID3 and ID4

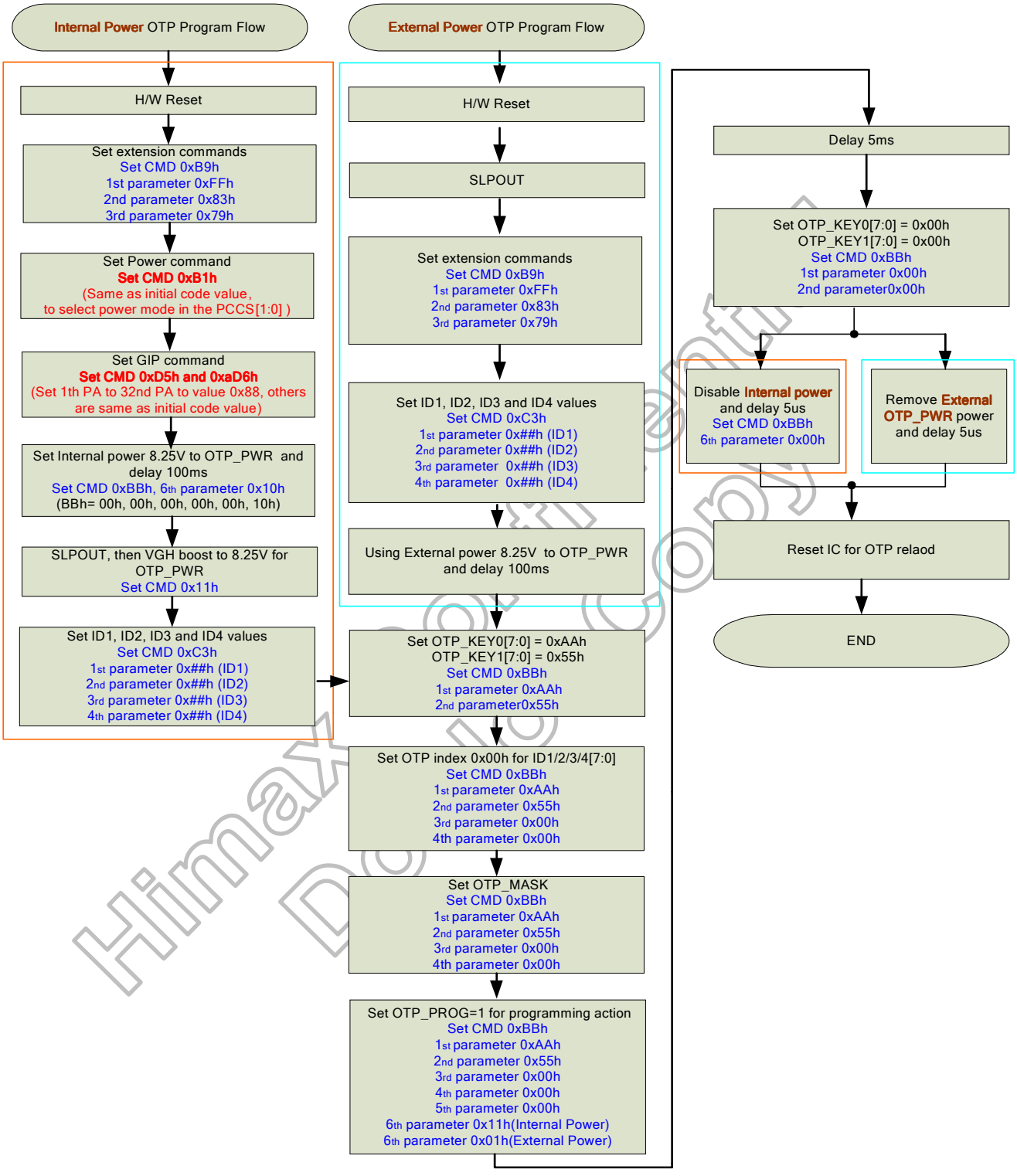


Figure 5.30: OTP Programming Sequence Example 2

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5.14.6 OTP read example of 0x0Dh (VCMC)

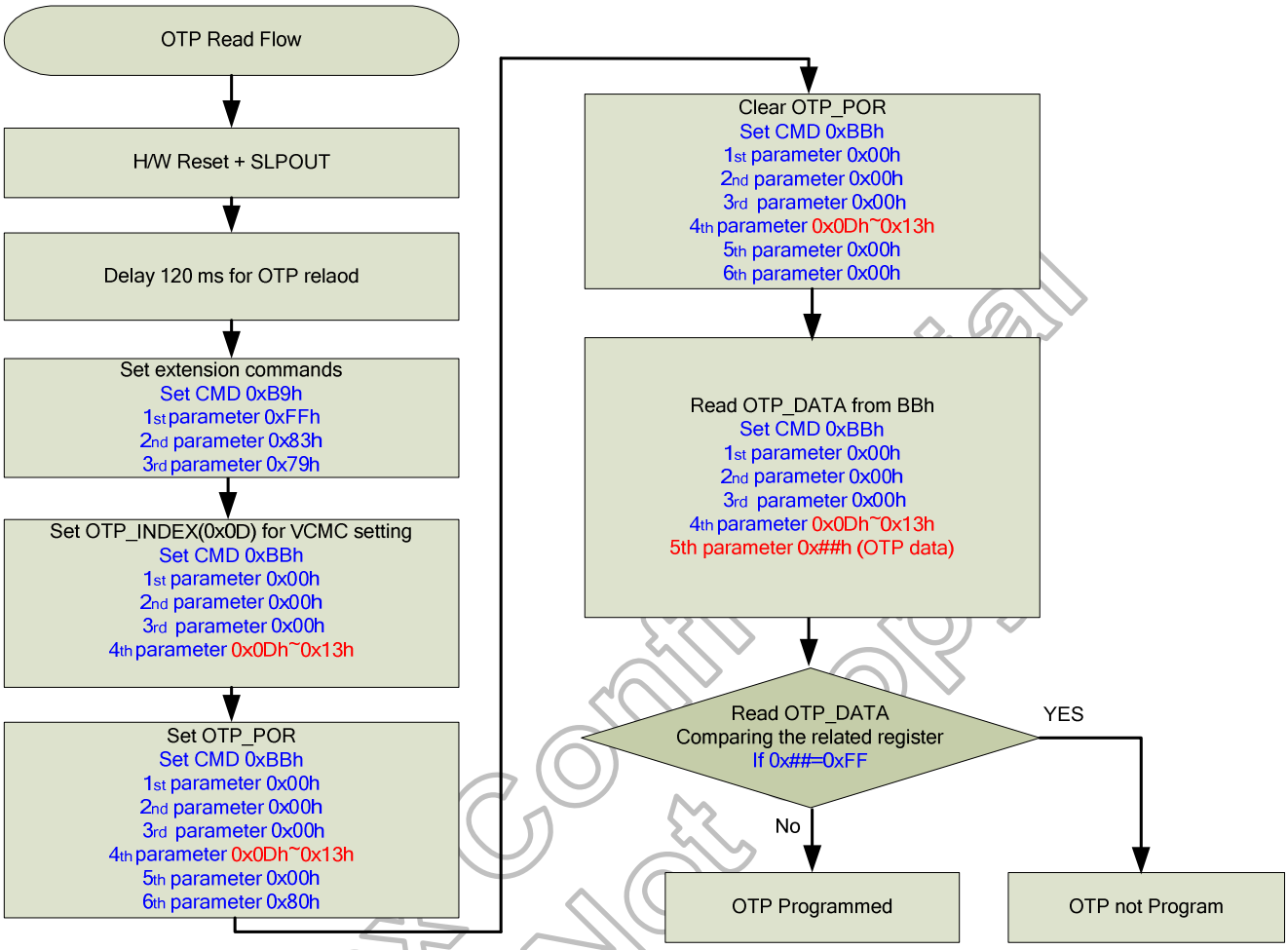


Figure 5.31: OTP Read Sequence of Index 0x0Dh

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6. Command

6.1 Command list

6.1.1 Standard command

(Hex)	Operation Code	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
00	NOP	0	1	↑	0	0	0	0	0	0	0	0	No Operation	-
01	SWRESET	0	1	↑	0	0	0	0	0	0	0	1	Software Reset	-
04	RDDIDIF	0	1	↑	0	0	0	0	0	1	0	0	Read Display Identification Information	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	ID1[7:0]									-
		1	↑	1	ID2[7:0]									-
		1	↑	1	ID3[7:0]									-
05	RDNUMPE	0	1	↑	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	P[7:0]									-
06	RDRED	0	1	↑	0	0	0	0	0	1	1	0	Read Red Colour	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	xx	-
07	RDGREEN	0	1	↑	0	0	0	0	0	1	1	1	Read Green Colour	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	G7	G6	G5	G4	G3	G2	G1	G0	xx	-
08	RDBLUE	0	1	↑	0	0	0	0	1	0	0	0	Read Blue Colour	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	-
09	RDDST	0	1	↑	0	0	0	0	1	0	0	1	Read display status	-
		1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read	-
		1	↑	1	D[31:24]									-
		1	↑	1	D[23:16]									-
		1	↑	1	D[15:8]									-
		1	↑	1	D[7:0]									-
0A	RDDPM	0	1	↑	0	0	0	0	1	0	1	0	Read display power mode	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0		-
0B	RDDMADCTL	0	1	↑	0	0	0	0	1	0	1	1	Read display MADCTL	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0		-
0C	RDDCOLMOD	0	1	↑	0	0	0	0	1	1	0	0	Read display pixel format	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0		-
0D	RDDIM	0	1	↑	0	0	0	0	1	1	0	1	Read display image mode	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0		-
0E	RDDSM	0	1	↑	0	0	0	0	1	1	1	0	Read display signal mode	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0		-
0F	RDDSDR	0	1	↑	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	bit0 for checksums function	-
10	SLPIN	0	1	↑	0	0	0	1	0	0	0	0	Sleep In	-
11	SLPOUT	0	1	↑	0	0	0	1	0	0	0	1	Sleep Out	-
13	NORON	0	1	↑	0	0	0	1	0	0	1	1	Normal display mode on	-
20	INVOFF	0	1	↑	0	0	1	0	0	0	0	0	Display inversion off	-
21	INVON	0	1	↑	0	0	1	0	0	0	0	1	Display inversion on	-

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22	ALLPOFF	0	1	↑	0	0	1	0	0	0	1	0	All pixel off (black)	-
23	ALLPON	0	1	↑	0	0	1	0	0	0	1	1	All pixel on (white)	-
26	GAMSET	0	1	↑	0	0	1	0	0	1	1	0	Gamma set	-
		1	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		-
28	DISPOFF	0	1	↑	0	0	1	0	1	0	0	0	Display off	-
29	DISPON	0	1	↑	0	0	1	0	1	0	0	1	Display on	-
34	TEOFF	0	1	↑	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-
35	TEON	0	1	↑	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-
		1	1	↑	X	X	X	X	X	X	X	M		-
36	MADCTL	0	1	↑	0	0	1	1	0	1	1	0	Memory Access Control	-
		1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0		-
38	IDMOFF	0	1	↑	0	0	1	1	1	0	0	0	Idle mode off	-
39	IDMON	0	1	↑	0	0	1	1	1	0	0	1	Idle mode on	-
3A	COLMOD	0	1	↑	0	0	1	1	1	0	1	0	-	-
		1	1	↑	X	D6	D5	D4	X	D2	D1	D0	-	-
44	TESL	0	1	↑	0	1	0	0	0	1	0	0	TESL	-
		1	1	↑	TELINE[15:8](8'b0)									-
		1	1	↑	TELINE[7:0](8'b0)									-
45	GETSCAN	0	1	↑	0	1	0	0	0	1	0	1	Reture the current scanline SLN[15:0]	-
		1	1	↑	SLN[15:8]									-
		1	1	↑	SLN[7:0]									-
4F	DSTBON	0	1	↑	0	1	0	0	1	1	1	1	Deep Standby Mode On	-
51	WRDISBV	0	1	↑	0	1	0	1	0	0	0	1	Write Display Brightness	-
		1	1	↑	DBV[7:0]									-
52	RDDISBV	0	1	↑	0	1	0	1	0	0	1	0	Read Display Brightness Value	-
		1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read	-
		1	↑	1	DBV[7:0]									-
53	WRCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Write CTRL Display	-
		1	1	↑	xx	xx	BCTRL	xx	DD	BL	xx	xx		-
54	RDCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Read Control Value Display	-
		1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read	-
		1	↑	1	0	0	BCTRL	0	DD	BL	0	0		-
55	WRCABC	0	1	↑	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-
		1	1	↑	0	0	0	0	0	0	CABC[1:0]			-
56	RDCABC	0	1	↑	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	↑	1	0	0	0	0	0	0	C1	C0		-
5E	WRCABCMB	0	1	↑	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-
		1	1	↑	CMB[7:0]									-
5F	RDCABCMB	0	1	↑	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	↑	1	CMB[7:0]									-
68	RDABCSDR	0	1	↑	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX		-
		1	↑	1	D[7:6]		0	0	0	0	0	0		-
A1	Read_DDB_start	0	1	↑	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	↑	1	x	x	x	x	x	x	x	x		-
		1	↑	1	x	x	x	x	x	x	x	x		-
		1	↑	1	x	x	x	x	x	x	x	x		-
A8	Read_DDB_continue	0	1	↑	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	↑	1	x	x	x	x	x	x	x	x		-

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		1	↑	1	x	x	x	x	x	x	x	x		-
		1	↑	1	x	x	x	x	x	x	x	x		-
AA	RDFCS	0	1	↑	1	0	1	0	1	0	1	0	Read first checksum	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	xx	-
AF	RDCCS	0	1	↑	1	0	1	0	1	1	1	1	Read continus checksum	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-
		1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	xx	-
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1	-
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	1	↑	module's manufacturer[7:0]									-
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2	-
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	1	↑	LCD module/driver version [7:0]									-
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3	-
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-
		1	1	↑	LCD module/driver ID[7:0]									-

Note: (1) Undefined commands are treated as NOP (00h) command.
(2) B0h to FFh are for factory use of display supplier.

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6.1.2 User define command and Internal command List Table

User define command and internal command are available only by setting “SETEXTC” command.

Index (Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Parameter Index	Default (Hex)
B0	SETAUTO	0	1	0	1	1	0	0	0	0		
		1	-	AUTO_OPT[6:0]							1	(00h)
		1	-	-	-	-	-	-	-	OSC_EN	2	(00h)
		1	-	-	-	-	-	-	-	STB	3	(01h)
		1	-	-	-	-	GON	DTE	D[1:0]		4	(0Ch)
B1	SETPOWER	0	1	0	1	1	0	0	0	1		
		1	DSTB	APF_EN	DD_TU	GASVCI_OPT[1:0]		AP[2:0]			1	(64h)
		1	HX5187_EN	VCI_LDOS[1:0]		VRHP[4:0]					2	(10h)
		1	-	DT[1:0]		VRHN[4:0]					3	(10h)
		1	PCCS[1:0]		EN_VSP_CLAMP	BTP[4:0]					4	(2Eh)
		1	XDK[2:0]			BTN[4:0]					5	(2Eh)
		1	XDKN[2:0]			EN_VSN_CLAMP	-		-	-	6	(50h)
		1	VCLS[2:0]			PMTU	VDDDNS[2:0]			-	7	(F0h)
		1	VGH_RATIO[1:0]	VGHS[4:0]						-	8	(5Ch)
		1	VGL_RATIO[1:0]	VGLS[4:0]						-	9	(5Ch)
		1	EN_NVREF	-		-		-	-	-	10	(80h)
		1	EN_VGH_REG	VGH_REGS[4:0]					-	-	11	(B8h)
		1	EN_VGL_REG	VGL_REGS[4:0]					-	-	12	(B8h)
		1	CLK_OPT5	CLK_OPT4	CLK_OPT3	CLK_OPT2	CLK_OPT1		-	-	13	(F8h)
		1	FS5[3:0]				FS4[3:0]				14	(22h)
		1	FS3[3:0]				FS2[3:0]				15	(22h)
		1	FS1[3:0]				FS0[3:0]				16	(22h)
B2	SETDISP	0	1	0	1	1	0	0	1	0		
		1	ZZ_LR	ZZ_EO	-			NW[2:0]			1	(80h)
		1	NL[7:0]								2	(44h)
		1	BP [7:0]								3	(08h)
		1	FP [7:0]								4	(03h)
		1	SAP[3:0]				vs_plus_bp_en	-	-	ABC_HS_BYPASS	5	(30h)
		1	RTN[7:0]								6	(50h)
B3	SETRGBIF	0	1	0	1	1	0	0	1	1		
		1	-	-	DPICC[1:0]		DPL	HSPL	VSPL	EPL		(01h)
B4	SETCYC	1	1	0	1	1	0	1	0	0		
		1	SPON[7:0]								1	(08h)
		1	SPOFF[7:0]								2	(30h)
		1	CON[7:0]								3	(08h)
		1	COFF[7:0]								4	(28h)
		1	CON1[7:0]								5	(05h)
		1	COFF1[7:0]								6	(36h)
		1	EQON1[7:0]								7	(04h)
		1	EQON2[7:0]								8	(58h)
		1	SON[7:0]								9	(08h)
		1	SOFF[7:0]								10	(58h)

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B6	SETVCOM (OTPx3)	0	1	0	1	1	0	1	1	0			
		1	VCMC_F[7:0]									1	(46h)
		1	VCMC_B[7:0]									2	(46h)
		1	VCOM_TIMES[2:0]			-	-	-	VCMC_B8	VCMC_F8		3	(00h)
B7	SETTE	0	1	0	1	1	0	1	1	1			
		1	-	-	TE_SEL[1:0]		TEI[3:0]					1	(00h)
		1	TEL_SEL[1:0]		-	-	-	TEP[10:8]				2	(00h)
		1	TEP[7:0]									3	(00h)
B8	SETGPO	0	1	0	1	1	1	1	0	1			
		1	GPO1SEL[3:0]				GPO0SEL[3:0]					1	(00h)
		1	GPO3SEL[3:0]				GPO2SEL[3:0]					2	(00h)
B9	SETEXTC	0	1	0	1	1	1	0	0	1			
		1	EXTC1[7:0]									1	(00h/FFh)
		1	EXTC2[7:0]									2	(00h/83h)
		1	EXTC3[7:0]									3	(00h/79h)
BB	SETOTP	0	1	0	1	1	1	0	1	1			
		1	OTP_KEY0[7:0]									1	(00h)
		1	OTP_KEY1[7:0]									2	(00h)
		1	OTP_MASK[7:0]									3	(00h)
		1	OTP_INDEX[7:0]									4	(00h)
		1	OTP_DATA[7:0]									5	(00h)
		1	OTP_POR	OTP_PWE	OTP_PWR_SEL	INTVPP_EN	OTP_PTM[1:0]		OTP_TEST	OTP_PROG		6	(00h)
BD	SET_BANK	0	1	1	1	1	0	0	0	1			
		1	-	-	-	-	-	-	BANK_INDEX[1:0]			1	(00h)
C1	SETDGCLUT	0	1	1	0	0	0	0	0	1			
		1	-	-	-	-	-	-	-	DGC_EN		Bank_0_1	(00h)
		1	0	0	0	0	R_GAMMA0[5:2]					Bank_0_2	--
		1	0	0	0	0	R_GAMMA1[5:2]					Bank_0_3	--
		1	0	0	0	R_GAMMA2[6:2]						Bank_0_4	--
		1	0	0	R_GAMMA3[7:2]							Bank_0_5	--
		1	0	0	R_GAMMA4[7:2]							Bank_0_6	--
		1	0	R_GAMMA5[8:2]								Bank_0_7	--
		1	0	R_GAMMA6[8:2]								Bank_0_8	--
		1	0	R_GAMMA7[8:2]								Bank_0_9	--
		1	0	R_GAMMA8[8:2]								Bank_0_10	--
		1	0	R_GAMMA9[8:2]								Bank_0_11	--
		1	0	R_GAMMA10[8:2]								Bank_0_12	--
		1	0	R_GAMMA11[8:2]								Bank_0_13	--
		1	0	R_GAMMA12[8:2]								Bank_0_14	--
		1	0	R_GAMMA13[8:2]								Bank_0_15	--
		1	R_GAMMA14[9:2]									Bank_0_16	--
		1	R_GAMMA15[9:2]									Bank_0_17	--
		1	R_GAMMA16[9:2]									Bank_0_18	--
		1	R_GAMMA17[9:2]									Bank_0_19	--
		1	R_GAMMA18[9:2]									Bank_0_20	--
		1	R_GAMMA19[9:2]									Bank_0_21	--
		1	R_GAMMA20[9:2]									Bank_0_22	--
		1	R_GAMMA21[9:2]									Bank_0_23	--
		1	R_GAMMA22[9:2]									Bank_0_24	--
		1	1	R_GAMMA23[8:2]								Bank_0_25	--
		1	1	R_GAMMA24[8:2]								Bank_0_26	--
		1	1	R_GAMMA25[8:2]								Bank_0_27	--
		1	1	R_GAMMA26[8:2]								Bank_0_28	--
		1	1	R_GAMMA27[8:2]								Bank_0_29	--
		1	1	R_GAMMA28[8:2]								Bank_0_30	--
		1	1	R_GAMMA29[8:2]								Bank_0_31	--

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1	1	R_GAMMA30[8:2]							Bank_0_32	--
1	1	R_GAMMA31[8:2]							Bank_0_33	--
1	1	R_GAMMA32[8:2]							Bank_0_34	--
1	R_GAMMA0[1:0]	R_GAMMA1[1:0]	R_GAMMA2[1:0]	R_GAMMA3[1:0]					Bank_0_35	--
1	R_GAMMA4[1:0]	R_GAMMA5[1:0]	R_GAMMA6[1:0]	R_GAMMA7[1:0]					Bank_0_36	--
1	R_GAMMA8[1:0]	R_GAMMA9[1:0]	R_GAMMA10[1:0]	R_GAMMA11[1:0]					Bank_0_37	--
1	R_GAMMA12[1:0]	R_GAMMA13[1:0]	R_GAMMA14[1:0]	R_GAMMA15[1:0]					Bank_0_38	--
1	R_GAMMA16[1:0]	R_GAMMA17[1:0]	R_GAMMA18[1:0]	R_GAMMA19[1:0]					Bank_0_39	--
1	R_GAMMA20[1:0]	R_GAMMA21[1:0]	R_GAMMA22[1:0]	R_GAMMA23[1:0]					Bank_0_40	--
1	R_GAMMA24[1:0]	R_GAMMA25[1:0]	R_GAMMA26[1:0]	R_GAMMA27[1:0]					Bank_0_41	--
1	R_GAMMA28[1:0]	R_GAMMA29[1:0]	R_GAMMA30[1:0]	R_GAMMA31[1:0]					Bank_0_42	--
1	R_GAMMA32[1:0]	-	-	-	-	-	-		Bank_0_43	--
1	0	0	0	0	G_GAMMA0[5:2]				Bank_1_1	--
1	0	0	0	0	G_GAMMA1[5:2]				Bank_1_2	--
1	0	0	0	G_GAMMA2[6:2]					Bank_1_3	--
1	0	0	G_GAMMA3[7:2]						Bank_1_4	--
1	0	0	G_GAMMA4[7:2]						Bank_1_5	--
1	0	G_GAMMA5[8:2]							Bank_1_6	--
1	0	G_GAMMA6[8:2]							Bank_1_7	--
1	0	G_GAMMA7[8:2]							Bank_1_8	--
1	0	G_GAMMA8[8:2]							Bank_1_9	--
1	0	G_GAMMA9[8:2]							Bank_1_10	--
1	0	G_GAMMA10[8:2]							Bank_1_11	--
1	0	G_GAMMA11[8:2]							Bank_1_12	--
1	0	G_GAMMA12[8:2]							Bank_1_13	--
1	0	G_GAMMA13[8:2]							Bank_1_14	--
1	G_GAMMA14[9:2]								Bank_1_15	--
1	G_GAMMA15[9:2]								Bank_1_16	--
1	G_GAMMA16[9:2]								Bank_1_17	--
1	G_GAMMA17[9:2]								Bank_1_18	--
1	G_GAMMA18[9:2]								Bank_1_19	--
1	G_GAMMA19[9:2]								Bank_1_20	--
1	G_GAMMA20[9:2]								Bank_1_21	--
1	G_GAMMA21[9:2]								Bank_1_22	--
1	G_GAMMA22[9:2]								Bank_1_23	--
1	1	G_GAMMA23[8:2]							Bank_1_24	--
1	1	G_GAMMA24[8:2]							Bank_1_25	--
1	1	G_GAMMA25[8:2]							Bank_1_26	--
1	1	G_GAMMA26[8:2]							Bank_1_27	--
1	1	G_GAMMA27[8:2]							Bank_1_28	--
1	1	G_GAMMA28[8:2]							Bank_1_29	--
1	1	G_GAMMA29[8:2]							Bank_1_30	--
1	1	G_GAMMA30[8:2]							Bank_1_31	--
1	1	G_GAMMA31[8:2]							Bank_1_32	--
1	1	G_GAMMA32[8:2]							Bank_1_33	--
1	G_GAMMA0[1:0]	G_GAMMA1[1:0]	G_GAMMA2[1:0]	G_GAMMA3[1:0]					Bank_1_34	--
1	G_GAMMA4[1:0]	G_GAMMA5[1:0]	G_GAMMA6[1:0]	G_GAMMA7[1:0]					Bank_1_35	--
1	G_GAMMA8[1:0]	G_GAMMA9[1:0]	G_GAMMA10[1:0]	G_GAMMA11[1:0]					Bank_1_36	--
1	G_GAMMA12[1:0]	G_GAMMA13[1:0]	G_GAMMA14[1:0]	G_GAMMA15[1:0]					Bank_1_37	--
1	G_GAMMA16[1:0]	G_GAMMA17[1:0]	G_GAMMA18[1:0]	G_GAMMA19[1:0]					Bank_1_38	--
1	G_GAMMA20[1:0]	G_GAMMA21[1:0]	G_GAMMA22[1:0]	G_GAMMA23[1:0]					Bank_1_39	--
1	G_GAMMA24[1:0]	G_GAMMA25[1:0]	G_GAMMA26[1:0]	G_GAMMA27[1:0]					Bank_1_40	--
1	G_GAMMA28[1:0]	G_GAMMA29[1:0]	G_GAMMA30[1:0]	G_GAMMA31[1:0]					Bank_1_41	--
1	G_GAMMA32[1:0]	-	-	-	-	-	-		Bank_1_42	--
1	0	0	0	0	B_GAMMA0[5:2]				Bank_2_1	--
1	0	0	0	0	B_GAMMA1[5:2]				Bank_2_2	--
1	0	0	0	B_GAMMA2[6:2]					Bank_2_3	--
1	0	0	B_GAMMA3[7:2]						Bank_2_4	--
1	0	0	B_GAMMA4[7:2]						Bank_2_5	--
1	0	B_GAMMA5[8:2]							Bank_2_6	--
1	0	B_GAMMA6[8:2]							Bank_2_7	--
1	0	B_GAMMA7[8:2]							Bank_2_8	--
1	0	B_GAMMA8[8:2]							Bank_2_9	--
1	0	B_GAMMA9[8:2]							Bank_2_10	--
1	0	B_GAMMA10[8:2]							Bank_2_11	--
1	0	B_GAMMA11[8:2]							Bank_2_12	--

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		1	0	B_GAMMA12[8:2]											Bank_2_13	--
		1	0	B_GAMMA13[8:2]											Bank_2_14	--
		1	B_GAMMA14[9:2]												Bank_2_15	--
		1	B_GAMMA15[9:2]												Bank_2_16	--
		1	B_GAMMA16[9:2]												Bank_2_17	--
		1	B_GAMMA17[9:2]												Bank_2_18	--
		1	B_GAMMA18[9:2]												Bank_2_19	--
		1	B_GAMMA19[9:2]												Bank_2_20	--
		1	B_GAMMA20[9:2]												Bank_2_21	--
		1	B_GAMMA21[9:2]												Bank_2_22	--
		1	B_GAMMA22[9:2]												Bank_2_23	--
		1	1	B_GAMMA23[8:2]											Bank_2_24	--
		1	1	B_GAMMA24[8:2]											Bank_2_25	--
		1	1	B_GAMMA25[8:2]											Bank_2_26	--
		1	1	B_GAMMA26[8:2]											Bank_2_27	--
		1	1	B_GAMMA27[8:2]											Bank_2_28	--
		1	1	B_GAMMA28[8:2]											Bank_2_29	--
		1	1	B_GAMMA29[8:2]											Bank_2_30	--
		1	1	B_GAMMA30[8:2]											Bank_2_31	--
		1	1	B_GAMMA31[8:2]											Bank_2_32	--
		1	1	B_GAMMA32[8:2]											Bank_2_33	--
		1	B_GAMMA0[1:0]		B_GAMMA1[1:0]		B_GAMMA2[1:0]		B_GAMMA3[1:0]						Bank_2_34	--
		1	B_GAMMA4[1:0]		B_GAMMA5[1:0]		B_GAMMA6[1:0]		B_GAMMA7[1:0]						Bank_2_35	--
		1	B_GAMMA8[1:0]		B_GAMMA9[1:0]		B_GAMMA10[1:0]		B_GAMMA11[1:0]						Bank_2_36	--
		1	B_GAMMA12[1:0]		B_GAMMA13[1:0]		B_GAMMA14[1:0]		B_GAMMA15[1:0]						Bank_2_37	--
		1	B_GAMMA16[1:0]		B_GAMMA17[1:0]		B_GAMMA18[1:0]		B_GAMMA19[1:0]						Bank_2_38	--
		1	B_GAMMA20[1:0]		B_GAMMA21[1:0]		B_GAMMA22[1:0]		B_GAMMA23[1:0]						Bank_2_39	--
		1	B_GAMMA24[1:0]		B_GAMMA25[1:0]		B_GAMMA26[1:0]		B_GAMMA27[1:0]						Bank_2_40	--
		1	B_GAMMA28[1:0]		B_GAMMA29[1:0]		B_GAMMA30[1:0]		B_GAMMA31[1:0]						Bank_2_41	--
		1	B_GAMMA32[1:0]		-	-	-	-	-	-					Bank_2_42	--
C3	SETID (OTPx3)	0	1	1	0	0	0	0	1	1						
		1	ID1[7:0]												1	(83h)
		1	ID2[7:0]												2	(79h)
		1	ID3[7:0]												3	(0Ch)
		1	ID4[7:0]												4	(00h)
		1	ID_TIMES[2:0]			-	-	-	-	-					5	(E0h)
C4	SETDDB	0	1	1	0	0	0	1	0	0						
		1	DDB1[7:0]												1	(00h)
		1	DDB2[7:0]												2	(00h)
		1	DDB3[7:0]												3	(00h)
		1	DDB4[7:0]												4	(00h)
C9	SETCABC	0	1	1	0	0	1	0	0	1						
		1	PWM_PERIOD[16]	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY					1	(1Fh)
		1	PWM_PERIOD[15:8]												2	(2Eh)
		1	PWM_PERIOD[7:0]												3	(1Eh)
		1	CABC_FSYNC	DIM_FRAME[6:0]											4	(1Eh)
		1	CABC_DD	-	-	BC_CTRL_EN	CABC_FLM[3:0]								5	(00h)
		1	CABC_STEP[7:0]												6	(1Eh)
CA	SETCABC GAIN	0	1	1	0	0	1	0	1	0						
		1	-	DBG0[6:0]											1	--
		1	-	DBG1[6:0]											2	--
		1	-	DBG2[6:0]											3	--
		1	-	DBG3[6:0]											4	--
		1	-	DBG4[6:0]											5	--
		1	-	DBG5[6:0]											6	--
		1	-	DBG6[6:0]											7	--
		1	-	DBG7[6:0]											8	--
		1	-	DBG8[6:0]											9	--
CB	SETCLOCK	0	1	1	0	0	1	0	1	1						
		1	-	-	-	-	UADJ[3:0]								1	(07h)

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CC	SETPANEL	0	1	1	0	0	1	1	0	0		
		1	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	1	(00h)
D3	SETGIP_0	0	1	1	0	1	0	0	1	1		
		1	-	-	-	-	-	-	VGLO_SEL	LVGL_SEL	1	--
		1	EQ_DELAY[7:0]								2	--
		1	-	-	GIP_EQ_MODE[1:0]		-	-	OVERLAP_OPT	-	3	--
		1	GTO[7:0]								4	--
		1	GNO[7:0]								5	--
		1	USER_GIP_GATE[7:0]								6	--
		1	USER_GIP_GATE1[7:0]								7	--
		1	SHR0_3[3:0]				SHR0_2[3:0]				8	--
		1	SHR0_1[3:0]				SHR0[11:8]				9	--
		1	SHR0[7:0]								10	--
		1	-				SHR0_GS[11:8]				11	--
		1	SHR0_GS[7:0]								12	--
		1	-				SHR1[11:8]				13	--
		1	SHR1[7:0]								14	--
		1	-				SHR1_GS[11:8]				15	--
		1	SHR1_GS[7:0]								16	--
		1	-				SHR2[11:8]				17	--
		1	SHR2[7:0]								18	--
		1	-				SHR2_GS[11:8]				19	--
		1	SHR2_GS[7:0]								20	--
		1	SHP0[3:0]				SCP[3:0]				21	--
		1	SHP2[3:0]				SHP1[3:0]				22	--
		1	CHR0[7:0]								23	--
		1	CHR0_GS[7:0]								24	--
		1	CHP0[3:0]				CCP0[3:0]				25	--
		1	CHR1[7:0]								26	--
		1	CHR1_GS[7:0]								27	--
		1	CHP1[3:0]				CCP1[3:0]				28	--
D5	SETGIP_1	0	1	1	0	1	0	1	0	1		
		1	GIP Setting								1~35	--
D6	SETGIP_2	0	1	1	0	1	0	1	0	1		
		1	GIP_GS Setting								1~32	--
E0	SETGAMMA (OTPx1)	0	1	1	1	0	0	0	0	0	Set Gamma Curve Related Setting	
		1	-	-	VRP0[5:0]						1	(05h)
		1	-	-	VRP1[5:0]						2	(0Ch)
		1	-	-	VRP2[5:0]						3	(13h)
		1	-	-	VRP3[5:0]						4	(20h)
		1	-	-	VRP4[5:0]						5	(39h)
		1	-	-	VRP5[5:0]						6	(3Fh)
		1	-	PRP0[6:0]							7	(24h)
		1	-	PRP1[6:0]							8	(39h)
		1	-	-	-	PKP0[4:0]					9	(08h)
		1	-	-	-	PKP1[4:0]					10	(0Ah)
		1	-	-	-	PKP2[4:0]					11	(0Ch)
		1	-	-	-	PKP3[4:0]					12	(16h)
		1	-	-	-	PKP4[4:0]					13	(10h)
		1	-	-	-	PKP5[4:0]					14	(16h)
		1	-	-	-	PKP6[4:0]					15	(1Ah)
		1	-	-	-	PKP7[4:0]					16	(17h)
		1	-	-	-	PKP8[4:0]					17	(17h)
		1	-	-	-	PKP9[4:0]					18	(06h)
		1	-	-	-	PKP10[4:0]					19	(0Dh)
		1	-	-	-	PKP11[4:0]					20	(0Fh)
		1	-	-	-	PKP12[4:0]					21	(12h)
		1	-	-	VRN0[5:0]						22	(05h)
		1	-	-	VRN1[5:0]						23	(0Ch)

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		1	-	-	VRN2[5:0]							24	(11h)
		1	-	-	VRN3[5:0]							25	(27h)
		1	-	-	VRN4[5:0]							26	(3Bh)
		1	-	-	VRN5[5:0]							27	(3Fh)
		1	-	PRN0[6:0]								28	(21h)
		1	-	PRN1[6:0]								29	(3Ah)
		1	-	-	-	PKN0[4:0]						30	(04h)
		1	-	-	-	PKN1[4:0]						31	(07h)
		1	-	-	-	PKN2[4:0]						32	(0Bh)
		1	-	-	-	PKN3[4:0]						33	(16h)
		1	-	-	-	PKN4[4:0]						34	(0Fh)
		1	-	-	-	PKN5[4:0]						35	(15h)
		1	-	-	-	PKN6[4:0]						36	(17h)
		1	-	-	-	PKN7[4:0]						37	(15h)
		1	-	-	-	PKN8[4:0]						38	(16h)
		1	-	-	-	PKN9[4:0]						39	(06h)
		1	-	-	-	PKN10[4:0]						40	(0Dh)
		1	-	-	-	PKN11[4:0]						41	(11h)
		1	-	-	-	PKN12[4:0]						42	(17h)
FD	SETCNCD/ GETCNCD	0	1	1	1	1	1	1	0	1			
		1	WR_CMD_CN[7:0]									1	--

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6.2 Standard Command Description

6.2.1 NOP (00h)

00H	NOP (No Operation)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.												
Restriction	-												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
	Sleep In or Booster Off								Yes				
Default	N/A												
Flow Chart	-												

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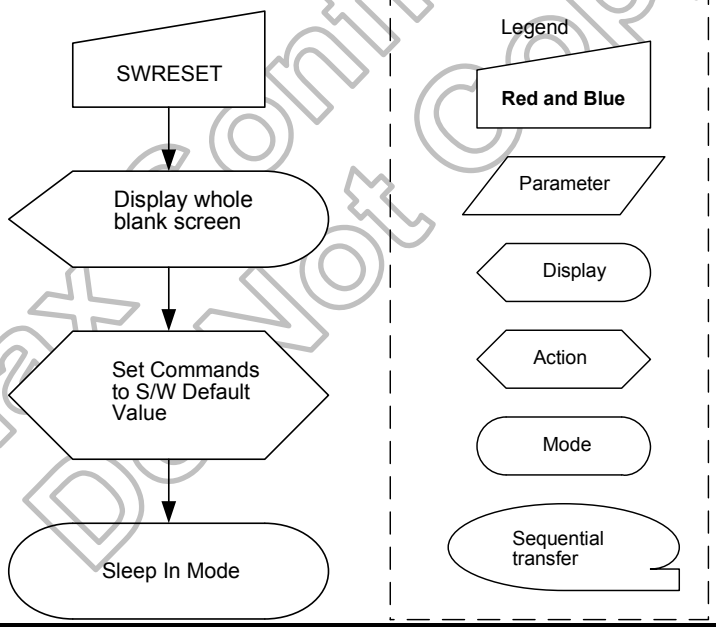
6.2.2 Software reset (01h)

01H	SWRESET (Software Reset)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command It will be necessary to wait 5msec before sending new command following software reset.												
Restriction	The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

Flow Chart



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6.2.3 Read Display Identification Information (04h)

04H	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	-	ID1[7:0]								xx
2nd parameter	1	↑	1	-	ID2[7:0]								xx
3rd parameter	1	↑	1	-	ID3[7:0]								xx

Description

This read byte returns 24-bit display identification information. The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX. The 3rd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6..0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value V[7:0]	Version	Changes
80h	-	-
81h	-	-
82h	-	-
83h	-	-
84h	-	-
85h	-	-

The 4th parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.

Restriction

-

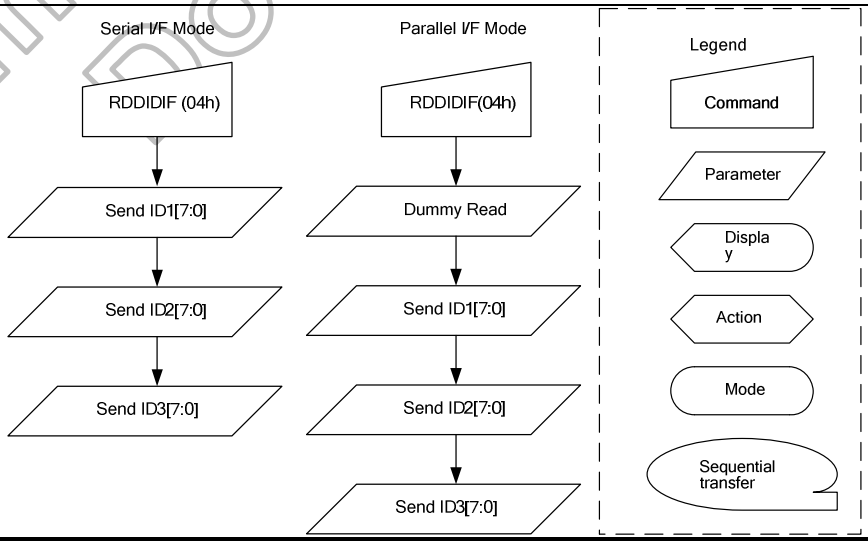
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	OTP Value
S/W Reset	OTP Value
H/W Reset	OTP Value

Flow Chart



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6.2.4 RDNUMPE: Read number of the parity errors (05h)

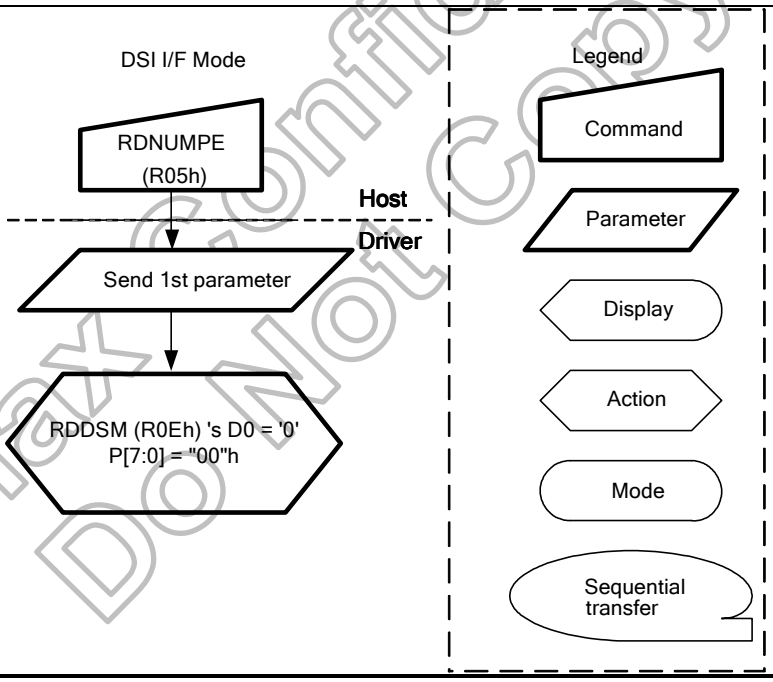
05H	RDNUMPE (Read Number of the Parity Errors)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	1	05
1st parameter	1	↑	1	-	P7	P6	P5	P4	P3	P2	P1	P0	xx
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (The read function is completed).												
Restriction	SETEXTC turn on to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

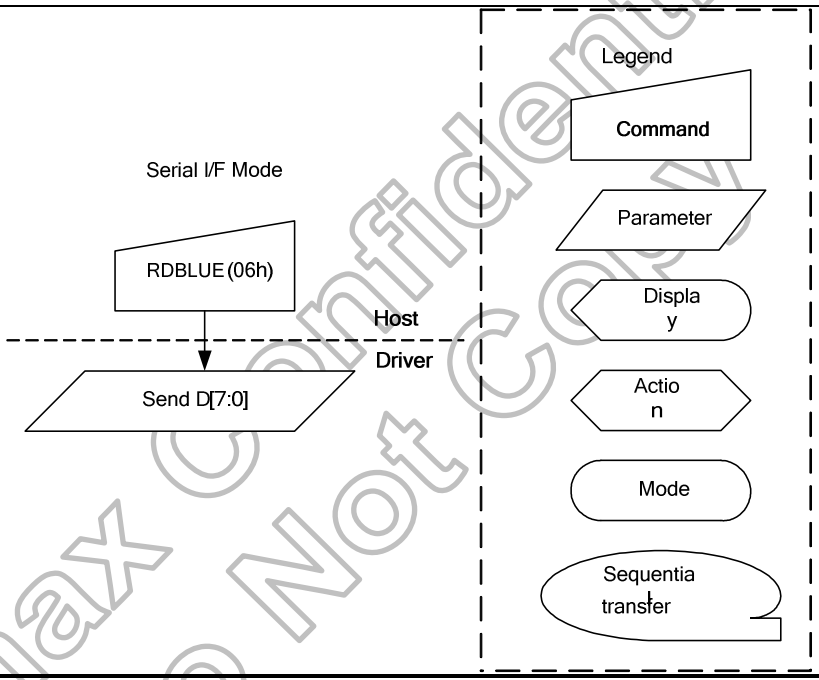
Default: P[7:0] = 0x00h

Flow Chart



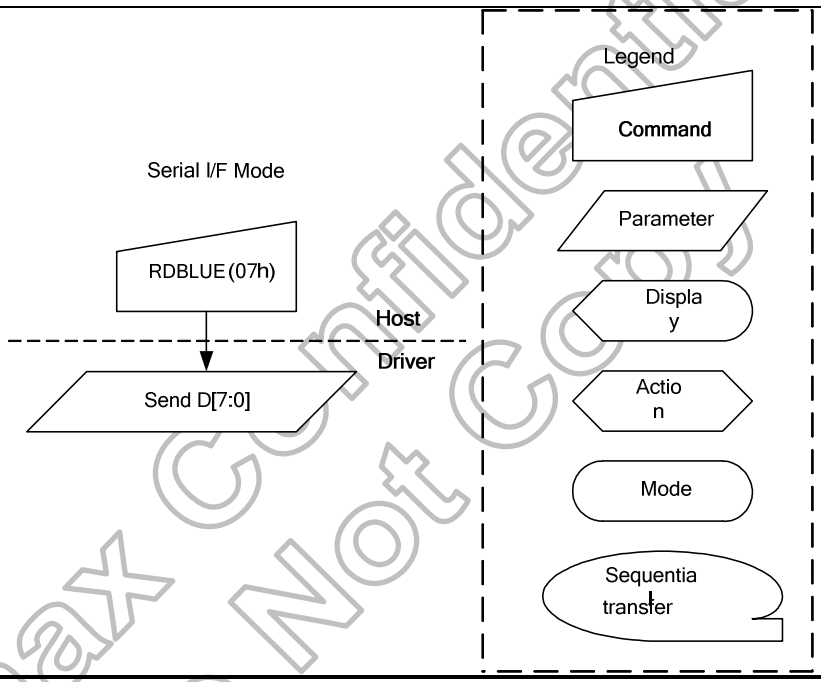
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6.2.5 Get_red_channel (06h)

06H	RDRED (Read Red Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	0	06
1st parameter	1	↑	1	-	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red colour value of the first pixel of the frame when DPI I/F is used. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	R[7:0] = 0x00h												
Flow Chart													

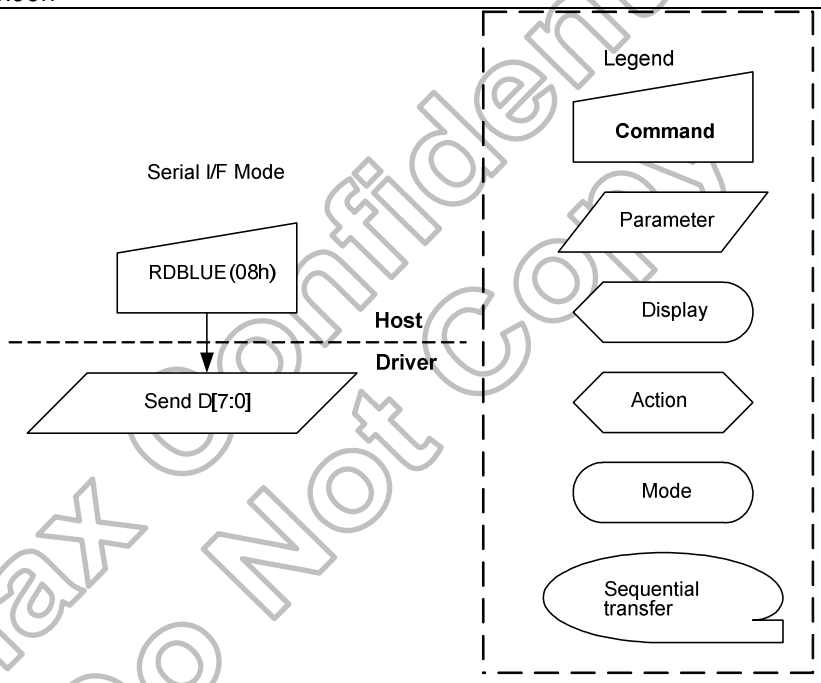
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6.2.6 Get_green_channel (07h)

07H	RDGREEN (Read Green Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	1	07
1st parameter	1	↑	1	-	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green colour value of the first pixel of the frame when DPI I/F is used. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	G[7:0] = 0x00h												
Flow Chart													

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6.2.7 Get_blue_channel (08h)

08H	RDBLUE (Read Blue Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	0	0	08
1st parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue colour value of the first pixel of the frame when DPI I/F is used. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	B[7:0] = 0x00h												
Flow Chart													

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6.2.8 Read Display Status (09h)

09H	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	-	D[31:24]								xx
2nd parameter	1	↑	1	-	D[23:16]								xx
3rd parameter	1	↑	1	-	D[15:8]								xx
4th parameter	1	↑	1	-	D[7:0]								xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D31	Booster Voltage Status	-
D30	Page Address Order	-
D29	Column Address Order	-
D28	Page/Column Order	-
D27	Display Device Line Refresh Order	-
D26	RGB/BGR Order	-
D25	Display Data Latch Data Order	-
D24	Source san sequence	-
D23	Gate san sequence	-
D22	Interface Colour Pixel Format Definition	-
D21		-
D20		-
D19	Idle Mode On/Off	-
D18	--	Set to '0'
D17	Sleep In/Out	-
D16	Display Normal Mode On/Off	-
D15	--	Set to '0'
D14	--	Set to '0'
D13	Inversion Status	-
D12	All Pixels On	-
D11	All Pixels Off	-
D10	Display On/Off	-
D9	Tearing Effect Line On/Off	-
D8	Gamma Curve Selection	-
D7		-
D6		-
D5	Tearing Effect Output Line Mode	-
D4	Horizontal Sync. (HSYNC, DPI I/F)	-
D3	Vertical Sync. (VSYNC, DPI I/F)	-
D2	Pixel Clock (DCK, DPI I/F)	-
D1	Data Enable (ENABLE, DPI I/F)	-
D0	Parity Error on DSI	-

Bit Values are explained overleaf.

Bit D31 – Booster Voltage Status
'0' = Booster Off.
'1' = Booster On.
Bit D30 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit D29 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit D28 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Rotation (When MADCTL B5='1').
Bit D27 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit D26 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').

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'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit D24 – Source san sequence
'0' = Source output Left to Right (When MADCTL B1='0').
'1' = Source output Right to Left (When MADCTL B1='1').
Bit D23 – Gate san sequence
'0' = Gate output Top to Bottom (When MADCTL B0='0').
'1' = Gate output Bottom to Top (When MADCTL B0='1').
Bits D22, D21, D20 – Interface Colour Pixel Format Definition

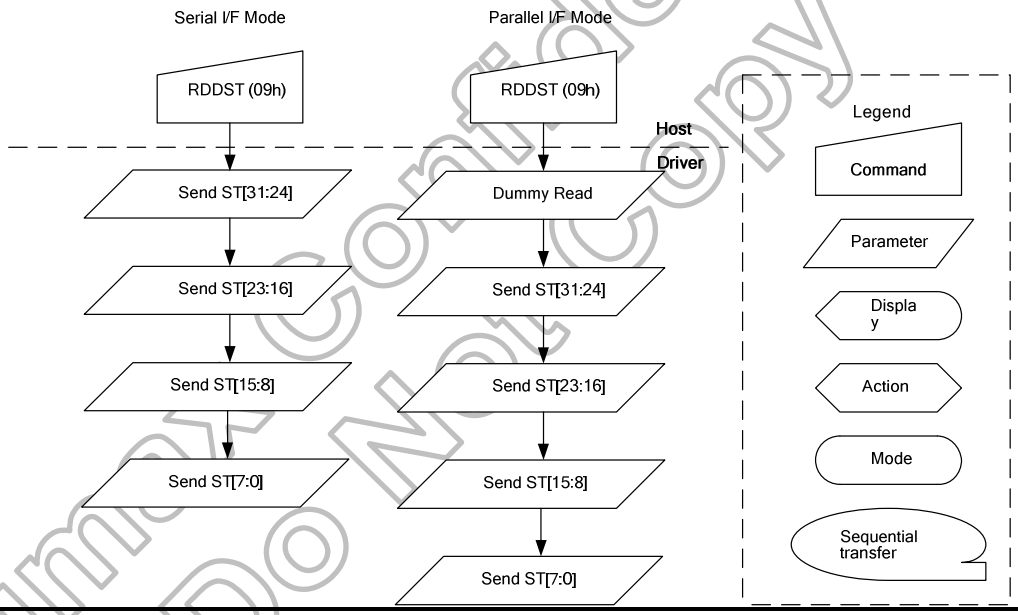
Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Bit D19 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D17 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D16 – Display Normal Mode On/Off
'0' = Partial or Scrolling Mode.
'1' = Normal Mode.
Bit D13 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
Bit D12 – All Pixels On.
'0' = Normal mode.
'1' = All Pixels On.
Bit D11 – All Pixels Off.
0' = Normal mode.
'1' = All Pixels Off.
Bit D10 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D9 – Tearing Effect Line On/Off
'0' =Tearing Effect Line Off.
'1' = Tearing Effect On.
Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	Reserved
Gamma Curve 2	0	0	1	Reserved
Gamma Curve 3	0	1	0	Reserved
Gamma Curve 4	0	1	1	Reserved
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Bit D5 – Tearing Effect Line Output Mode.
'0' = Mode 1, V-Blanking only.
'1' = Mode 2, both H-Blanking and V-Blanking.
Bit D4 – Horizontal Sync. (DPI I/F) On/Off, Note 1.
'0' = Horizontal Sync. Line is Off ("Low").
'1' = Horizontal Sync. Line is On ("High").
Bit D3 – Vertical Sync. (DPI I/F) On/Off, Note 1.
'0' = Vertical Sync. Line is Off ("Low").
'1' = Vertical Sync. Line is On ("High").
Bit D2 – Pixel Clock (PCLK, DPI I/F) On/Off, Note 1.
'0' = PCLK line is Off ("Low").

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	Bit D1 – Data Enable (DE, DPI I/F)) On/Off, Note 1. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0–Parity Error on DSI. '0'=No Parity Error. '1'=Parity Error. **Note:** This bit indicates current status of the line when this command has been sent.
Restriction	
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out – Yes Normal Mode On, Idle Mode On, Sleep Out – Yes Partial Mode On, Idle Mode Off, Sleep Out – Yes Partial Mode On, Idle Mode On, Sleep Out – Yes Sleep In or Booster Off – Yes
Default	Status / Default Value Power On Sequence – See description S/W Reset – See description H/W Reset – See description
Flow Chart	

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6.2.9 Get_power_mode (0Ah)

<table>
<tr><th rowspan="2">0AH</th><th colspan="13">RDDPM (Read Display Power Mode)</th></tr>
<tr><th>D/CX</th><th>RDX</th><th>WRX</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>--</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>-</td></tr>
<tr><td>D5</td><td>--</td><td>-</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>Set to ‘0’</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>-</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>-</td></tr>
<tr><td>D1</td><td>--</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>--</td><td>Set to ‘0’</td></tr>
</table>
Bits D7, D5, D1 and D0 for future use and are set to ‘0’.
Bit D6 – Idle Mode On/Off
‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.
Bit D4 – Sleep In/Out
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.
Bit D3 – Display Normal Mode On/Off
‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.
Bit D2 – Display On/Off
‘0’ = Display is Off.</td></tr>
<tr><td>Restrictions</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">D[7:0] = 0x08h</td></tr>
</table>

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6.2.10 Read display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	-
D1	Source scan sequence	-
D0	Gate scan sequence	-

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit D5 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Rotation (When MADCTL B5='1').
Note: For Bits D7 to D5, also refer to Section 5.3 MCU to memory write/read direction.
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').
Note: For Bits D4 and D3 also refer to Section 6.2.31 Set_address_mode (36h).
Bit D2 – Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit D1 – Source scan sequence
'0' = Source output Left to Right (When MADCTL B1='0').
'1' = Source output Right to Left (When MADCTL B1='1').
Bit D0 – Gate scan sequence
'0' = Gate output Top to Bottom (When MADCTL B0='0').

Restrictions

-

Register Availability

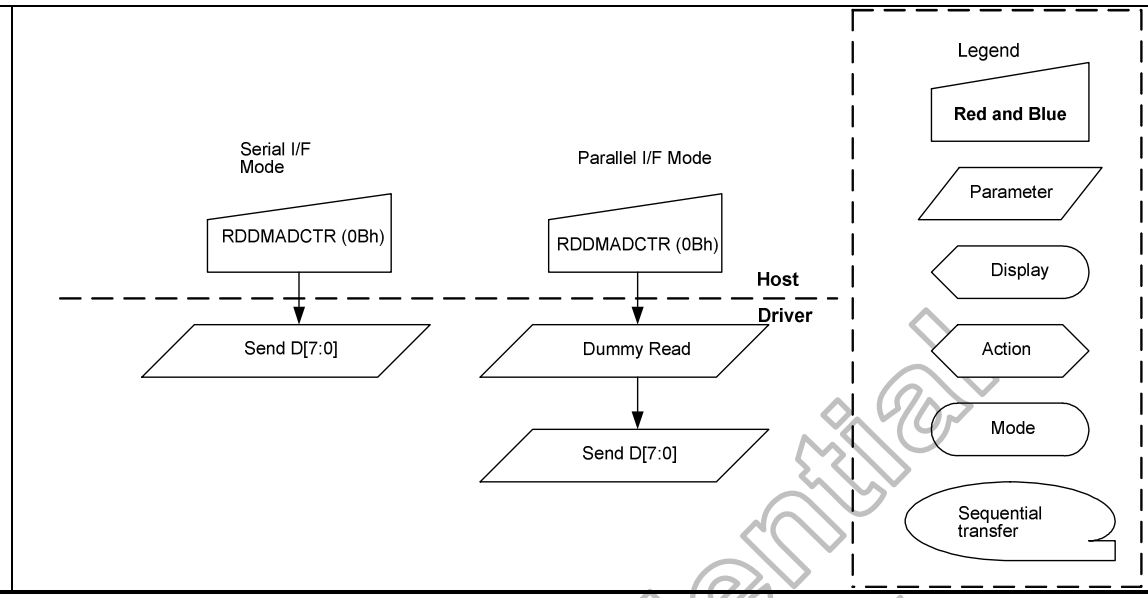
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

D[7:0] = 0x00h

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Flow Chart



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6.2.11 Get_pixel_format (0Ch)

0CH	RDDCOLMOD (Read Display COLMOD)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	-	D6	D5	D4	-	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	-
D5		-
D4		-
D3	Reserved	Set to '0'
D2		Set to '0'
D1		Set to '0'
D0		Set to '0'

Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
For Setting pixel format, see section 6.2.30 Set_pixel_format (3Ah)".

Interface Colour Format	D6	D5	D4
Not Defined	Others		
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.

Restrictions

-

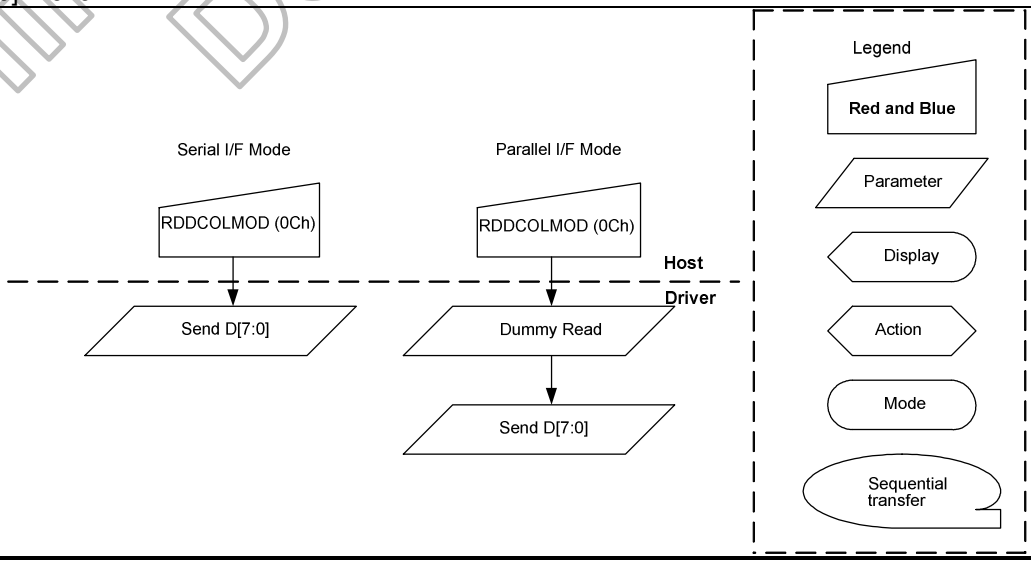
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

D[7:0] = 0x07h

Flow Chart



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6.2.12 Get_display_mode (0Dh)

0DH	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:
Bit D5 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
Bit D4 – All Pixels On
'0' = Normal Display
'1' = White Display
Bit D3 – All Pixels Off
'0' = Normal Display
'1' = Black Display
Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

-

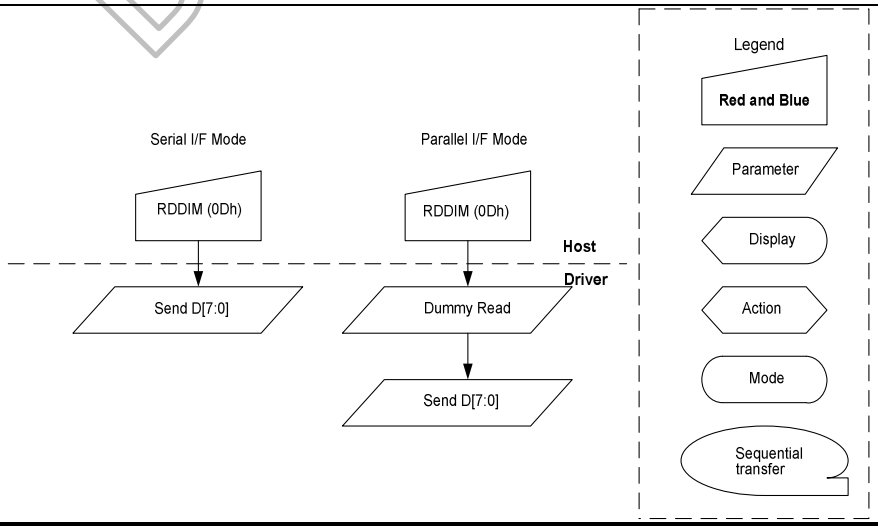
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

D[7:0] = 0x00h

Flow Chart



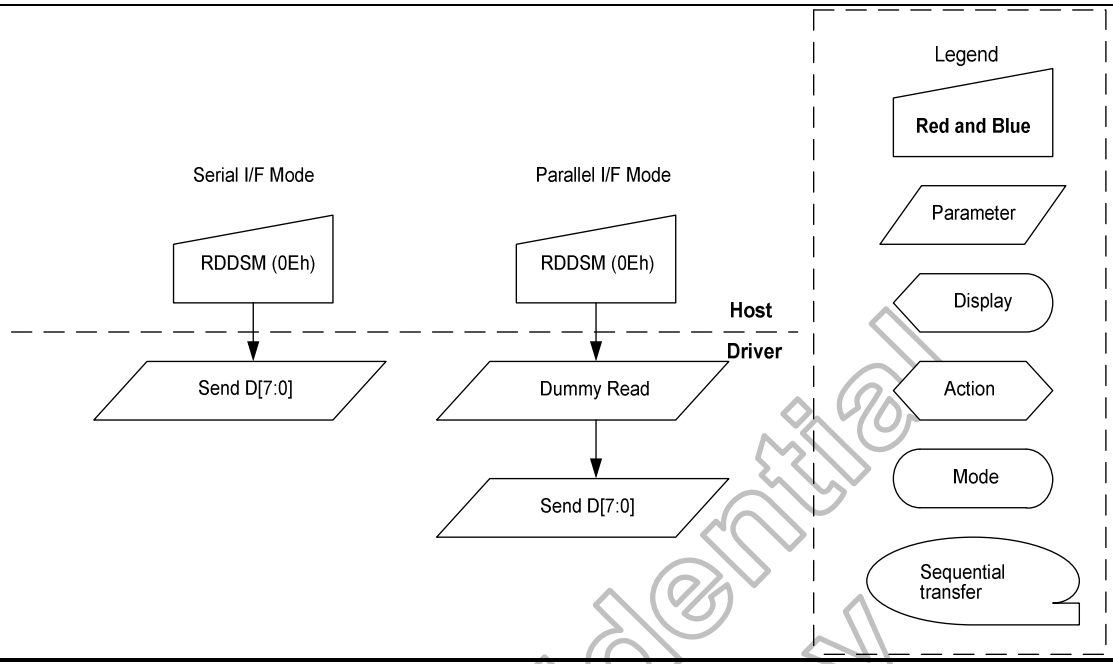
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6.2.13 Get_signal_mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx
Description	T This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 5.5.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. Bit D5 – Horizontal Sync. (RGB I/F) On/Off. '0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High"). Bit D4 – Vertical Sync. (RGB I/F) On/Off. '0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High"). Bit D3 – Pixel Clock (PCLK, RGB I/F) On/Off. '0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High"). Bit D2 – Data Enable (DE, RGB I/F)) On/Off. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0–Parity Error on DSI, see "Read number of the parity errors (05h)". '0'=No Parity Error. '1'=Parity Error. D1 is for future use and are set to '0'.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	D[7:0] = 0x00h												

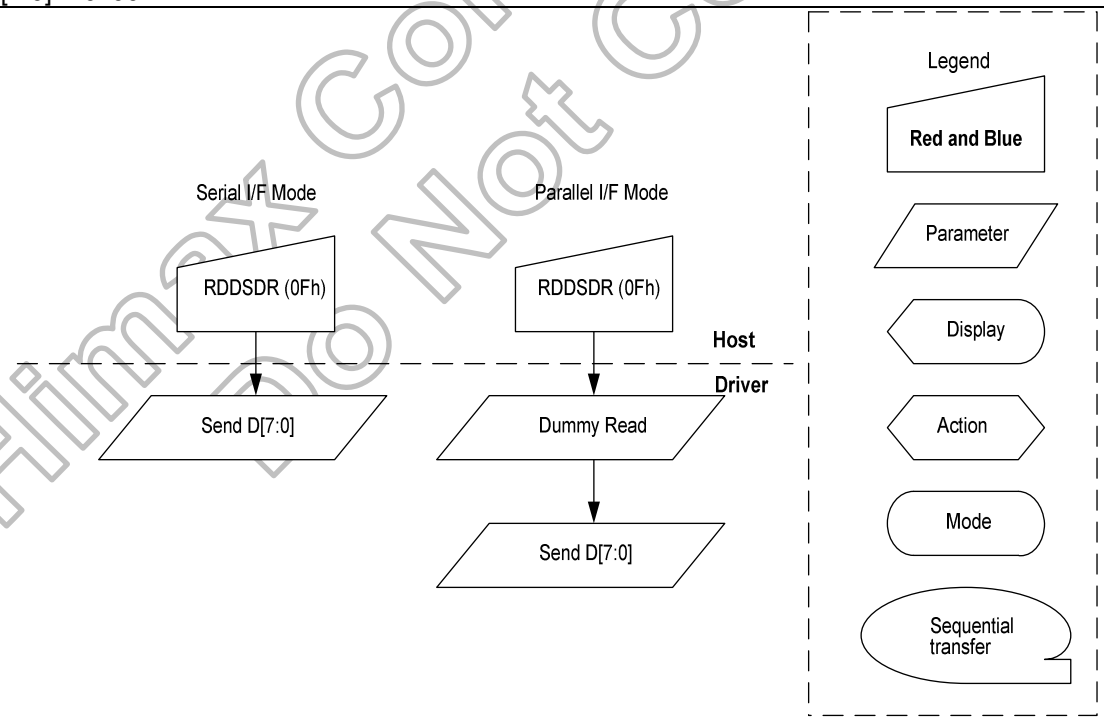
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Flow Chart



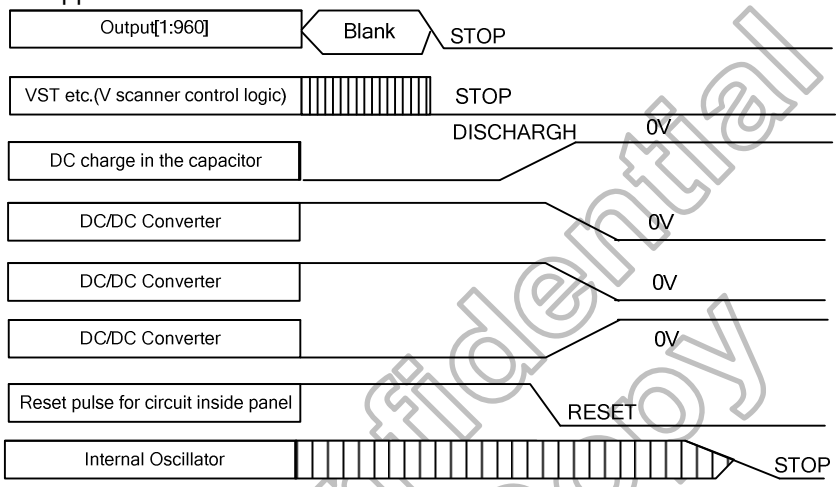
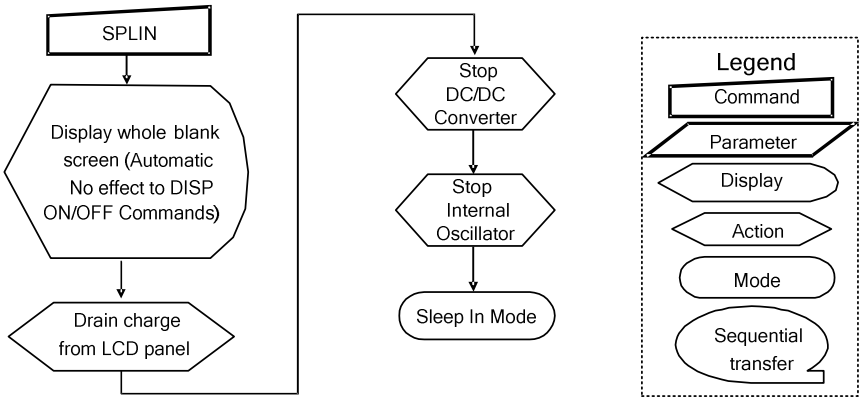
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6.2.14 Get_diagnostic_result (0Fh)

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	1	1	-	D7	D6	D5	D4	0	0	0	0	xx
Description	The display module returns the self-diagnostic results following a Sleep Out command. See section 5.15 for a description of the status results. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved Set to '0'.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

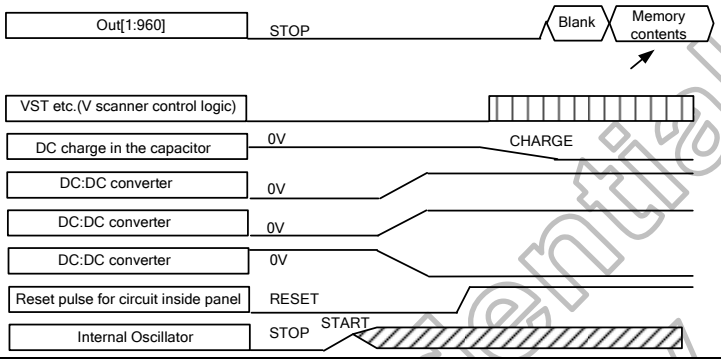
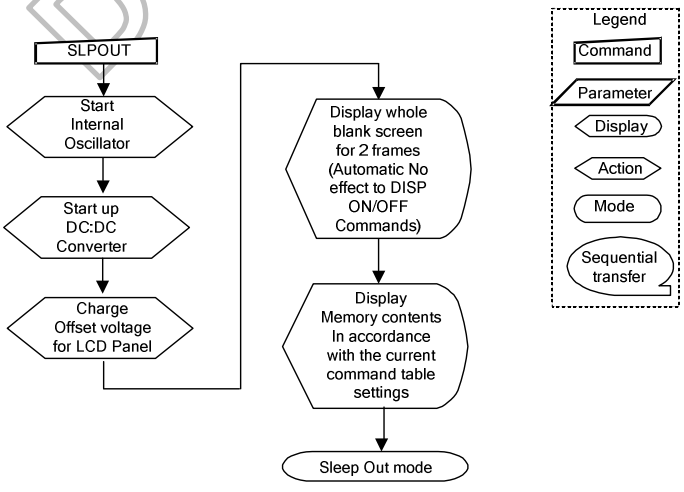
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6.2.15 Enter_sleep_mode (10h)

10H	SLPIN (Sleep In)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	N/A												
Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued. 												

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6.2.16 Exit_sleep_mode (11h)

11H	SLPOUT (Sleep Out)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	N/A												
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 												

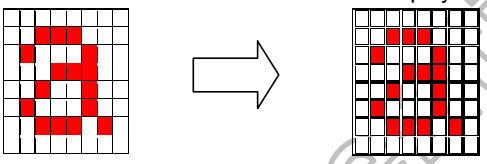
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6.2.17 Enter_normal_mode (13h)

13H	NORON (Normal Display Mode On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	N/A												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

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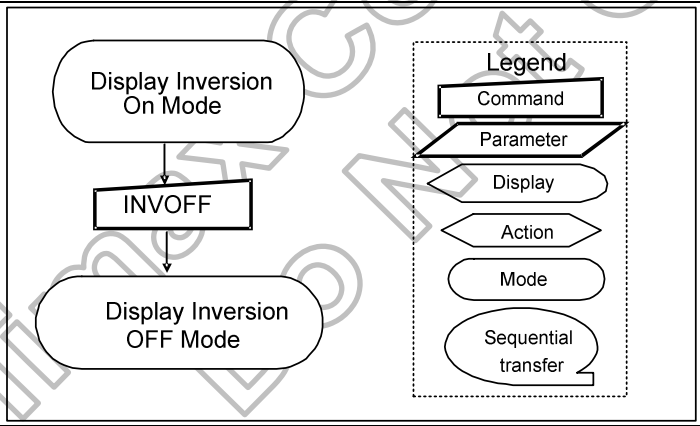
6.2.18 Exit_inversion_mode (20h)

20H	INVOFF (Display Inversion Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	No parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory (Example) Display 												
Restriction	This command has no effect when module is already in inversion off mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

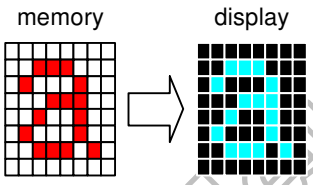
Default: N/A

Flow Chart



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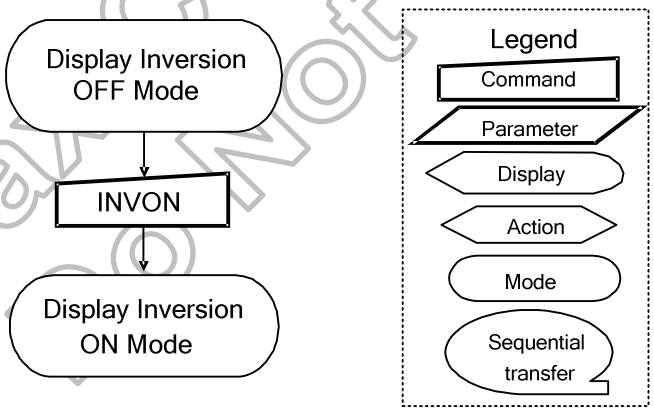
6.2.19 Enter_inversion_mode (21h)

21H	INVON (Display Inversion On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

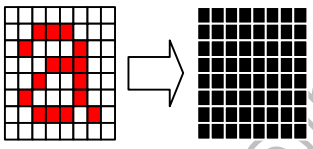
Default: N/A

Flow Chart



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6.2.20 All_Pixel_Off (22h)

22H	ALLPOFF (All Pixel Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	0	22
Parameter	NO PARAMETER												
Description	This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status (Example) memory display  'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.												
Restriction	This command has no effect when module is already in inversion on mode.												

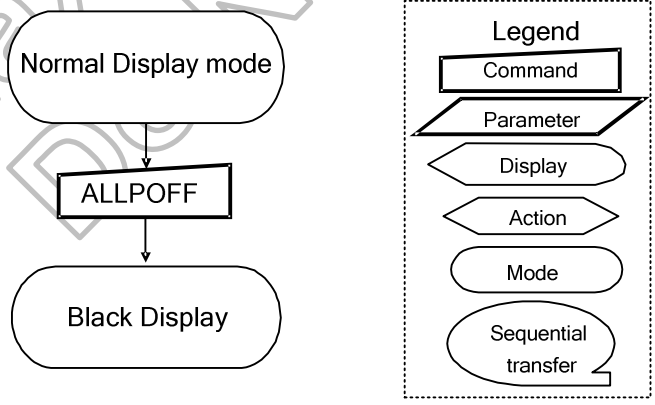
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

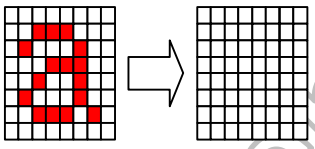
Status	Default Value
Power On Sequence	Off
S/W Reset	Off

Flow Chart



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6.2.21 All_Pixel_On (23h)

23H	ALLPON(All Pixel On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	1	23
Parameter	NO PARAMETER												
Description	This command turns the display panel white in 'Sleep out ' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display  'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.												
Restriction	This command has no effect when module is already in inversion on mode.												

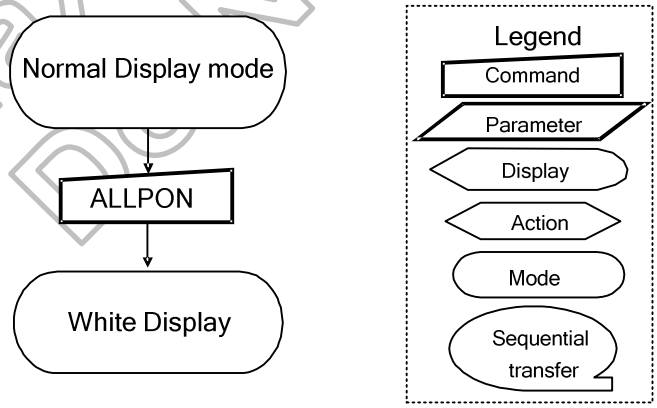
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off

Flow Chart



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6.2.22 Set_gamma_curve (26h)

26H	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	1	1	0	26
Parameter	1	1	↑	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1..08

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[7..0]	Parameter	Curve selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

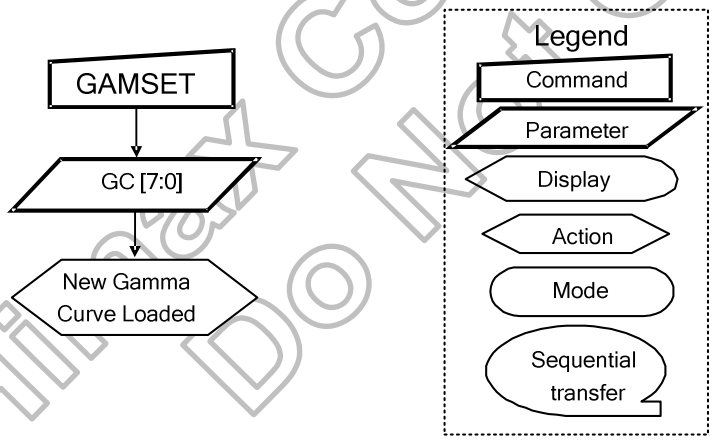
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

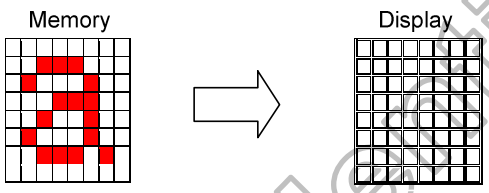
GC[7:0] = 0x01h

Flow Chart



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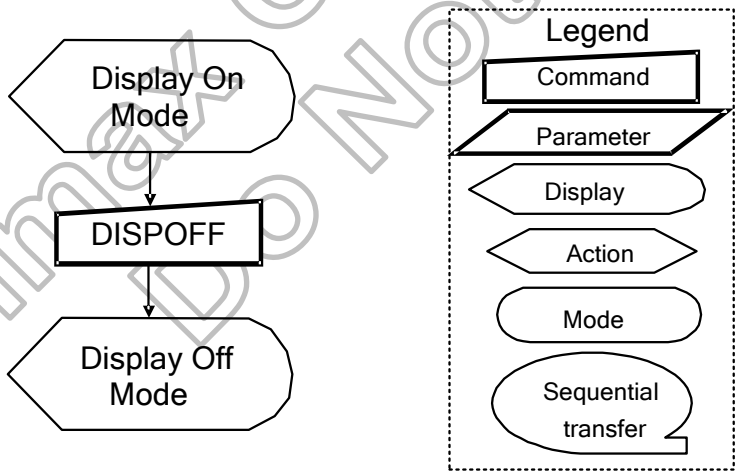
6.2.23 Set_display_off (28h)

28H	DISPOFF (Display Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example 												
Restriction	This command has no effect when module is already in display off mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

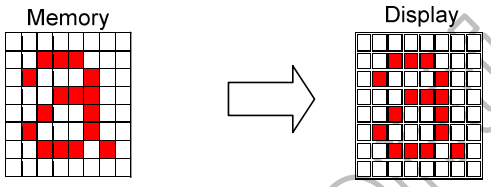
Default: N/A

Flow Chart

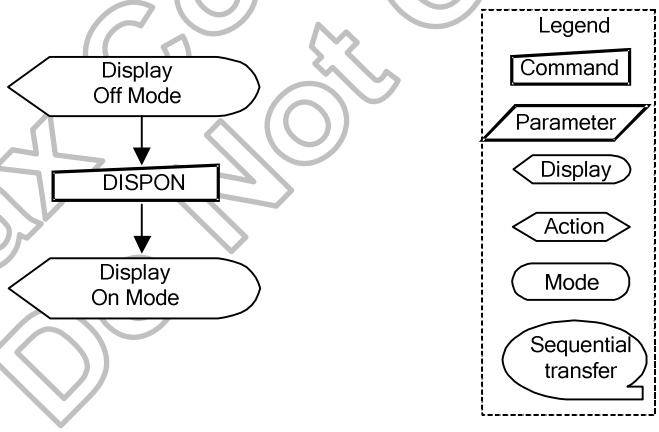


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6.2.24 Set_display_on (29h)

29H	DISPON (Display On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 												
Restriction	This command has no effect when module is already in display on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	N/A
Flow Chart	

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6.2.25 Tearing effect line off (34h)

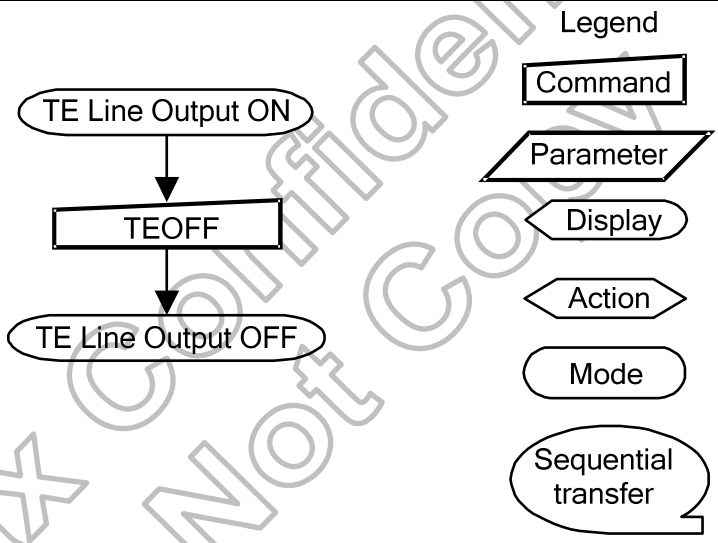
34H	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: OFF

Flow Chart



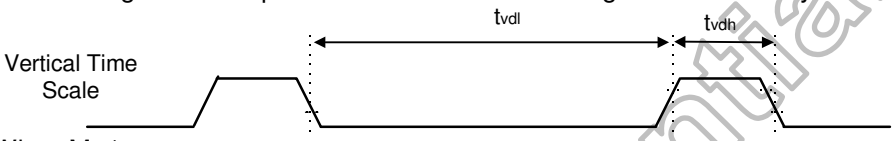
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6.2.26 Set_tear_on (35h)

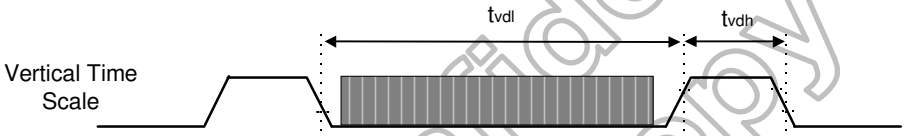
35H	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

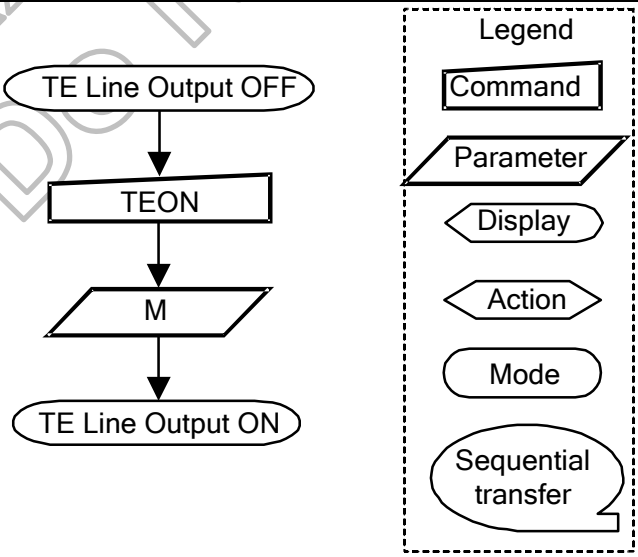
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

OFF

Flow Chart



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6.2.27 Set_address_mode (36h)

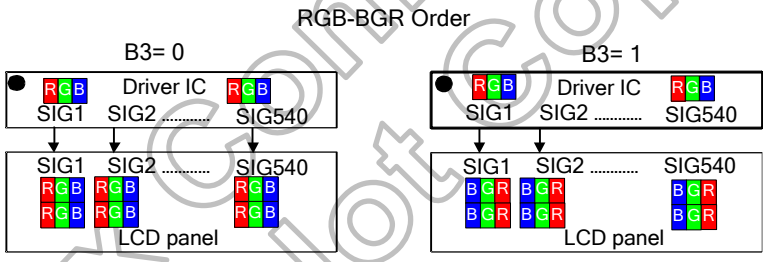
36H	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	-	B7	B6	B5	B4	B3	B2	B1	B0	XX

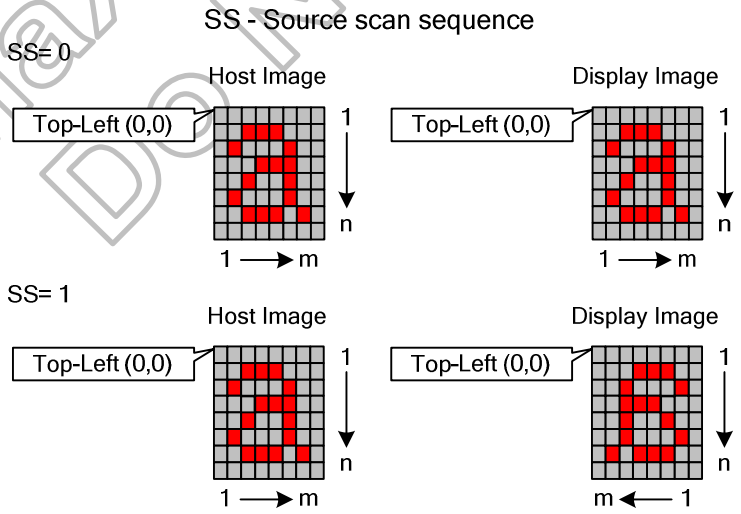
Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

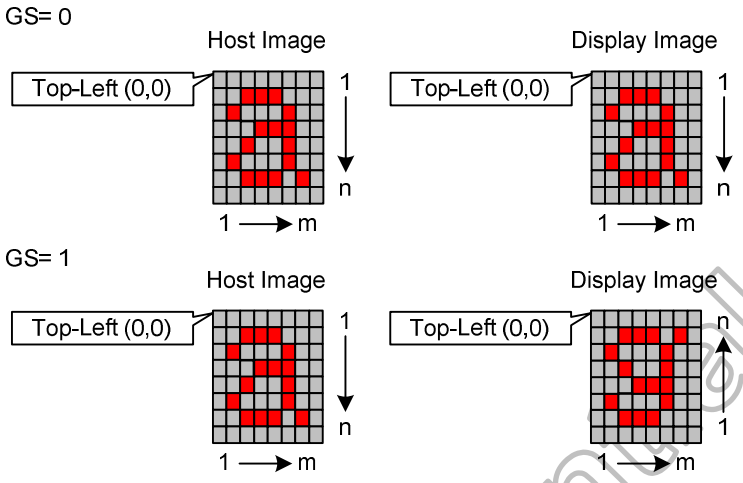
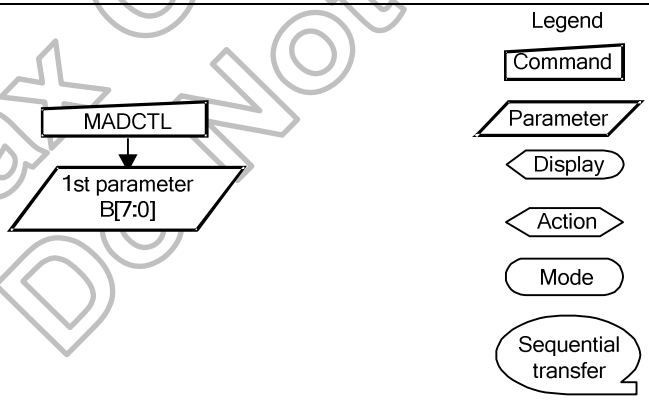
Bit Assignment

BIT	NAME	DESCRIPTION
B7	Not Defined	Set to "0".
B6	Not Defined	
B5	Not Defined	
B4	Not Defined	
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2	Not Defined	Set to "0".
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module



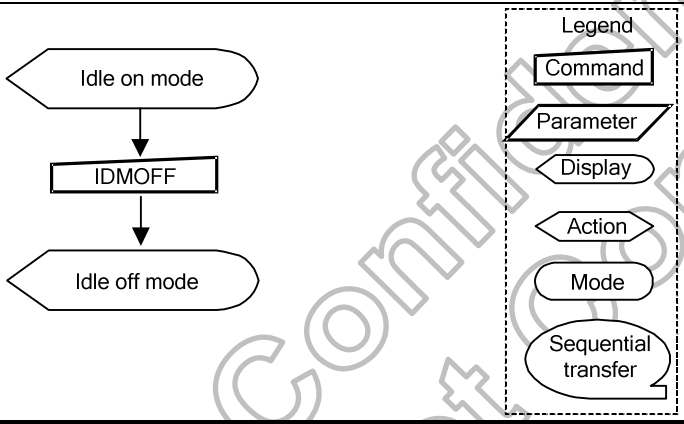


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<table>
<tr><td></td><td>GS - Gate scan sequence

</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default value</th></tr>
<tr><td>Power On Sequence</td><td>B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

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6.2.28 Idle mode off (38h)

38H	IDMOFF (Idle mode off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
Default	Idle mode is OFF.												
Flow Chart													

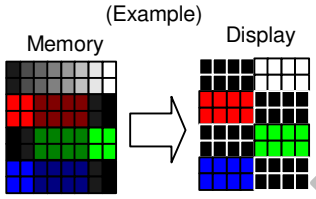
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6.2.29 Enter_Idle_mode (39h)

39H	IDMON (Idle mode on)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.



Display Colour

	R7 - R0	G7 - G0	B7 - B0
Black	0x00h	0x00h	0x00h
Blue	0x00h	0x00h	0xFFh
Red	0xFFh	0x00h	0x00h
Magenta	0xFFh	0x00h	0xFFh
Green	0x00h	0xFFh	0x00h
Cyan	0x00h	0xFFh	0xFFh
Yellow	0xFFh	0xFFh	0x00h
White	0xFFh	0xFFh	0xFFh

Restriction

This command has no effect when module is already in idle on mode.

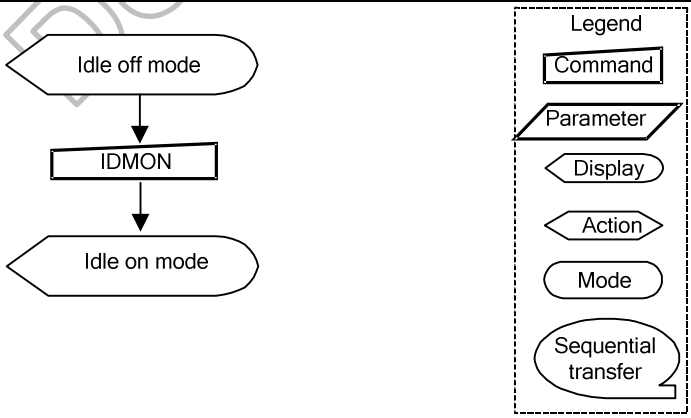
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

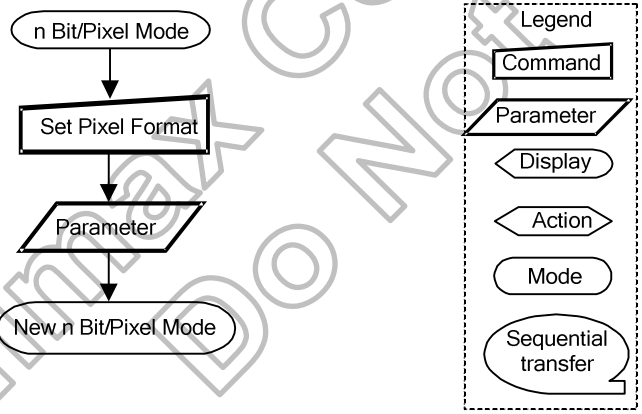
Idle mode is OFF.

Flow Chart



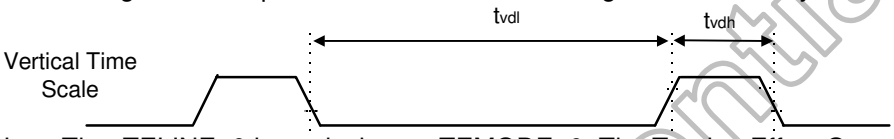
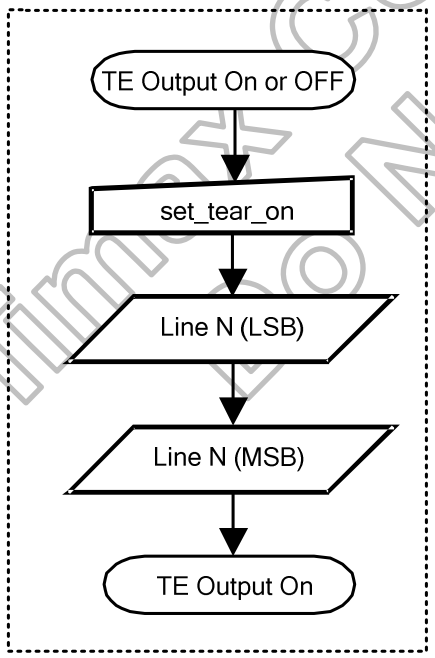
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6.2.30 Set_pixel_format (3Ah)

<table>
<tr><td rowspan="2">3A H</td><td colspan="13">COLMOD (Interface Pixel Format)</td></tr>
<tr><td>D/CX</td><td>RDX</td><td>WRX</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>X</td><td>D6</td><td>D5</td><td>D4</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define the format of RGB picture data.
D6~D4 : DPI Pixel format Definition.
The formats are shown in the table:
<table>
<tr><td>Pixel Format</td><td>D6</td><td>D5</td><td>D4</td></tr>
<tr><td>Not Defined</td><td colspan="3">Others</td></tr>
<tr><td>16 Bit/Pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 Bit/Pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 Bit/Pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
If a particular interface is not used then the corresponding bits in the parameter returned from the display module undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default value</td></tr>
<tr><td>Power On Sequence</td><td>24 Bit/Pixel</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">
</td></tr>
</table>

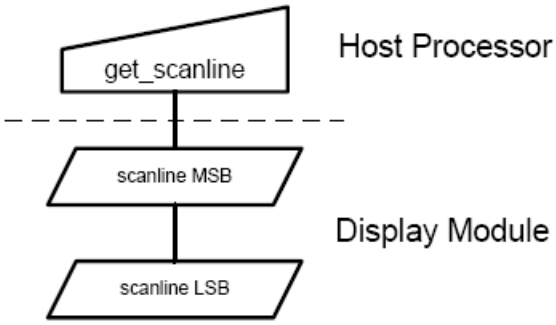
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6.2.31 Set tear scan lines (44h)

44H	TESL (Tear Effect Scan Lines)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.												
Restriction	The command has no effect when Tearing Effect output is already ON.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	TELINE[15:0]=0x0000h												
Flow Chart	 												

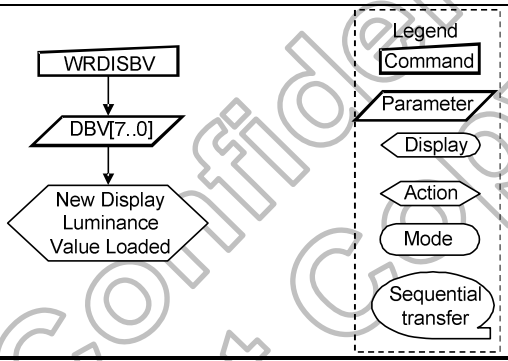
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6.2.32 Get the current scanline(45h)

45H	GETSCAN (Get the current scanline)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	1	45
1st parameter	1	1	↑	-	SLN[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	SLN[7:0](8'b0)								00..FF
Description	The display module returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes												
Default	SLN[15:0]= 0x0000h												
Flow Chart													

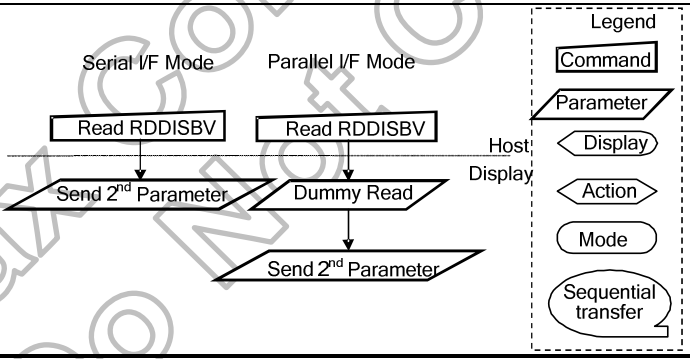
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6.2.33 Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	-	DBV[7:0]								00 .. FF
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "5.13.3 Brightness Control Block".												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

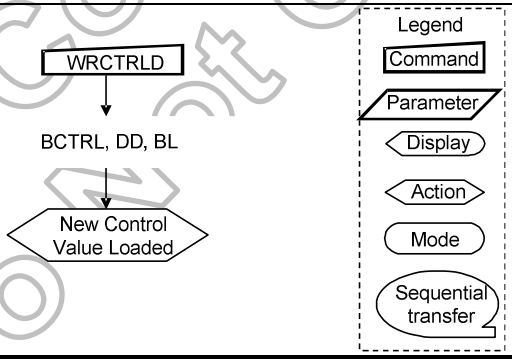
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6.2.34 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read
2nd parameter	1	↑	1	-	DBV[7:0]								xx
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: “5.13.3 Brightness Control Block”, and “6.2.33 Write Display Brightness (51h)” DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is ‘0’ when bit BCTRL of “6.2.35 Write CTRL Display (53h)” command is ‘0’. DBV[7:0] is manual set brightness specified with “6.2.35 Write CTRL Display (53h)” command when bit BCTRL is ‘1’. When bit BCTRL of “6.2.35 Write CTRL Display (53h)” command is ‘1’ and bit C1/C0 of “6.2.37 Write Content Adaptive Brightness Control (55h)” are ‘0’, DBV[7:0] output is the brightness value specified with “6.2.33 Write Display Brightness (51h)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

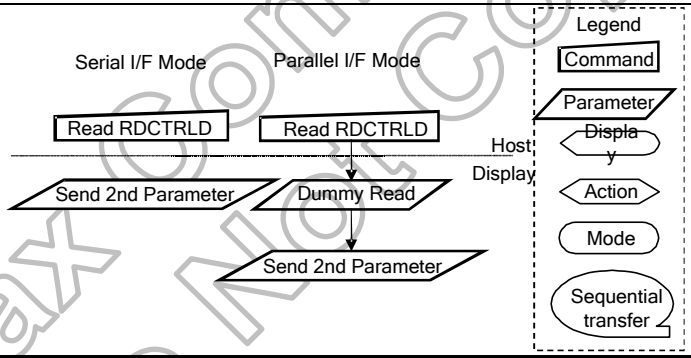
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6.2.35 Write CTRL display (53h)

53H	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00 .. FF
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

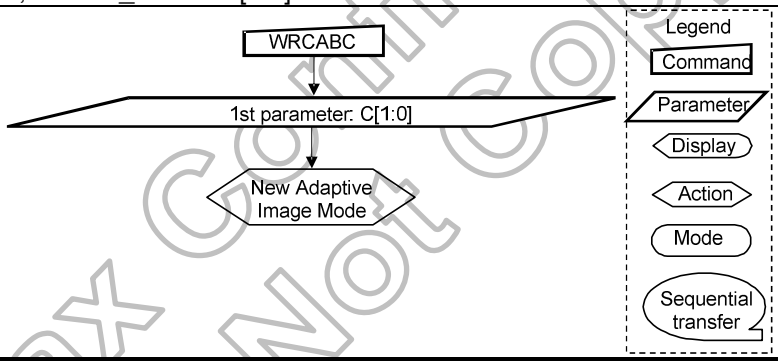
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6.2.36 Read CTRL value display (54h)

54H	RDCTRLD (Read Control Value Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	0	54
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command returns ambient light and brightness control values, see chapter: "6.2.35 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

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6.2.37 Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	-	0	0	0	0	0	0	CABC[1:0]		xx
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.13 Content Adaptive Brightness Control (CABC)". C1 / C0 / Function: 0 / 0 / Off 0 / 1 / User Interface Image 1 / 0 / Still Picture 1 / 1 / Moving Image												
Restriction													
Register Availability	Status / Availability: Sleep Out / Yes Sleep In / Yes												
Default	CABC[1:0] = 00, IMAGE_Enhance[3:0]=0000												
Flow Chart													

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6.2.38 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read
2nd parameter	1	↑	1	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.13 Content Adaptive Brightness Control (CABC)".

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

Restriction

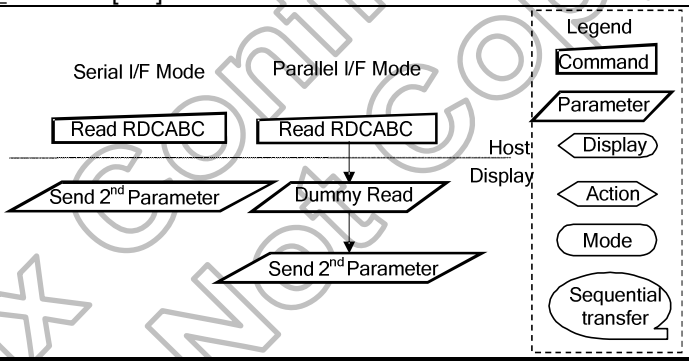
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

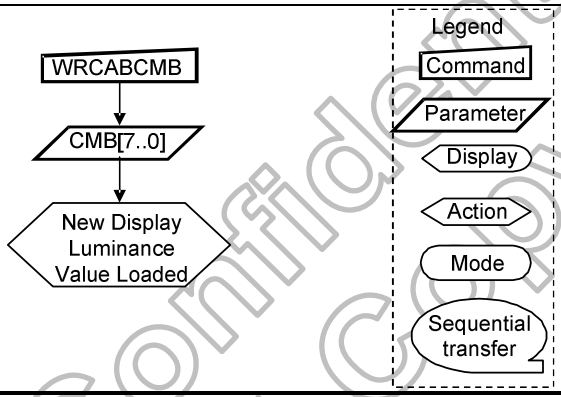
C[1:0] = 00, IMAGE_Enhance[3:0]=0000

Flow Chart



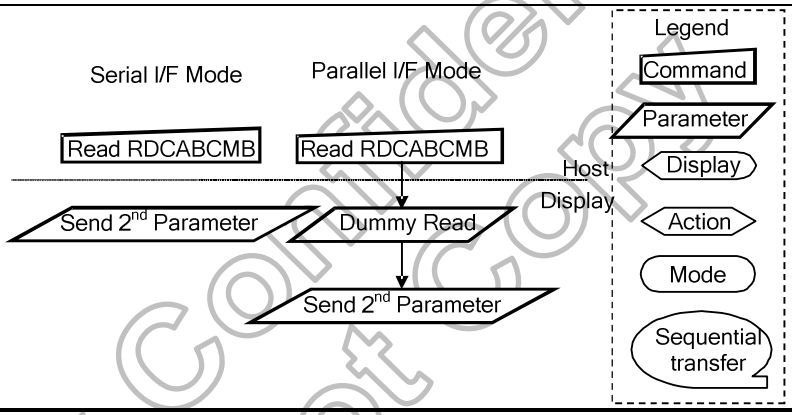
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6.2.39 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	1	-	CMB[7:0]								00 .. FF
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "5.13.4 Minimum brightness setting of CABC function".												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00												
Flow Chart													

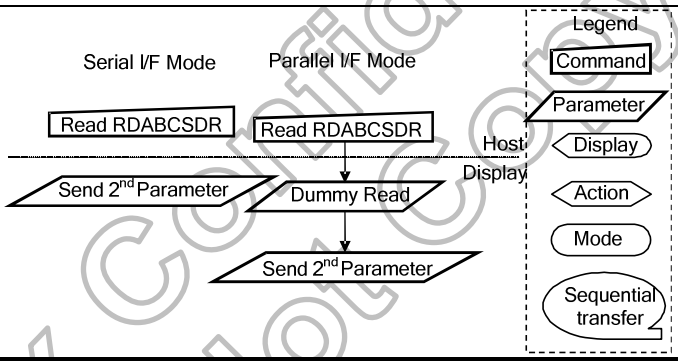
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6.2.40 Read CABC minimum brightness (5Fh)

5FH	RDCABCMB (Read CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2nd parameter	1	↑	1	-	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “5.13.4 Minimum brightness setting of CABC function”. CMB[7:0] is CABC minimum brightness specified with “6.2.39 Write CABC minimum brightness (5Eh)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00												
Flow Chart													

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6.2.41 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	D[7:6]		0	0	0	0	0	0	xx
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: ● Bit D7 – Register Loading Detection See section “5.10.1 Register loading Detection”. ● Bit D6 – Functionality Detection See section “5.10.2 Functionality Detection “. ● Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0] = 0x00												
Flow Chart													

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6.2.42 Read_DDB_start (A1h)

A1H	Read_DDB_start												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx

Description

This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.
The format of returned data is as follows:
Parameter 2: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.
Parameter 3: MS (most significant) byte of Supplier ID.
Parameter 4: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.
Parameter 5: MS (most significant) byte of Supplier Elective Data
Parameter 6: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)
- Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in *MIPI Alliance Standard for Device Descriptor Block (DDB)*.

DDBs may contain many more data fields providing information about the peripheral.
In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token.
The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.
The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB.
Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.

Restrictions

-

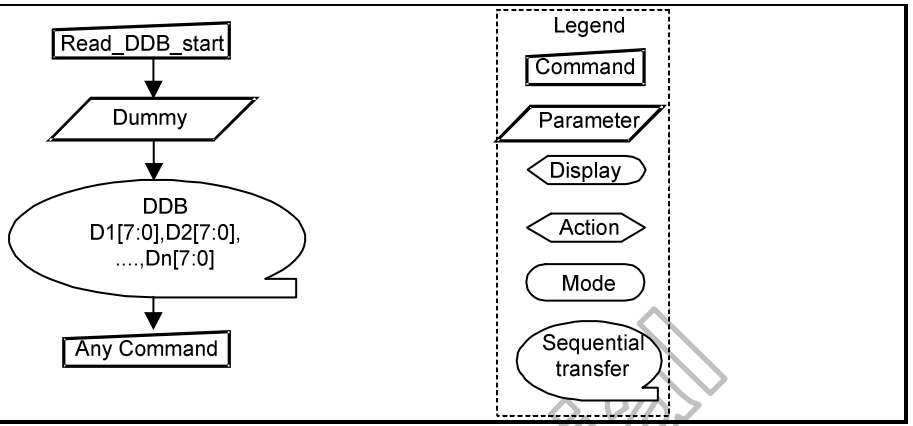
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

D[7:0] = 0x00

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Flow Chart	

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6.2.43 Read_DDB_continue (A8h)

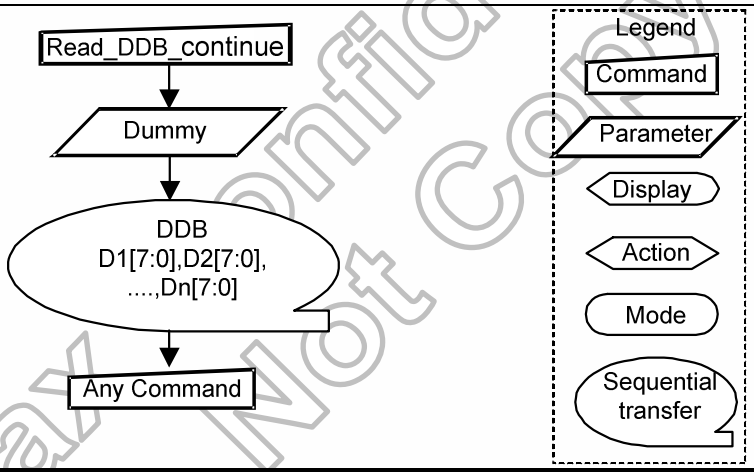
A8H	Read_DDB_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	0	0	0	A8
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.												
Restrictions	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default: D[7:0] = 0x00

Flow Chart



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6.2.44 Read first checksum (AAh)

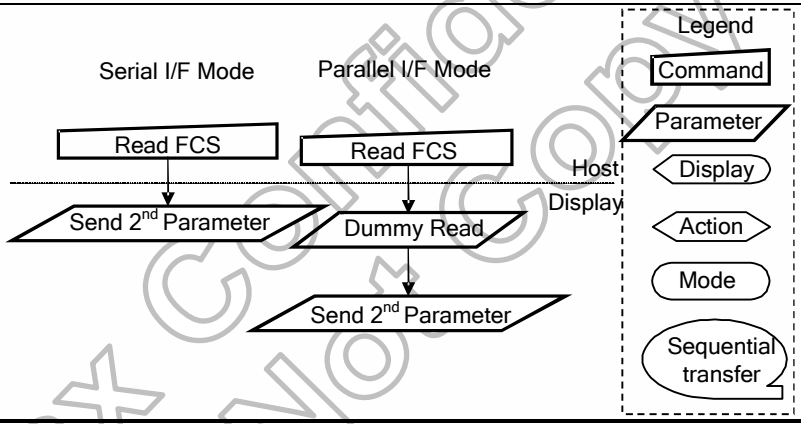
AAH	RDFCS (Read First Checksum)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	0	1	0	AA
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	-
2nd parameter	1	↑	1	FCS[7:0]								-
Description	This command returns the first checksum what has been calculated from The area registers and the frame memory after the write access to those registers and/or frame memory has been done.											
Restrictions	It will be necessary to wait 150ms after there is the last write access on command area registers before there can read this checksum value.											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: FCS[7:0] = 0x00

Flow Chart



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6.2.45 Read continue checksum (AFh)

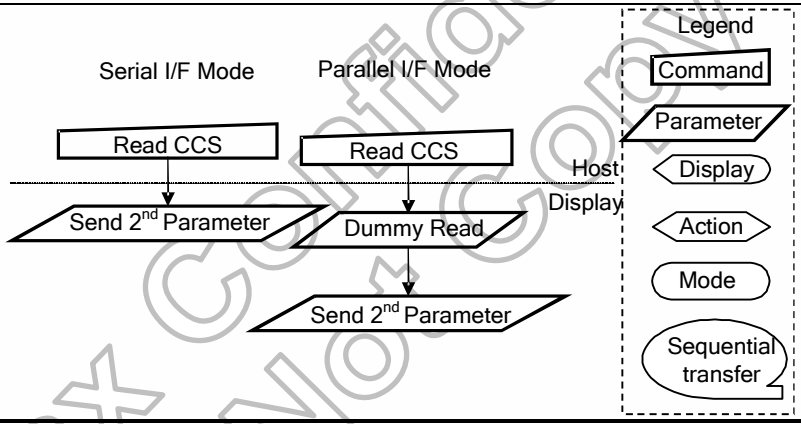
AFh	RDCCS (Read Continue Checksum)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	1	1	1	AA
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	-
2nd parameter	1	↑	1	CCS[7:0]								-
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from command area registers and the frame memory after the write access to those registers and/or frame memory has been done.											
Restrictions	It will be necessary to wait 300ms after there is the last write access on command area registers before there can read this checksum value in the first time.											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: CCS[7:0] = 0x00

Flow Chart



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6.2.46 Read ID1 (DAh)

DAH	RDID1 (Read ID1)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	-	module's manufacturer[7:0]								xx
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.												
Restriction	-												

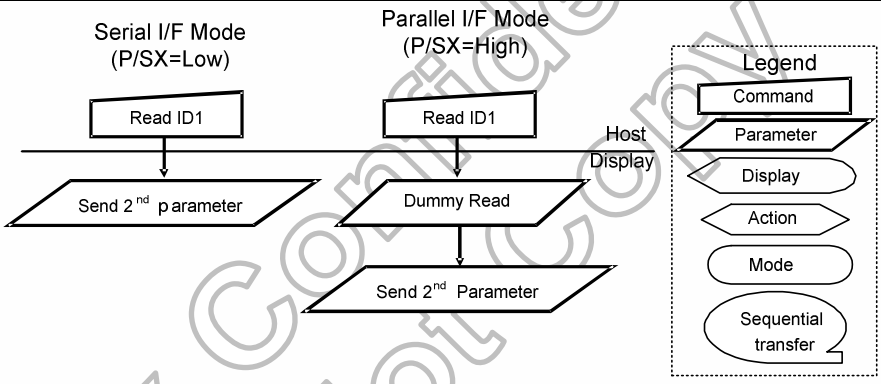
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Default value	OTP value
ID1[7:0]=0x00	Define by customer

Flow Chart



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6.2.47 Read ID2 (DBh)

DBH	RDID2 (Read ID2)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	1	1	DB
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	LCD module/driver version [7:0]								-
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:												
Restrictions	-												

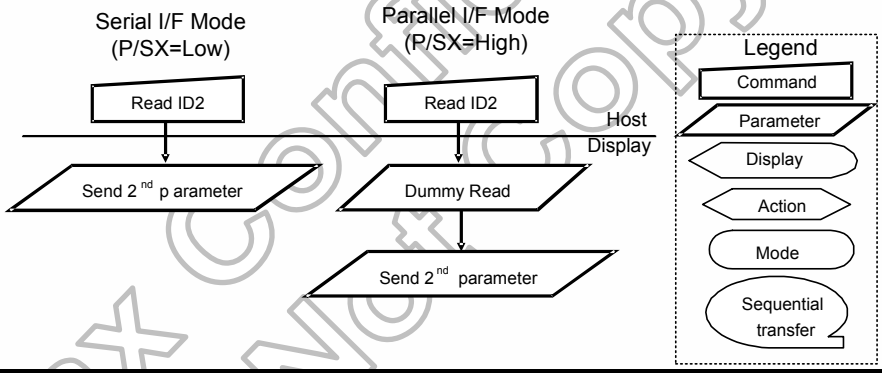
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Default value	OTP value
ID2[7:0]=0x00	Define by customer

Flow Chart



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6.2.48 Read ID3 (DCh)

DCH	RDID3 (Read ID3)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	LCD module/driver ID[7:0]								xx
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.												
Restrictions	-												

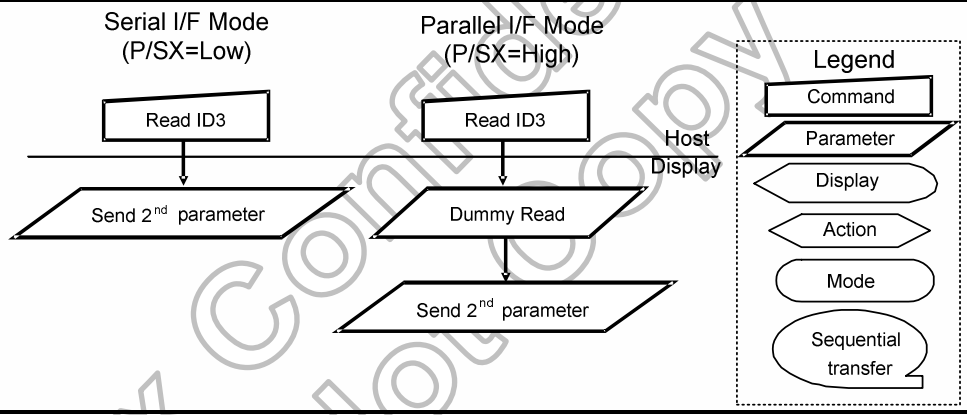
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Default value	OTP value
ID3[7:0]=0x00	Define by customer

Flow Chart



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6.3 User Define Command Description

6.3.1 SETAUTO: Set auto sequence (B0h)

<table>
<tr><th rowspan="2">B0H</th><th colspan="10">SETSAUTO(Set auto sequence)</th></tr>
<tr><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0</td></tr>
<tr><td>1st parameter</td><td>1</td><td>-</td><td colspan="7">AUTO_OPT[6:0]</td><td>00</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>OSC_EN</td><td>00</td></tr>
<tr><td>3rd parameter</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>STB</td><td>01</td></tr>
<tr><td>4th parameter</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>GON</td><td>DTE</td><td colspan="2">D[1:0]</td><td>0C</td></tr>
<tr><td>Description</td><td colspan="10">This command is used for DCS command auto sequence and manual mode debug use, please don't access this command in initial code.

AUTO_OPT[6:0]: Internal option, not open. Please set 00h.

OSC_EN: Enable internal oscillator. “1”: Enable; “0”: Disable.

STB: When STB = “1”, the HX8379-C enters the standby mode, where all display operation stops, suspend all the internal operations. But the internal R-C oscillator stop or not is determined by OSC_EN bit. To minimize the standby power, please set OSC_EN to 0. During the standby mode, only the following process can be executed.
a. Exit the Standby mode (STB = “0”)
b. Enable or disable the oscillator
c. Software reset

D[1:0]: Setting Source driver output
<table>
<tr><th>D1</th><th>D0</th><th>Source Output</th><th>HX8379-C Internal Operations</th></tr>
<tr><td>0</td><td>0</td><td>Halt</td><td>Halt</td></tr>
<tr><td>0</td><td>1</td><td>Blanking or GND</td><td>GIP initial sequence</td></tr>
<tr><td>1</td><td>0</td><td>V255 or V0</td><td>Blanking</td></tr>
<tr><td>1</td><td>1</td><td>Normal</td><td>Operate</td></tr>
</table>
DTE: Source output enable selection
<table>
<tr><th>DTE</th><th>Source Output</th></tr>
<tr><td>0</td><td>Source output off</td></tr>
<tr><td>1</td><td>Source output on</td></tr>
</table>
GON: GIP control signal enable selection
<table>
<tr><th>GON</th><th>GIP Enable</th></tr>
<tr><td>0</td><td>GIP Off</td></tr>
<tr><td>1</td><td>GIP On</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="10">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
</table>

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6.3.2 SETPOWER: Set power (B1h)

B1H	SETPOWER(Set power related setting)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	0	1	B1
1st parameter	1	DSTB	APF_EN	DD_TU	GASVCI_OPT[1:0]		AP[2:0]			64
2nd parameter	1	-	VCI_LDOS[1:0]		VRHP[4:0]					10
3rd parameter	1	-	DT[1:0]		VRHN[4:0]					10
4th parameter	1	PCCS[1:0]		EN_VSP_CLAMP	BTP[4:0]					2E
5th parameter	1	XDK[2:0]			BTN[4:0]					2E
6th parameter	1	XDKN[2:0]			EN_VSN_CLAMP	-	-	-	-	50
7th parameter	1	VCLS[2:0]			PMTU	VDDDNS[2:0]			-	F0
8th parameter	1	VGH_RATIO[1:0]	VGHS[4:0]						-	5C
9th parameter	1	VGL_RATIO[1:0]	VGLS[4:0]						-	5C
10th parameter	1	EN_NVREF	-	-	-	-	-	-	-	80
11th parameter	1	EN_VGH_REG	VGH_REGS[4:0]					-	-	B8
12th parameter	1	EN_VGL_REG	VGL_REGS[4:0]					-	-	B8
13th parameter	1	CLK_OPT5	CLK_OPT4	CLK_OPT3	CLK_OPT2	CLK_OPT1	-	-	-	F8
14th parameter	1	FS5[3:0]				FS4[3:0]				22
15th parameter	1	FS3[3:0]				FS2[3:0]				22
16th parameter	1	FS1[3:0]				FS0[3:0]				22

Description

AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.5μA
0	1	0	1.0μA
0	1	1	1.5μA
1	0	0	2.0μA
1	0	1	2.5μA
1	1	0	3.0μA
1	1	1	3.5μA

GASVCI_OPT[1:0]: Set the threshold voltage of GAS function(APF_EN =1)

GASVCI_OPT1	GASVCI_OPT0	GAS threshold voltage
0	0	1.73V
0	1	2.15V
1	0	2.36V

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DD_TU: Set DD_TU="1", VDDD will increase at Sleep In mode.

APF_EN: Abnormal power-off detection enable(GAS function). "1": Enable.

DSTB: Set '1' to enter deep standby mode for saving power in SLPIN mode. User must enter SLPIN mode before enter deep standby mode and leave deep stand by mode before SLPOUT.

VCI_LDOS[1:0]: Set the regulated voltage of VDD3 in external VSP mode.

VCI_LDOS 1	VCI_LDOS 0	VDD3 threshold voltage
0	0	VDDDX1.6
0	1	VDDDX2
1	0	VDDDX2.2
1	1	VDDDX2.5

DT[1:0]: Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

VRHP[4:0]: VSPR regulator output control setting for source data output driving.

VRHP[4:0]					VSPR Voltage
0	0	0	0	0	VPREF
0	0	0	0	1	3.1V
0	0	0	1	0	3.2V
0	0	0	1	1	3.3V
0	0	1	0	0	3.4V
0	0	1	0	1	3.5V
0	0	1	1	0	3.6V
0	0	1	1	1	3.7V
0	1	0	0	0	3.8V
0	1	0	0	1	3.9V
0	1	0	1	0	4.0V
0	1	0	1	1	4.1V
0	1	1	0	0	4.2V
0	1	1	0	1	4.3V
0	1	1	1	0	4.4V
0	1	1	1	1	4.5V
1	0	0	0	0	4.6V
1	0	0	0	1	4.7V
1	0	0	1	0	4.8V
1	0	0	1	1	4.9V
1	0	1	0	0	5.0V
1	0	1	0	1	5.1V
1	0	1	1	0	5.2V
1	0	1	1	1	5.3V
1	1	0	0	0	5.4V
1	1	0	0	1	5.5V
1	1	0	1	0	5.6V
1	1	0	1	1	5.7V
1	1	1	0	0	5.8V
1	1	1	0	1	5.9V
1	1	1	1	0	6.0V
1	1	1	1	1	6.1V

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VRHN[4:0]: VSNR regulator output control setting for source data output driving

VRHN[4:0]					VSNR Voltage
0	0	0	0	0	VNREF
0	0	0	0	1	-3.1V
0	0	0	1	0	-3.2V
0	0	0	1	1	-3.3V
0	0	1	0	0	-3.4V
0	0	1	0	1	-3.5V
0	0	1	1	0	-3.6V
0	0	1	1	1	-3.7V
0	1	0	0	0	-3.8V
0	1	0	0	1	-3.9V
0	1	0	1	0	-4.0V
0	1	0	1	1	-4.1V
0	1	1	0	0	-4.2V
0	1	1	0	1	-4.3V
0	1	1	1	0	-4.4V
0	1	1	1	1	-4.5V
1	0	0	0	0	-4.6V
1	0	0	0	1	-4.7V
1	0	0	1	0	-4.8V
1	0	0	1	1	-4.9V
1	0	1	0	0	-5.0V
1	0	1	0	1	-5.1V
1	0	1	1	0	-5.2V
1	0	1	1	1	-5.3V
1	1	0	0	0	-5.4V
1	1	0	0	1	-5.5V
1	1	0	1	0	-5.6V
1	1	0	1	1	-5.7V
1	1	1	0	0	-5.8V
1	1	1	0	1	-5.9V
1	1	1	1	0	-6.0V
1	1	1	1	1	-6.1V

PCCS[1:0]: VSP/VSN pumping method selection(valid only in EXT_VSPN=0)

PCCS1	PCCS0	Driving mode
0	0	Internal Charge Pump
0	1	Reserved
1	0	Reserved
1	1	HX5186-A/B/C

EN_VSP_CLAMP: Enable VSP clamp function. '1': Enable; '0': Disable.

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP Voltage
0	0	0	0	0	3.00V
0	0	0	0	1	3.15V
0	0	0	1	0	3.30V
0	0	0	1	1	3.45V
0	0	1	0	0	3.60V
0	0	1	0	1	3.75V
0	0	1	1	0	3.90V
0	0	1	1	1	4.05V
0	1	0	0	0	4.2V
0	1	0	0	1	4.35V

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0	1	0	1	0	4.5V
0	1	0	1	1	4.65V
0	1	1	0	0	4.8V
0	1	1	0	1	4.95V
0	1	1	1	0	5.1V
0	1	1	1	1	5.25V
1	0	0	0	0	5.40V
1	0	0	0	1	5.55V
1	0	0	1	0	5.70V
1	0	0	1	1	5.85V
1	0	1	0	0	6.00V
1	0	1	0	1	6.15V
1	0	1	1	0	6.30V
1	0	1	1	1	6.45V
1	1	0	0	0	6.60V
1	1	0	0	1	6.75V
1	1	0	1	0	6.90V
1	1	0	1	1	7.05V
1	1	1	0	0	7.20V
1	1	1	0	1	7.35V
1	1	1	1	0	7.5V
1	1	1	1	1	7.65V

BTN[4:0]: Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

BTN4	BTN3	BTN2	BTN1	BTN0	VSN Voltage
0	0	0	0	0	-3.00V
0	0	0	0	1	-3.15V
0	0	0	1	0	-3.30V
0	0	0	1	1	-3.45V
0	0	1	0	0	-3.60V
0	0	1	0	1	-3.75V
0	0	1	1	0	-3.90V
0	0	1	1	1	-4.05V
0	1	0	0	0	-4.2V
0	1	0	0	1	-4.35V
0	1	0	1	0	-4.5V
0	1	0	1	1	-4.65V
0	1	1	0	0	-4.8V
0	1	1	0	1	-4.95V
0	1	1	1	0	-5.1V
0	1	1	1	1	-5.25V
1	0	0	0	0	-5.40V
1	0	0	0	1	-5.55V
1	0	0	1	0	-5.70V
1	0	0	1	1	-5.85V
1	0	1	0	0	-6.00V
1	0	1	0	1	-6.15V
1	0	1	1	0	-6.30V
1	0	1	1	1	-6.45V
1	1	0	0	0	-6.60V
1	1	0	0	1	-6.75V
1	1	0	1	0	-6.90V
1	1	0	1	1	-7.05V
1	1	1	0	0	-7.20V
1	1	1	0	1	-7.35V
1	1	1	1	0	-7.5V
1	1	1	1	1	-7.65V

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XDK[2:0]: Setting charge pump mode of VSP voltage

XDK2	XDK1	XDK0	VSP	CAP.
0	0	0	Inhibit	-
0	0	1	X2 Pump	4
0	1	0	X2.5 Pump	4
0	1	1	Inhibit	-
1	0	0	X3 Pump	4
1	0	1	Inhibit	-
1	1	0	Inhibit	-

XDKN[2:0]: Setting charge pump mode of VSN voltage

XDKN2	XDKN1	XDKN0	VSN	CAP.
0	0	0	Inhibit	-
0	0	1	Inhibit	-
0	1	0	X2.5 Pump	4
0	1	1	Inhibit	-
1	0	0	X3 Pump	4
1	0	1	Inhibit	-
1	1	0	Inhibit	-
1	1	1	Inhibit	-

EN_VSN_CLAMP: Enable VSN clamp function. '1': Enable; '0': Disable.

PMTU: Enable PSRR of VCI regulator. '1': Enable; '0': Disable.

VDDDNS[2:0]: Specify the VDDDN voltage.

VDDDNS[2:0]	VDDDN Voltage
000	-2.5V
001	-2.6V
010	-2.7V
011	-2.8V
100	-2.9V
101	-3.0V
110	-3.1V

VCLS[2:0]: Specify the VCL voltage.

VCLS[2:0]	VCL Voltage
000	-2.5V
001	-2.6V
010	-2.7V
011	-2.8V
100	-2.9V
101	-3.0V
110	-3.1V
111	-VDD3

VGHS[4:0]: VGH output voltage setting. The LCD drive voltage level VGH can be selected according to the characteristic of liquid crystal which panel used.

VGHS 4	VGHS 3	VGHS 2	VGHS 1	VGHS 0	VGH Voltage
0	0	0	0	0	6.4V
0	0	0	0	1	6.8V
0	0	0	1	0	7.2V
0	0	0	1	1	7.6V
0	0	1	0	0	8V
0	0	1	0	1	8.4V
0	0	1	1	0	8.8V

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0	0	1	1	1	9.2V
0	1	0	0	0	9.6V
0	1	0	0	1	10V
0	1	0	1	0	10.4V
0	1	0	1	1	10.8V
0	1	1	0	0	11.2V
0	1	1	0	1	11.6V
0	1	1	1	0	12V
0	1	1	1	1	12.4V
1	0	0	0	0	12.8V
1	0	0	0	1	13.2V
1	0	0	1	0	13.6V
1	0	0	1	1	14V
1	0	1	0	0	14.4V
1	0	1	0	1	14.8V
1	0	1	1	0	15.2V
1	0	1	1	1	15.6V
1	1	0	0	0	16V
1	1	0	0	1	16.4V
1	1	0	1	0	16.8V
1	1	0	1	1	17.2V
1	1	1	0	0	17.6V
1	1	1	0	1	18V
1	1	1	1	0	18.4V
1	1	1	1	1	18.8V

VGLS[4:0]: VGL output voltage setting. The LCD drive voltage level VGL can be selected according to the characteristic of liquid crystal which panel used.

VGLS 4	VGLS 3	VGLS 2	VGLS 1	VGLS 0	VGL Voltage
0	0	0	0	0	-6.4V
0	0	0	0	1	-6.8V
0	0	0	1	0	-7.2V
0	0	0	1	1	-7.6V
0	0	1	0	0	-8V
0	0	1	0	1	-8.4V
0	0	1	1	0	-8.8V
0	0	1	1	1	-9.2V
0	1	0	0	0	-9.6V
0	1	0	0	1	-10V
0	1	0	1	0	-10.4V
0	1	0	1	1	-10.8V
0	1	1	0	0	-11.2V
0	1	1	0	1	-11.6V
0	1	1	1	0	-12V
0	1	1	1	1	-12.4V
1	0	0	0	0	-12.8V
1	0	0	0	1	-13.2V
1	0	0	1	0	-13.6V
1	0	0	1	1	-14V
1	0	1	0	0	-14.4V
1	0	1	0	1	-14.8V
1	0	1	1	0	-15.2V
1	0	1	1	1	-15.6V
1	1	0	0	0	-16V
1	1	0	0	1	-16.4V
1	1	0	1	0	-16.8V
1	1	0	1	1	-17.2V

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1	1	1	0	0	-17.6V
1	1	1	0	1	-18V
1	1	1	1	0	-18.4V
1	1	1	1	1	-18.8V

VGH_RATIO[1:0]: Specify the VGH voltage source.

VGH_RATIO[1:0]		VGH Voltage
0	0	(0-VSN)+VDD3
0	1	(0-VSN)+VSP
1	0	(VSP-VSN)+VDD3
1	1	(VSP-VSN)+VSP

VGL_RATIO[1:0]: Specify the VGL voltage source.

VGL_RATIO[1:0]		VGL Voltage
0	0	VSN-(VDD3-0)
0	1	VSN-(VSP-0)
1	0	VSN-(VDD3-VSN)
1	1	VSN-(VSP-VSN)

EN_NVREF: Enable NVREF circuit (Default : '1': Enable);

EN_VGH_REG: Enable VGH_REG regulator. '1': Enable; '0': Disable.
EN_VGL_REG: Enable VGL_REG regulator. '1': Enable; '0': Disable.

VGH_REGS[4:0]: VGH_REG output voltage setting. The LCD drive voltage level VGH_REG can be selected according to the characteristic of liquid crystal which panel used.

VGH_REGS 4	VGH_REGS 3	VGH_REGS 2	VGH_REGS 1	VGH_REGS 0	VGH_REG Voltage
0	0	0	0	0	6.4V
0	0	0	0	1	6.8V
0	0	0	1	0	7.2V
0	0	0	1	1	7.6V
0	0	1	0	0	8V
0	0	1	0	1	8.4V
0	0	1	1	0	8.8V
0	0	1	1	1	9.2V
0	1	0	0	0	9.6V
0	1	0	0	1	10V
0	1	0	1	0	10.4V
0	1	0	1	1	10.8V
0	1	1	0	0	11.2V
0	1	1	0	1	11.6V
0	1	1	1	0	12V
0	1	1	1	1	12.4V
1	0	0	0	0	12.8V
1	0	0	0	1	13.2V
1	0	0	1	0	13.6V
1	0	0	1	1	14V
1	0	1	0	0	14.4V
1	0	1	0	1	14.8V
1	0	1	1	0	15.2V
1	0	1	1	1	15.6V
1	1	0	0	0	16V
1	1	0	0	1	16.4V
1	1	0	1	0	16.8V
1	1	0	1	1	17.2V

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1	1	1	0	0	17.6V
1	1	1	0	1	18V
1	1	1	1	0	18.4V
1	1	1	1	1	18.8V

VGL_REGS[4:0]: VGL_REG output voltage setting. The LCD drive voltage level VGL_REG can be selected according to the characteristic of liquid crystal which panel used.

VGL_REGS 4	VGL_REGS 3	VGL_REGS 2	VGL_REGS 1	VGL_REGS 0	VGL_REG Voltage
0	0	0	0	0	-6.4V
0	0	0	0	1	-6.8V
0	0	0	1	0	-7.2V
0	0	0	1	1	-7.6V
0	0	1	0	0	-8V
0	0	1	0	1	-8.4V
0	0	1	1	0	-8.8V
0	0	1	1	1	-9.2V
0	1	0	0	0	-9.6V
0	1	0	0	1	-10V
0	1	0	1	0	-10.4V
0	1	0	1	1	-10.8V
0	1	1	0	0	-11.2V
0	1	1	0	1	-11.6V
0	1	1	1	0	-12V
0	1	1	1	1	-12.4V
1	0	0	0	0	-12.8V
1	0	0	0	1	-13.2V
1	0	0	1	0	-13.6V
1	0	0	1	1	-14V
1	0	1	0	0	-14.4V
1	0	1	0	1	-14.8V
1	0	1	1	0	-15.2V
1	0	1	1	1	-15.6V
1	1	0	0	0	-16V
1	1	0	0	1	-16.4V
1	1	0	1	0	-16.8V
1	1	0	1	1	-17.2V
1	1	1	0	0	-17.6V
1	1	1	0	1	-18V
1	1	1	1	0	-18.4V
1	1	1	1	1	-18.8V

CLK_OPT1: The pumping clock of VSP will reset with Hsync when CLK_OPT1 = 1.

CLK_OPT2: The pumping clock of VSN will reset with Hsync when CLK_OPT2 = 1.

CLK_OPT3: The pumping clock of VGH will reset with Hsync when CLK_OPT3 = 1.

CLK_OPT4: The pumping clock of VGL will reset with Hsync when CLK_OPT4 = 1.

CLK_OPT5: The pumping clock of VCL will reset with Hsync when CLK_OPT5 = 1.

FS0[3:0]: Set the operating frequency of the HX5186-A/B/C control signal VCSW1/VCSW2
(Fosc_pump=5MHz)

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FS03	FS02	FS01	FS00	EXT_CHG_CLK (HX5186 VCSW clk)	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/2	2	2500.0
0	0	0	1	Fosc_pump/4	4	1250.0
0	0	1	0	Fosc_pump/8	8	625.0
0	0	1	1	Fosc_pump/16	16	312.5
0	1	0	0	Fosc_pump/32	32	156.3
0	1	0	1	Fosc_pump/48	48	104.2
0	1	1	0	Fosc_pump/64	64	78.1
0	1	1	1	Fosc_pump/80	80	62.5
1	0	0	0	Fosc_pump/96	96	52.1
1	0	0	1	Fosc_pump/112	112	44.6
1	0	1	0	Fosc_pump/126	126	39.7
1	0	1	1	Fosc_pump/144	144	34.7
1	1	0	0	Fosc_pump/160	160	31.3
1	1	0	1	Fosc_pump/176	176	28.4
1	1	1	0	Fosc_pump/192	192	26.0
1	1	1	1	Fosc_pump/208	208	24.0

FS1[3:0]: Set the operating frequency of the step-up circuit for VSP voltage generation. (Fosc_pump=5MHz)

FS13	FS12	FS11	FS10	VSP_CLK	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/32	32	156.3
0	0	0	1	Fosc_pump/64	64	78.1
0	0	1	0	Fosc_pump/96	96	52.1
0	0	1	1	Fosc_pump/128	128	39.1
0	1	0	0	Fosc_pump/160	160	31.3
0	1	0	1	Fosc_pump/192	192	26.0
0	1	1	0	Fosc_pump/224	224	22.3
0	1	1	1	Fosc_pump/256	256	19.5
1	0	0	0	Hsync*4	0.25	460.7
1	0	0	1	Hsync*2	0.5	230.4
1	0	1	0	Hsync	1	115.2
1	0	1	1	Hsync/2	2	57.6
1	1	0	0	Hsync/4	4	28.8
1	1	0	1	Hsync/8	8	14.4
1	1	1	0	Hsync/16	16	7.2
1	1	1	1	Inhibited	Inhibited	Inhibited

FS2[3:0]: Set the operating frequency of the step-up circuit for VSN voltage generation. (Fosc_pump=5MHz)

FS23	FS22	FS21	FS20	VSN_CLK	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/32	32	156.3
0	0	0	1	Fosc_pump/64	64	78.1
0	0	1	0	Fosc_pump/96	96	52.1
0	0	1	1	Fosc_pump/128	128	39.1
0	1	0	0	Fosc_pump/160	160	31.3
0	1	0	1	Fosc_pump/192	192	26.0
0	1	1	0	Fosc_pump/224	224	22.3
0	1	1	1	Fosc_pump/256	256	19.5
1	0	0	0	Hsync*4	0.25	460.7
1	0	0	1	Hsync*2	0.5	230.4
1	0	1	0	Hsync	1	115.2
1	0	1	1	Hsync/2	2	57.6
1	1	0	0	Hsync/4	4	28.8
1	1	0	1	Hsync/8	8	14.4

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1	1	1	0	Hsync/16	16	7.2
1	1	1	1	Inhibited	Inhibited	Inhibited

FS3[3:0]: Set the operating frequency of the step-up circuit for VGH voltage generation. (Fosc_pump=5MHz)

FS33	FS32	FS31	FS30	VGH_CLK	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/32	32	156.3
0	0	0	1	Fosc_pump/64	64	78.1
0	0	1	0	Fosc_pump/96	96	52.1
0	0	1	1	Fosc_pump/128	128	39.1
0	1	0	0	Fosc_pump/160	160	31.3
0	1	0	1	Fosc_pump/192	192	26.0
0	1	1	0	Fosc_pump/224	224	22.3
0	1	1	1	Fosc_pump/256	256	19.5
1	0	0	0	Hsync*4	0.25	460.7
1	0	0	1	Hsync*2	0.5	230.4
1	0	1	0	Hsync	1	115.2
1	0	1	1	Hsync/2	2	57.6
1	1	0	0	Hsync/4	4	28.8
1	1	0	1	Hsync/8	8	14.4
1	1	1	0	Hsync/16	16	7.2
1	1	1	1	Inhibited	Inhibited	Inhibited

FS4[3:0]: Set the operating frequency of the step-up circuit for VGL voltage generation. (Fosc_pump=5MHz)

FS43	FS42	FS41	FS40	VGL_CLK	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/32	32	156.3
0	0	0	1	Fosc_pump/64	64	78.1
0	0	1	0	Fosc_pump/96	96	52.1
0	0	1	1	Fosc_pump/128	128	39.1
0	1	0	0	Fosc_pump/160	160	31.3
0	1	0	1	Fosc_pump/192	192	26.0
0	1	1	0	Fosc_pump/224	224	22.3
0	1	1	1	Fosc_pump/256	256	19.5
1	0	0	0	Hsync*4	0.25	460.7
1	0	0	1	Hsync*2	0.5	230.4
1	0	1	0	Hsync	1	115.2
1	0	1	1	Hsync/2	2	57.6
1	1	0	0	Hsync/4	4	28.8
1	1	0	1	Hsync/8	8	14.4
1	1	1	0	Hsync/16	16	7.2
1	1	1	1	Inhibited	Inhibited	Inhibited

FS5[3:0]: Adjust the charge pump frequency of internal VCL. (Fosc_pump=5MHz)

FS53	FS52	FS51	FS50	VCL_CLK	5MHz/ Div	Freq (kHz)
0	0	0	0	Fosc_pump/32	32	156.3
0	0	0	1	Fosc_pump/64	64	78.1
0	0	1	0	Fosc_pump/96	96	52.1
0	0	1	1	Fosc_pump/128	128	39.1
0	1	0	0	Fosc_pump/160	160	31.3
0	1	0	1	Fosc_pump/192	192	26.0
0	1	1	0	Fosc_pump/224	224	22.3
0	1	1	1	Fosc_pump/256	256	19.5
1	0	0	0	Hsync*4	0.25	460.7
1	0	0	1	Hsync*2	0.5	230.4

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	1	0	1	0	Hsync	1	115.2
	1	0	1	1	Hsync/2	2	57.6
	1	1	0	0	Hsync/4	4	28.8
	1	1	0	1	Hsync/8	8	14.4
	1	1	1	0	Hsync/16	16	7.2
	1	1	1	1	Inhibited	Inhibited	Inhibited

Restrictions	SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.3 SETDISP: Set display related register (B2h)

B2H	SETDISP(Set display related register)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	1	0	B2
1st parameter	1	ZZ_LR	ZZ_EO	-	-	-	NW[2:0]			80
2nd parameter	1	NL[7:0]								44
3rd parameter	1	BP[7:0]								08
4th parameter	1	FP[7:0]								03
5th parameter	1	SAP[3:0]				vs_plus _bp_en	-	-	ABC_H S_BYP ASS	30
6th parameter	1	RTN[7:0]								50

Description

This command is used to set display related register

ZZ_LR: Zig-zag Left / Right mode selection.

ZZ_LR	Zig-zag Left / Right mode selection
0	S1~SR1
1	SL1~S1440

ZZ_EO: Zig-zag Odd / Even mode selection.

ZZ_EO	Zig-zag Odd / Even mode selection
0	Odd-line shift
1	Even-line shift

NW[2:0]: Inversion type setting.

NW2	NW1	NW0	Inversion type
0	0	0	Column inversion
0	0	1	1-dot inversion
0	1	0	2-dot inversion
0	1	1	4-dot inversion
1	0	0	8-dot inversion
1	0	1	Zig-zag inversion
1	1	0	2+2 inversion
1	1	1	3-dot inversion

NL[7:0]: Setting the number of lines to drive the LCD at an interval of 4 lines. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[7:0]								Line
0	0	0	0	0	0	0	0	320
0	0	0	0	0	0	0	1	328
0	0	0	0	0	0	1	0	336
0	0	0	0	0	0	1	1	344
. . .								. . .
0	1	0	0	0	1	0	0	864
. . .								. . .
0	1	0	1	0	1	1	0	1008
0	1	0	1	0	1	1	1	1016
0	1	0	1	1	0	0	0	1024
Others								Inhibited
1	1	1	1	1	1	1	0	854

BP[7:0] : Specify the amount of scan line for back porch(BP).
FP[7:0]: Specify the amount of scan line for front porch (FP).

FP[7:0] / BP[7:0]	Number of FP	Number of BP

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8h'00	2 lines
8h'01	3 lines
8h'02	4 lines
8h'03	5 lines
8h'04	6 lines
8h'05	7 lines
• • •	• • •
8h'FB	253 lines
8h'FC	254 lines
8h'FD	255 lines
8h'FE	256 lines
8h'FF	257 lines

Note: Set BP[7:0] = VS + VBP – 2, and FP[7:0] = VFP – 2.

SAP[3:0]: Set Current of Operational Amplifier

SAP3	SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	0	1 * Iref
0	0	0	1	2 * Iref
0	0	1	0	3 * Iref
0	0	1	1	4 * Iref
0	1	0	0	5 * Iref
0	1	0	1	6 * Iref
0	1	1	0	7 * Iref
0	1	1	1	8 * Iref
• • • • • • • • • • • • • • • •				
1	1	1	1	16 * Iref

VS_PLUS_BP_EN: When DSI blanking mode, internal osc will be clock.
0: No clock during DSI blanking period.
1: Using internal osc as clock during blanking period.

ABC_HS_BYPASS: Internal use, not open.

RTN[7:0]: A cycle time of the line width for internal TCON.

RTN[7:0]	Clock per Line	Line time(us)
8h'00	80 clocks	10
8h'01	81 clocks	10.125
8h'02	82 clocks	10.25
8h'03	83 clocks	10.375
• • •	• • •	• • •
8h'50	160 clocks	20
• • •	• • •	• • •
8'hFD	333 clocks	41.625
8'hFE	334 clocks	41.75
8'hFF	335 clocks	41.875

Note : Clock = External clk(32 MHz)/4 = 8 MHz

Restrictions	SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.4 SETRGBIF: Set RGB interface related register (B3h)

B3H	SETRGBIF(Set RGB interface related register)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	1	1	B3
1st parameter	1	-	-	DPICC[1:0]		DPL	HSPL	VSPL	EPL	01

Description

This command is used to set DPI interface related register.

EPL: Specify the polarity of DE pin in DPI interface mode.

EPL	ENABLE pin	Display
0	0	Enable
0	1	Disable
1	0	Disable
1	1	Enable

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DCLK pin. When DPL=0, the data is read on the rising edge of DCLK signal. When DPL=1, the data is read on the falling edge of DCLK signal.

DPICC: DPI Color mapping Configuration

Register 3Ah	DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	DPICC
50h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	2'b00
	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	2'b01
	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x	2'b10
60h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	2'b00
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	2'b01
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	2'b00

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.5 SETCYC: Set display cycle timing (B4h)

B4H	SETCYC(Set display cycle timing)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	0	0	B4
1st parameter	1	SPON[7:0]								08
2nd parameter	1	SPOFF[7:0]								30
3rd parameter	1	CON[7:0]								08
4th parameter	1	COFF[7:0]								28
5th parameter	1	CON1[7:0]								05
6th parameter	1	COFF1[7:0]								36
7th parameter	1	EQON1[7:0]								04
8th parameter	1	EQON2[7:0]								58
9th parameter	1	SON[7:0]								08
10th parameter	1	SOFF[7:0]								58

Description

This command is used to set display waveform cycles.

SPON[7:0]: Fine tune the Start and End signal delay from original starting point.
(1 OSC CLK = 1/8MHz)

SPON[7:0]	Start / END signal output start delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
:	
0xFEh	254 OSC CLK
0xFFh	255 OSC CLK

SPOFF[7:0]: Fine tune the Start and End signal ending point.

SPOFF[7:0]	Start / END signal output end delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
:	
0xFEh	254 x OSC CLK
0xFFh	255 x OSC CLK

Note: When output Start / End signal width is 1- Hsync only, set SPON[7:0] < SPOFF[7:0]

CON[7:0]/CON1[7:0]: Fine tune the Clock signal delay from original starting point.

CON[7:0]/CON1[7:0]	Clock signal output start delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
:	
0xFEh	254 OSC CLK
0xFFh	255 OSC CLK

COFF[7:0]/COFF1[7:0]: Fine tune the Clock signal ending point.

COFF[7:0]/COFF1[7:0]	Clock signal output end delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
:	
0xFEh	254 OSC CLK

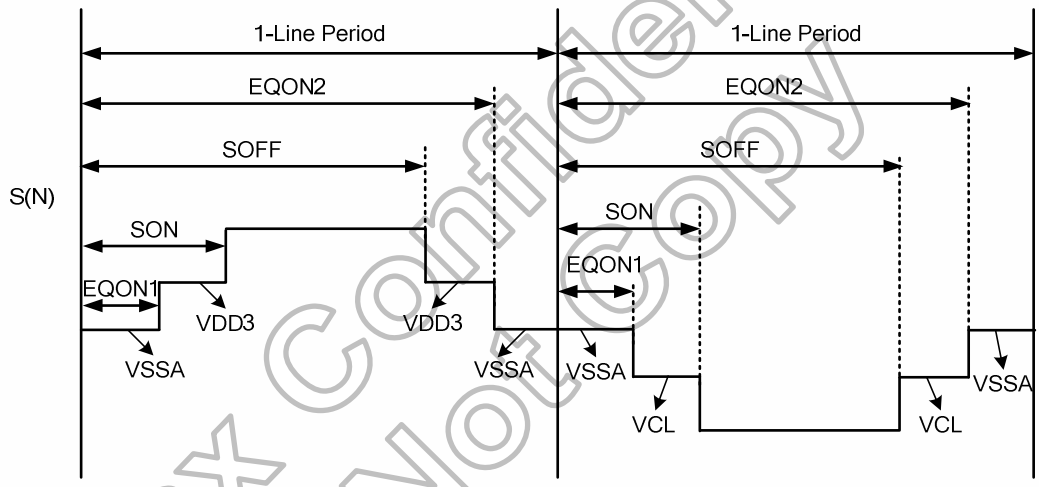
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0xFFh	255 OSC CLK

Note: When output Clock signal width is 1- Hsync only, set COFF[7:0] ≧ CON[7:0] + 2

EQON1/EQON2[7:0]: Specify the source EQ period.
(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

EQON1/EQON2[7:0]								Source EQ Period
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.	.	.	.	.	.	.	.	. . . . .
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle



SON[7:0]: Specify the valid source output start time.
(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

SON[7:0]								Source output start time
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.	.	.	.	.	.	.	.	. . . . .
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle

SOFF[7:0]: Specify the valid source output end time.
(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

SOFF[7:0]								Source output end time
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.	.	.	.	.	.	.	.	. . . . .
1	1	1	1	1	1	0	0	1008 OSC clock cycle

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	1	1	1	1	1	1	0	1	1012 OSC clock cycle
	1	1	1	1	1	1	1	0	1016 OSC clock cycle
	1	1	1	1	1	1	1	1	1020 OSC clock cycle

Restrictions: -

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.6 SETVCOM: Set VCOM voltage (B6h)

B6 H	SETVCOM (Set VCOM Voltage)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	B6
1st parameter	1	VCMC_F[7:0]								46
2nd parameter	1	VCMC_B[7:0]								46
3rd parameter	1	VCOM_TIMES[2:0]			-	-	-	VCMC_B8	VCMC_F8	00

Description

This command is used to set VCOM Voltage.
VCMC_F[8:0]: Forward scan VCOM voltage control.

VCMC_B[8:0]: Backward scan VCOM voltage control.

VCMC_F[8:0]/VCMC_B[8:0]									VCOM
0	0	0	0	0	0	0	0	0	-0.3V
0	0	0	0	0	0	0	0	1	-0.31V
0	0	0	0	0	0	0	1	0	-0.32V
0	0	0	0	0	0	0	1	1	-0.33V
:									:
1	0	1	1	1	0	0	0	1	-3.99V
1	0	1	1	1	0	0	1	0	-4V
101110011~111111101									inhibited
111111110									VSSA
111111111									HZ

VCOM_TIMES[2:0]: Read the VCOM OTP programmed times.

VCOM_TIMES[2:0]	VCOM OTP Programmed Times
111	No programmed
011	VCOM has been programmed 1 time
001	VCOM has been programmed 2 times
000	VCOM has been programmed 3 times

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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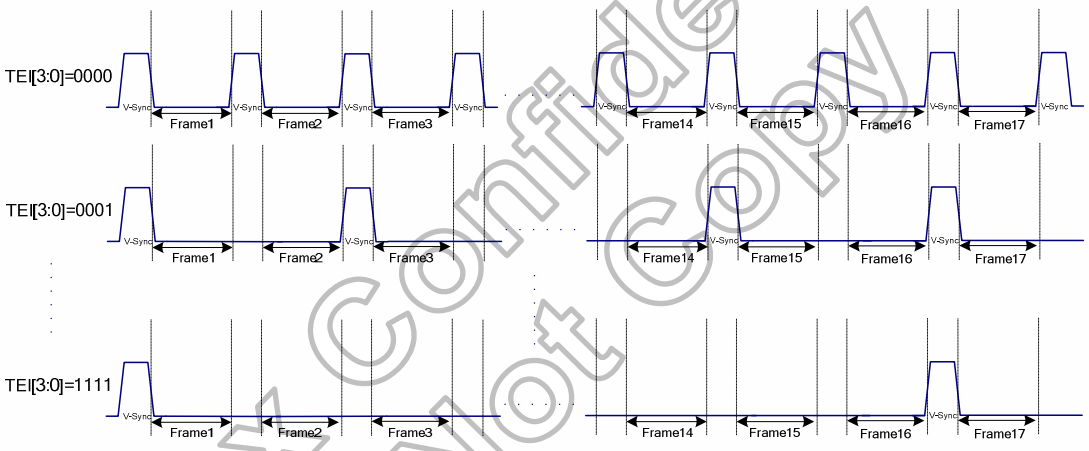
6.3.7 SETTE: Set internal TE function (B7h)

B7H	SETTE (Set internal TE function)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	1	B7
1st parameter	1	-	-	TE_SEL[1:0]		TEI[3:0]				00
2nd parameter	1	TEL_SEL[1:0]		-	-	-	TEP[10:8]			00
3rd parameter	1	TEP[7:0]								00

Description

TEI[3:0]: Set the output interval of TE signal according to the display data rewrite cycle and data transfer rate.

TEI3	TEI2	TEI1	TEI0	Output Interval
0	0	0	0	1 frame
0	0	0	1	2 frames
0	0	1	0	3 frames
. . . . .				. .
1	1	1	0	15 frames
1	1	1	1	16 frames



TEP[10:0]: Set the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation.
Make sure the setting restriction 11'h000 ≤ TEP[10:0] ≤ Numbers of Line-1.

TEP[10:0]	Output position
000h	0th line
001h	1st line
002h	2nd line
003h	3rd line
. . .	. . .
3FEh	1022nd line
3FFh	1023rd line
400h	1024th line

TE_SEL / TER_SEL[1:0]: Set the TE/TEL pins output signal type.

TEL_SEL1/ TE_SEL1	TEL_SEL0/ TE_SEL0	TE / TEL
0	0	Normal DCS case, combine with CMD R35h Set_tear_on
0	1	TE_VSYNC only
1	0	TE_HSYNC only
1	1	Source driving period (for touch sensor controller use)

Restrictions	SETEXTC turn on to enable this command.

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Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

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6.3.8 SETGPO: Set GPO output function (B8h)

<table>
<tr><th rowspan="2">B8H</th><th colspan="10">SETGPO (Set GPO output function)</th></tr>
<tr><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>B8</td></tr>
<tr><td>1st parameter</td><td>1</td><td colspan="4">GPO1SEL[3:0]</td><td colspan="4">GPO0SEL[3:0]</td><td>00</td></tr>
<tr><td>2nd parameter</td><td>1</td><td colspan="4">GPO3SEL[3:0]</td><td colspan="4">GPO2SEL[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set GPOn pin output.
<table>
<tr><th>GPOnSEL[3:0]</th><th>Output signal</th></tr>
<tr><td>0000</td><td>No output</td></tr>
<tr><td>0001</td><td>Source driving period
(for touch sensor controller use)</td></tr>
<tr><td>Others</td><td>Inhibited.</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="10">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
</table>

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6.3.9 SETEXTC: Set extented command set (B9h)

<table>
<tr><th rowspan="2">B9H</th><th colspan="10">SETEXTC (Set extended command set)</th></tr>
<tr><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>B9</td></tr>
<tr><td>1st parameter</td><td>1</td><td colspan="8">EXTC1[7:0]</td><td>FF</td></tr>
<tr><td>2nd parameter</td><td>1</td><td colspan="8">EXTC2[7:0]</td><td>83</td></tr>
<tr><td>3rd parameter</td><td>1</td><td colspan="8">EXTC3[7:0]</td><td>79</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to set extended command set access enable.
<table>
<tr><th>Extend CMD</th><th>Command description</th></tr>
<tr><td>Enable</td><td>After command (B9h), must write 3 parameters (FFh, 83h, 79h) by order</td></tr>
<tr><td>Disable(default)</td><td>After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh, 83h, 79h)</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="11">-</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
</table>

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6.3.10 SETOTP: Set OTP (BBh)

BBH	SETOTP(Set OTP)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	1	1	BB
1st parameter	1	OTP_KEY0[7:0]								
2nd parameter	1	OTP_KEY1[7:0]								00
3rd parameter	1	OTP_MASK[7:0]								00
4th parameter	1	OTP_INDEX[7:0]								00
5th parameter	1	OTP_DATA[7:0]								00
6th parameter	1	OTP_POR	OTP_PWE	OTP_PWR_SEL	INTVPP_EN	OTP_PTM[1:0]		OTP_TEST	OTP_PROG	00

FDescription

This command is used to set OTP Related Setting.

OTP_KEY0[7:0], OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	If HX8379-C operate on OTP program mode, Then keep on OTP program mode. If HX8379-C operate on non-OTP program mode, Then keep on non-OTP program mode.

OTP_MASK[7:0]: Bit programming mask, "1" means this bit can't be programmed.

OTP_INDEX[7:0]: Set index of OTP table for programming.

OTP_DATA[7:0]: Read back the OTP index data.

OTP_PROG: When set to 1, the register content of OTP index is programmed.

OTP_TEST: "0", setting OTP_PROG high will trig internal state machine.
"1", setting OTP_PROG high will not trig internal state machine.

OTP_PTM[1:0]: For test mode enabling.

INTVPP_EN: OTP_PWR power selected.
"0" : External OTP_PWR is selected when programmed.
"1" : Internal OTP_PWR (VGH short to OTP_PWR) is selected when programmed.

OTP_PWR_SEL: When written to 1, OTP_PWR voltage is fed to OTP circuit.

OTP_PWE: OTP program write enable, if 1, means OTP is able to be programmed.

OTP_POR: Pulse for OTP data read operation.

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.11 SET_BANK: Set register bank partition index(BDh)

BDH	SET_BANK(Set register bank partition index)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	1	BD
1st parameter	1	-	-	-	-	-	-	BANK_INDEX [1:0]		00

Description

Set the register bank for some Commands that beyond 64 parameters

This command is active only for RC1h.
For example:
Write RC1h, PA44~PA85
Step1: write RBDh = 01h
Step2: write RC1h, PA44~85

Read RC1h, PA86~PA127
Step1: write RBDh = 02h
Step2: read RC1h, PA86~127

BANK INDEX[1:0]	RC1h (SETDGCLUT)
00(Bank 0)	PA1~43
01(Bank 1)	PA44~85
10(Bank 2)	PA86~127
11(Bank 3)	NA

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.12 SETDGCLUT: Set DGC LUT (C1h)

C1H	SETDGCLUT (Set DGC LUT)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	1	C1
Bank 0 1st parameter	1	-	-	-	-	-	-	-	DGC_EN	00
2nd parameter	1	0	0	0	0	R_GAMMA0[5:2]				-
3rd parameter	1	0	0	0	0	R_GAMMA1[5:2]				-
4th parameter	1	0	0	0	R_GAMMA2[6:2]					-
5th parameter	1	0	0	R_GAMMA3[7:2]						-
6th parameter	1	0	0	R_GAMMA4[7:2]						-
7th parameter	1	0	R_GAMMA5[8:2]							-
8th parameter	1	0	R_GAMMA6[8:2]							-
9th parameter	1	0	R_GAMMA7[8:2]							-
10th parameter	1	0	R_GAMMA8[8:2]							-
11th parameter	1	0	R_GAMMA9[8:2]							-
12th parameter	1	0	R_GAMMA10[8:2]							-
13th parameter	1	0	R_GAMMA11[8:2]							-
14th parameter	1	0	R_GAMMA12[8:2]							-
15th parameter	1	0	R_GAMMA13[8:2]							-
16th parameter	1	R_GAMMA14[9:2]								-
17th parameter	1	R_GAMMA15[9:2]								-
18th parameter	1	R_GAMMA16[9:2]								-
19th parameter	1	R_GAMMA17[9:2]								-
20th parameter	1	R_GAMMA18[9:2]								-
21th parameter	1	R_GAMMA19[9:2]								-
22th parameter	1	R_GAMMA20[9:2]								-
23th parameter	1	R_GAMMA21[9:2]								-
24th parameter	1	R_GAMMA22[9:2]								-
25th parameter	1	1	R_GAMMA23[8:2]							-
26th parameter	1	1	R_GAMMA24[8:2]							-
27th parameter	1	1	R_GAMMA25[8:2]							-
28th parameter	1	1	R_GAMMA26[8:2]							-
29th parameter	1	1	R_GAMMA27[8:2]							-
30th parameter	1	1	R_GAMMA28[8:2]							-
31th parameter	1	1	R_GAMMA29[8:2]							-
32th parameter	1	1	R_GAMMA30[8:2]							-
33th parameter	1	1	R_GAMMA31[8:2]							-
34th parameter	1	1	R_GAMMA32[8:2]							-
35th parameter	1	R_GAMMA0[1:0]		R_GAMMA1[1:0]		R_GAMMA2[1:0]		R_GAMMA3[1:0]		-
36th parameter	1	R_GAMMA4[1:0]		R_GAMMA5[1:0]		R_GAMMA6[1:0]		R_GAMMA7[1:0]		-
37th parameter	1	R_GAMMA8[1:0]		R_GAMMA9[1:0]		R_GAMMA10[1:0]		R_GAMMA11[1:0]		-
38th parameter	1	R_GAMMA12[1:0]		R_GAMMA13[1:0]		R_GAMMA14[1:0]		R_GAMMA15[1:0]		-
39th parameter	1	R_GAMMA16[1:0]		R_GAMMA17[1:0]		R_GAMMA18[1:0]		R_GAMMA19[1:0]		-
40th parameter	1	R_GAMMA20[1:0]		R_GAMMA21[1:0]		R_GAMMA22[1:0]		R_GAMMA23[1:0]		-
41th parameter	1	R_GAMMA24[1:0]		R_GAMMA25[1:0]		R_GAMMA26[1:0]		R_GAMMA27[1:0]		-
42th parameter	1	R_GAMMA28[1:0]		R_GAMMA29[1:0]		R_GAMMA30[1:0]		R_GAMMA31[1:0]		-
43th parameter	1	R_GAMMA32[1:0]		-	-	-	-	-	-	-
Bank 1 1st parameter	1	0	0	0	0	G_GAMMA0[5:2]				-
2nd parameter	1	0	0	0	0	G_GAMMA1[5:2]				-
3rd parameter	1	0	0	0	G_GAMMA2[6:2]					-
4th parameter	1	0	0	G_GAMMA3[7:2]						-
5th parameter	1	0	0	G_GAMMA4[7:2]						-
6th parameter	1	0	G_GAMMA5[8:2]							-
7th parameter	1	0	G_GAMMA6[8:2]							-
8th parameter	1	0	G_GAMMA7[8:2]							-

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9th parameter	1	0	G_GAMMA8[8:2]						-
10th parameter	1	0	G_GAMMA9[8:2]						-
11th parameter	1	0	G_GAMMA10[8:2]						-
12th parameter	1	0	G_GAMMA11[8:2]						-
13th parameter	1	0	G_GAMMA12[8:2]						-
14th parameter	1	0	G_GAMMA13[8:2]						-
15th parameter	1	G_GAMMA14[9:2]							-
16th parameter	1	G_GAMMA15[9:2]							-
17th parameter	1	G_GAMMA16[9:2]							-
18th parameter	1	G_GAMMA17[9:2]							-
19th parameter	1	G_GAMMA186[9:2]							-
20th parameter	1	G_GAMMA10[9:2]							-
21th parameter	1	G_GAMMA20[9:2]							-
22th parameter	1	G_GAMMA21[9:2]							-
23th parameter	1	G_GAMMA22[9:2]							-
24th parameter	1	1	G_GAMMA23[8:2]						-
25th parameter	1	1	G_GAMMA24[8:2]						-
26th parameter	1	1	G_GAMMA25[8:2]						-
27th parameter	1	1	G_GAMMA26[8:2]						-
28th parameter	1	1	G_GAMMA27[8:2]						-
29th parameter	1	1	G_GAMMA28[8:2]						-
30th parameter	1	1	G_GAMMA29[8:2]						-
31th parameter	1	1	G_GAMMA30[8:2]						-
32th parameter	1	1	G_GAMMA31[8:2]						-
33th parameter	1	1	G_GAMMA32[8:2]						-
34th parameter	1	G_GAMMA0[1:0]		G_GAMMA1[1:0]		G_GAMMA2[1:0]		G_GAMMA3[1:0]	-
35th parameter	1	G_GAMMA4[1:0]		G_GAMMA5[1:0]		G_GAMMA6[1:0]		G_GAMMA7[1:0]	-
36th parameter	1	G_GAMMA8[1:0]		G_GAMMA9[1:0]		G_GAMMA10[1:0]		G_GAMMA11[1:0]	-
37th parameter	1	G_GAMMA12[1:0]		G_GAMMA13[1:0]		G_GAMMA14[1:0]		G_GAMMA15[1:0]	-
38th parameter	1	G_GAMMA16[1:0]		G_GAMMA17[1:0]		G_GAMMA18[1:0]		G_GAMMA19[1:0]	-
39th parameter	1	G_GAMMA20[1:0]		G_GAMMA21[1:0]		G_GAMMA22[1:0]		G_GAMMA23[1:0]	-
40th parameter	1	G_GAMMA24[1:0]		G_GAMMA25[1:0]		G_GAMMA26[1:0]		G_GAMMA27[1:0]	-
41th parameter	1	G_GAMMA28[1:0]		G_GAMMA29[1:0]		G_GAMMA30[1:0]		G_GAMMA31[1:0]	-
42th parameter	1	G_GAMMA32[1:0]		-	-	-	-	-	-
Bank 2 1st parameter	1	0	0	0	0	B_GAMMA0[5:2]			-
2nd parameter	1	0	0	0	0	B_GAMMA1[5:2]			-
3rd parameter	1	0	0	0	B_GAMMA2[6:2]				-
4th parameter	1	0	0	B_GAMMA3[7:2]					-
5th parameter	1	0	0	B_GAMMA4[7:2]					-
6th parameter	1	0	B_GAMMA5[8:2]						-
7th parameter	1	0	B_GAMMA6[8:2]						-
8th parameter	1	0	B_GAMMA7[8:2]						-
9th parameter	1	0	B_GAMMA8[8:2]						-
10th parameter	1	0	B_GAMMA9[8:2]						-
11th parameter	1	0	B_GAMMA10[8:2]						-
12th parameter	1	0	B_GAMMA11[8:2]						-
13th parameter	1	0	B_GAMMA12[8:2]						-
14th parameter	1	0	B_GAMMA13[8:2]						-
15th parameter	1	B_GAMMA14[9:2]							-
16th parameter	1	B_GAMMA15[9:2]							-
17th parameter	1	B_GAMMA16[9:2]							-
18th parameter	1	B_GAMMA17[9:2]							-
19th parameter	1	B_GAMMA18[9:2]							-
20th parameter	1	B_GAMMA19[9:2]							-
21th parameter	1	B_GAMMA20[9:2]							-

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22th parameter	1	B_GAMMA21[9:2]								-
23th parameter	1	B_GAMMA22[9:2]								-
24th parameter	1	1	B_GAMMA23[8:2]							-
25th parameter	1	1	B_GAMMA24[8:2]							-
26th parameter	1	1	B_GAMMA25[8:2]							-
27th parameter	1	1	B_GAMMA26[8:2]							-
28th parameter	1	1	B_GAMMA27[8:2]							-
29th parameter	1	1	B_GAMMA28[8:2]							-
30th parameter	1	1	B_GAMMA29[8:2]							-
31th parameter	1	1	B_GAMMA30[8:2]							-
32th parameter	1	1	B_GAMMA31[8:2]							-
33th parameter	1	1	B_GAMMA32[8:2]							-
34th parameter	1	B_GAMMA0[1:0]		B_GAMMA1[1:0]		B_GAMMA2[1:0]		B_GAMMA3[1:0]		-
35th parameter	1	B_GAMMA4[1:0]		B_GAMMA5[1:0]		B_GAMMA6[1:0]		B_GAMMA7[1:0]		-
36th parameter	1	B_GAMMA8[1:0]		B_GAMMA9[1:0]		B_GAMMA10[1:0]		B_GAMMA11[1:0]		-
37th parameter	1	B_GAMMA12[1:0]		B_GAMMA13[1:0]		B_GAMMA14[1:0]		B_GAMMA15[1:0]		-
38th parameter	1	B_GAMMA16[1:0]		B_GAMMA17[1:0]		B_GAMMA18[1:0]		B_GAMMA19[1:0]		-
39th parameter	1	B_GAMMA20[1:0]		B_GAMMA21[1:0]		B_GAMMA22[1:0]		B_GAMMA23[1:0]		-
40th parameter	1	B_GAMMA24[1:0]		B_GAMMA25[1:0]		B_GAMMA26[1:0]		B_GAMMA27[1:0]		-
41th parameter	1	B_GAMMA28[1:0]		B_GAMMA29[1:0]		B_GAMMA30[1:0]		B_GAMMA31[1:0]		-
42th parameter	1	B_GAMMA32[1:0]		-	-	-	-	-	-	-

Description

This command is used to set Digital Gamma Curve Look-Up Table.

R/G/B Digital Gamma Curve Look-Up Table are divided in three banks.
Select Bank in command BDh before setting DGC LUT C1h.

Set_Bank (BDh)	DGC_EN / DGC LUT
00h	DGC_EN : 1st PA and R color DGC LUT : 2nd PA~ 43th PA
01h	G color DGC LUT : 1st PA~ 42th PA
02h	B color DGC LUT : 1st PA~ 42th PA

DGC_EN: Enable the DGC function

LUT Default Value (Hex)	R/G/B DGC LUT
00h	GAMMA0[9:0]
08h	GAMMA1[9:0]
10h	GAMMA2[9:0]
18h	GAMMA3[9:0]
20h	GAMMA4[9:0]
28h	GAMMA5[9:0]
30h	GAMMA6[9:0]
38h	GAMMA7[9:0]
40h	GAMMA8[9:0]
48h	GAMMA9[9:0]
50h	GAMMA10[9:0]
58h	GAMMA11[9:0]
60h	GAMMA12[9:0]
68h	GAMMA13[9:0]
70h	GAMMA14[9:0]
78h	GAMMA15[9:0]

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80h	GAMMA16[9:0]	
88h	GAMMA17[9:0]	
90h	GAMMA18[9:0]	
98h	GAMMA19[9:0]	
A0h	GAMMA20[9:0]	
A8h	GAMMA21[9:0]	
B0h	GAMMA22[9:0]	
B8h	GAMMA23[9:0]	
C0h	GAMMA24[9:0]	
C8h	GAMMA25[9:0]	
D0h	GAMMA26[9:0]	
D8h	GAMMA27[9:0]	
E0h	GAMMA28[9:0]	
E8h	GAMMA29[9:0]	
F0h	GAMMA30[9:0]	
F8h	GAMMA31[9:0]	
FFh	GAMMA32[9:0]	

Restrictions: SETEXTC turn on to enable this command.

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

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6.3.13 SETID: Set ID (C3h)

C3H	SETID (Set ID)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	1	1	C3
1st parameter	1	ID1[7:0]								83
2nd parameter	1	ID2[7:0]								79
3rd parameter	1	ID3[7:0]								0C
4th parameter	1	ID4[7:0]								00
5th parameter	1	ID_TIMES[2:0]			-	-	-	-	-	E0

Description

ID1[7:0] is used to set ID RDAh value.

ID2[7:0] is used to set ID RDBh value.

ID3[7:0] is used to set ID RDCh value.

ID4[7:0] is used to set the fourth ID.

ID_TIMES[2:0]: Read the ID OTP programmed times.

ID_TIMES[2:0]	ID OTP Programmed Times
111	No programmed
011	ID has been programmed 1 time
001	ID has been programmed 2 times
000	ID has been programmed 3 times

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.14 SETDDB: Set DDB (C4h)

C4H	SETDDB (Set DDB)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	0	0	C4
1st parameter	1	DDB1[7:0]								00
2nd parameter	1	DDB2[7:0]								00
3rd parameter	1	DDB3[7:0]								00
4th parameter	1	DDB4[7:0]								00
Description	This command is used to set CMD RA1h DDB1~4 value.									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

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6.3.15 SETCABC: Set CABC control (C9h)

C9H	SETCABC (Set CABC Control)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	0	1	C9
1st Parameter	1	PWM_PERIOD[16]	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY	1F
2nd Parameter	1	PWM_PERIOD[15:8]								2E
3rd Parameter	1	PWM_PERIOD[7:0]								1E
4th Parameter	1	CABC_FSYNC	DIM_FRAME[6:0]							1E
5th Parameter	1	CABC_DD	-	-	BC_CTRL_EN	CABC_FLM[3:0]				00

Description

This command is used to set CABC parameter.

SEL_BLDUTY: Backlight pwm output duty on/off control when CABC operation.
'0', The Backlight pwm output duty is 100%.
'1', The Backlight pwm output duty is calculated from CABC operation.

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

SEL_GAIN[1:0]: CABC gain select.

SEL_GAIN[1:0]	Gain
00	Use 1.00 as CABC calculate gain
01	Use 0.5x CABC calculate gain
10	Use 0.75x as CABC calculate gain
11	Use CABC calculate gain

SEL_PWMCLK[2:0] : Internal PWM_CLK divider for CABC clock.

SEL_PWMCLK[2:0]			Brightness Control Clock frequency
0	0	0	PWM_CLK / 1
0	0	1	PWM_CLK / 2
0	1	0	PWM_CLK / 4
0	1	1	PWM_CLK / 6
1	0	0	PWM_CLK / 8
1	0	1	PWM_CLK / 10
1	1	0	PWM_CLK / 12
1	1	1	PWM_CLK / 14

PWM_PERIOD[16:0]: The backlight PWM output period setting.

When PWM_PERIOD[16]=0, PWM_PERIOD[15:6] setting inhibited.

PWM_PERIOD [5:0]						CABC_PWM_OUT signal frequency
0	0	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/500
0	0	0	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/513
0	0	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/527
0	0	0	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/541
0	0	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/556
0	0	0	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/572
0	0	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/589
0	0	0	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/607
0	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/625
0	0	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/646
0	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/667

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0	0	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/690
0	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/715
0	0	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/741
0	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/770
0	0	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/800
0	1	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/834
0	1	0	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/870
0	1	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/910
0	1	0	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/953
0	1	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1000
0	1	0	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1053
0	1	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1112
0	1	0	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1177
0	1	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1250
0	1	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1334
0	1	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1429
0	1	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1539
0	1	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1667
0	1	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1819
0	1	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2000
0	1	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2223
1	0	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2500
1	0	0	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2858
1	0	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/3334
1	0	0	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/4000
1	0	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/5000
1	0	0	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/6667
1	0	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/10000
1	0	0	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/20000
1	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/22223
1	0	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/25000
1	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/28572
1	0	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/33334
1	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/40000
1	0	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/50000
1	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/66667
1	0	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/100000
1	1	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/200000
Others						Inhibited

When PWM_PERIOD[16]=1:
CABC_PWM_OUT frequency=
[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/(PWM_PERIOD[15:0]+1)
Note: PWM_PERIOD[15:0]=0000h is inhibited.

DIM_FRAME[6:0] : Number of dimming frames used in manual brightness dimming.

CABC_FSYNC: Reset CABC_PWM_OUT signal by each VSYNC.

CABC_DD: CABC dimming function enable bit.
(Main dimming function enable/disable ,
It also controls data gain and backlight dimming function from on to off and off to on .)
'0', Disable CABC dimming.
'1', Enable CABC dimming.

BC_CTRL_EN: Enable Backlight & PMIC.

CABC_STEP[7:0]: CABC step numbers during dimming period.

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<table>
<tr><td></td><td>CABC_FLM[3:0]: CABC dimming frame number for each step.</td></tr>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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6.3.16 SETCABCGAIN: Set CABC Gain value (CAh)

CAH	SETCABCGAIN (Set CABC Gain value)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	0	CA
1st Parameter	1	-	DBG0[6:0]							-
2nd parameter	1	-	DBG1[6:0]							-
3rd parameter	1	-	DBG2[6:0]							-
4th parameter	1	-	DBG3[6:0]							-
5th parameter	1	-	DBG4[6:0]							-
6th parameter	1	-	DBG5[6:0]							-
7th parameter	1	-	DBG6[6:0]							-
8th parameter	1	-	DBG7[6:0]							-
9th parameter	1	-	DBG8[6:0]							-

Description

DBG0~8[6:0] : Gain select register 0~8.

DBG0~8[6:0]							CABC Gain	CABC Duty
0	0	x	x	x	x	x	Reserve	
0	1	0	0	0	0	0	1+0/32	100%
0	1	0	0	0	0	1	1+1/32	96.97%
0	1	0	0	0	1	0	1+2/32	94.12%
0	1	0	0	0	1	1	1+3/32	91.43%
0	1	0	0	1	0	0	1+4/32	88.89%
0	1	0	0	1	0	1	1+5/32	86.49%
0	1	0	0	1	1	0	1+6/32	84.21%
0	1	0	0	1	1	1	1+7/32	82.05%
0	1	0	1	0	0	0	1+8/32	80%
0	1	0	1	0	0	1	1+9/32	78.05%
0	1	0	1	0	1	0	1+10/32	76.19%
0	1	0	1	0	1	1	1+11/32	74.42%
0	1	0	1	1	0	0	1+12/32	72.73%
0	1	0	1	1	0	1	1+13/32	71.11%
0	1	0	1	1	1	0	1+14/32	69.57%
0	1	0	1	1	1	1	1+15/32	68.09%
0	1	1	0	0	0	0	1+16/32	66.67%
0	1	1	0	0	0	1	1+17/32	65.31%
0	1	1	0	0	1	0	1+18/32	64%
0	1	1	0	0	1	1	1+19/32	62.75%
0	1	1	0	1	0	0	1+20/32	61.54%
0	1	1	0	1	0	1	1+21/32	60.38%
0	1	1	0	1	1	0	1+22/32	59.26%
0	1	1	0	1	1	1	1+23/32	58.18%
0	1	1	1	0	0	0	1+24/32	57.14%
0	1	1	1	0	0	1	1+25/32	56.14%
0	1	1	1	0	1	0	1+26/32	55.17%
0	1	1	1	0	1	1	1+27/32	54.24%
0	1	1	1	1	0	0	1+28/32	53.33%
0	1	1	1	1	0	1	1+29/32	52.46%
0	1	1	1	1	1	0	1+30/32	51.61%
0	1	1	1	1	1	1	1+31/32	50.79%
1	0	0	0	0	0	0	1+32/32	50%

For details, please refer to chapter “5.13.2 CABC Block”.

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

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6.3.17 SETPANEL: Set panel related register (CCh)

CCH	SETPANEL(Set panel related register)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	1	0	0	CC
1st parameter	1	-	-	-	-	SS_ PANEL	GS_ PANEL	REV_ PANEL	BGR_ PANEL	00

Description0

This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user

BGR_PANEL: The order of <R><G><B> dot color for module supplier, default value is stored in OTP. If color filter of panel is <B><G><R> type, setting BGR_PANEL = 1, if color filter of panel is <R><G><B> type, setting BGR_PANEL = 0. This bit is to make panel module look like a <R><G><B> type panel form the user viewpoint.

REV_PANEL: The REV_PANEL setting is combined with HW_Pin NBWSEL to select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally-white and normally-black panels.

	NBWSEL=1	NBWSEL=0
REV_PANEL = 0	Normally-white panel	Normally-black panel
REV_PANEL = 1	Normally-black panel	Normally-white panel

GS_PANEL: Specify the shift direction of gate driver output.
When GS_PANEL = 0, the panel control signal is normal scan.
When GS_PANEL = 1, the panel control signal is reverse scan.

SS_PANEL: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S1440. When SS_PANEL = 1, the shift direction from S1440 to S1.

Restrictions: SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.18 SETCLOCK : Adjust OSC frequency (CBh)

CBH	SETCLOCK (Adjust OSC frequency)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	1	CB
1st Parameter	1	-	-	-	-	UADJ[3:0]				07

Description

UADJ[3:0]: For user to adjust OSC frequency, default is 32 MHz.

UADJ[3:0]				Internal oscillator frequency
0	0	0	0	61.49%
0	0	0	1	67.29%
0	0	1	0	72.69%
0	0	1	1	78.26%
0	1	0	0	83.20%
0	1	0	1	89.14%
0	1	1	0	94.51%
0	1	1	1	100.00%
1	0	0	0	103.95%
1	0	0	1	109.72%
1	0	1	0	114.55%
1	0	1	1	120.56%
1	1	0	0	124.70%
1	1	0	1	130.56%
1	1	1	0	135.40%
1	1	1	1	140.93%

Restrictions: SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.19 SETGIP_0: Set GIP timing (D3h)

D3H	SETGIP_0(Set GIP Option 0)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	0	1	1	D3
1st parameter	1	-	-	-	-	-	-	VGLO_SEL	LVGL_SEL	-
2nd parameter	1	EQ_DELAY[7:0]								-
3rd parameter	1	-	-	GIP_EQ_MODE [1:0]		-	-	OVER LAP_ OPT	-	-
4th parameter	1	GTO[7:0]								-
5th parameter	1	GNO[7:0]								-
6th parameter	1	USER_GIP_GATE[7:0]								-
7th parameter	1	USER_GIP_GATE1[7:0]								-
8th parameter	1	SHR0_3[3:0]				SHR0_2[3:0]				-
9th parameter	1	SHR0_1[3:0]				SHR0[11:8]				-
10th parameter	1	SHR0[7:0]								-
11st parameter	1	-	-	-	-	SHR0_GS[11:8]				-
12nd parameter	1	SHR0_GS[7:0]								-
13rd parameter	1	-	-	-	-	SHR1[11:8]				-
14th parameter	1	SHR1[7:0]								-
15th parameter	1	-	-	-	-	SHR1_GS[11:8]				-
16th parameter	1	SHR1_GS[7:0]								-
17th parameter	1	-	-	-	-	SHR2[11:8]				-
18th parameter	1	SHR2[7:0]								-
19th parameter	1	-	-	-	-	SHR2_GS[11:8]				-
20th parameter	1	SHR2_GS[7:0]								-
21st parameter	1	SHP0[3:0]				SCP[3:0]				-
22nd parameter	1	SHP2[3:0]				SHP1[3:0]				-
23rd parameter	1	CHR0[7:0]								-
24th parameter	1	CHR0_GS[7:0]								-
25th parameter	1	CHP0[3:0]				CCP0[3:0]				-
26th parameter	1	CHR1[7:0]								-
27th parameter	1	CHR1_GS[7:0]								-
28th parameter	1	CHP1[3:0]				CCP1[3:0]				-

Description

This command is used for GIP signal setting.

VGLO_SEL: VGLO voltage selection.

VGLO_SEL	VGLO Voltage Selection
0	VGL
1	VGL_REG

LVGL_SEL: LVGL voltage selection.

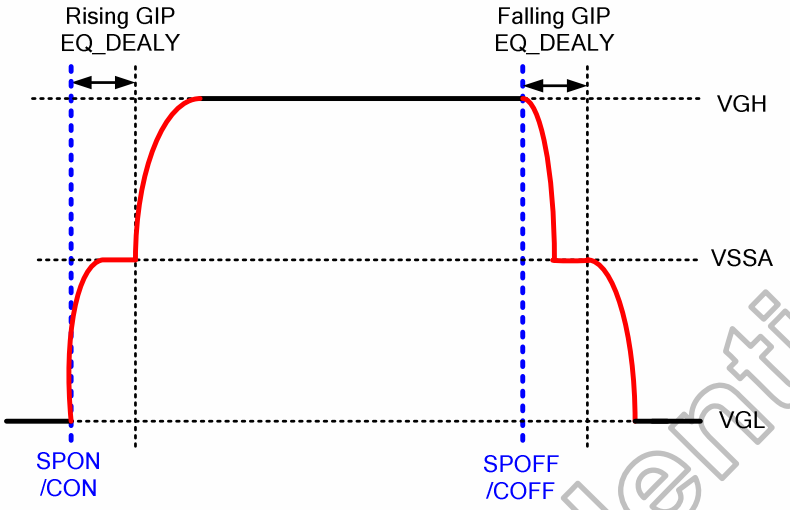
LVGL_SEL	LVGL Voltage Selection
0	VGL
1	VGL_REG

EQ_DELAY[7:0]: Set GIP control signal EQ period

EQ_DELAY [7:0]								GIP EQ Period
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	8 OSC clock cycle
0	0	0	0	0	0	1	0	16 OSC clock cycle
0	0	0	0	0	0	1	1	24 OSC clock cycle
0	0	0	0	0	1	0	0	32 OSC clock cycle
. . . . .								. . . . .
1	1	1	1	1	1	0	0	2016 OSC clock cycle
1	1	1	1	1	1	0	1	2024 OSC clock cycle

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1	1	1	1	1	1	1	0	2032 OSC clock cycle
1	1	1	1	1	1	1	1	2040 OSC clock cycle



GIP_EQ_MODE[1:0]: GIP EQ (pre-charge) type selection

GIP_EQ_MODE[1]	GIP_EQ_MODE[0]	GIP EQ Type
0	0	Both rising / falling EQ
0	1	Only rising edge EQ
1	0	Only falling edge EQ
1	1	EQ Off

OVERLAP_OPT: Choose GPWR over lap type.
When set '1', GPWR low period longer then high period.
When set '0', GPWR high period longer then low period.

GTO[7:0] : Define toggle period of output GPWR clock signal setting

GTO[7:0]	GPWR toggle frequency
8'h00	64 x Frame/Line
8'h01	1 x Frame/ Line
8'h02	2 x Frame/ Line
8'h03	3 x Frame/ Line
. . . . .	. . . . .
8'hFD	253 x Frame/ Line
8'hFE	254 x Frame/ Line
8'hFF	255 x Frame/ Line

GNO[7:0]: Define output GPWR clock signal non-overlap timing

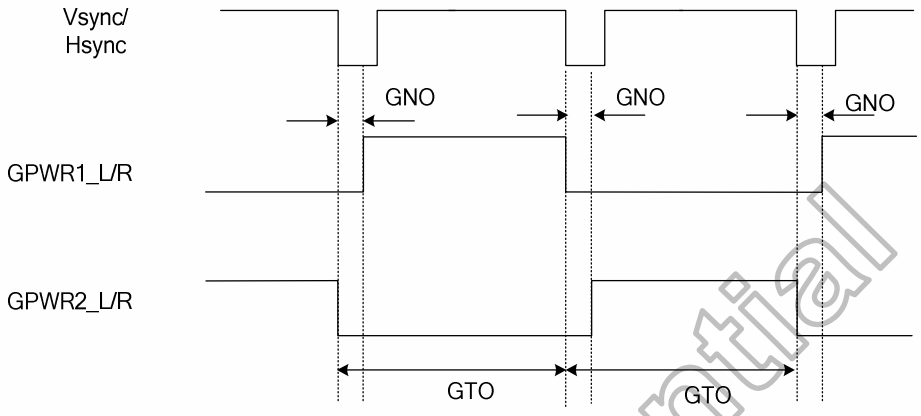
GNO[7:0]	GPWR non-overlap timing
8'h00	0
8'h01	1 x OSC CLK
8'h02	2 x OSC CLK
8'h03	3 x OSC CLK
. . . . .	. . . . .
8'hFD	253 x OSC CLK
8'hFE	254 x OSC CLK
8'hFF	255 x OSC CLK

GPWR1/2 toggle period unit defined by frame or line depend on GIP_OPT[4] bit setting.

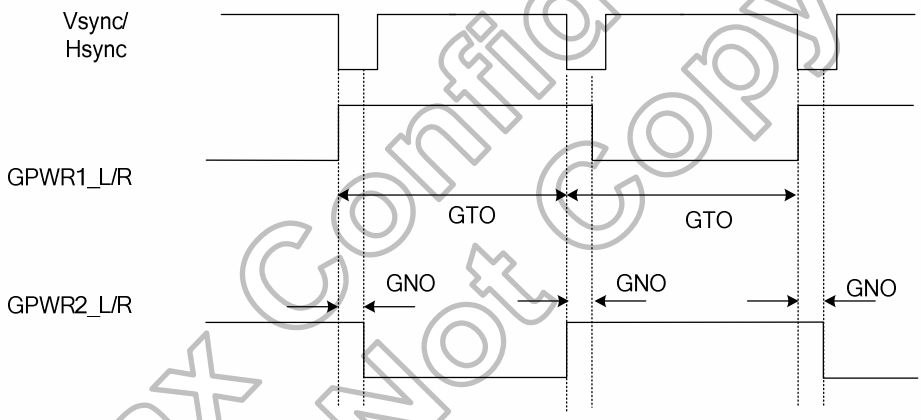
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Non-overlap timing depends on GNO[7:0] setting.

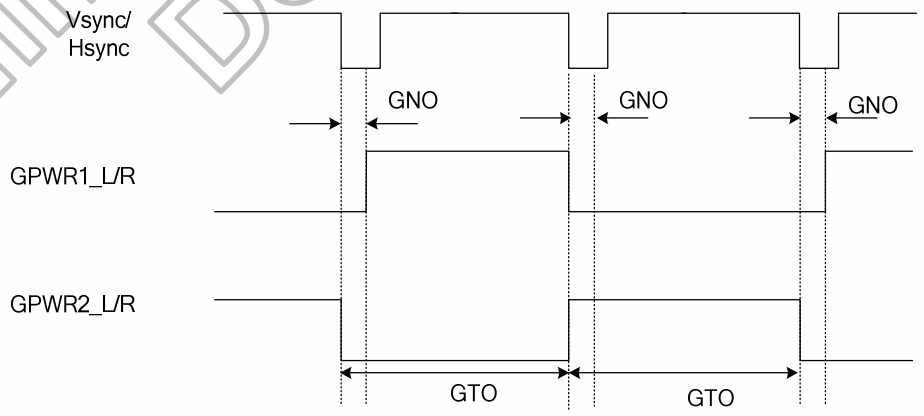
GPWR1/2 non-overlap signal are as below:



GPWR1/2 overlap signal are as below:



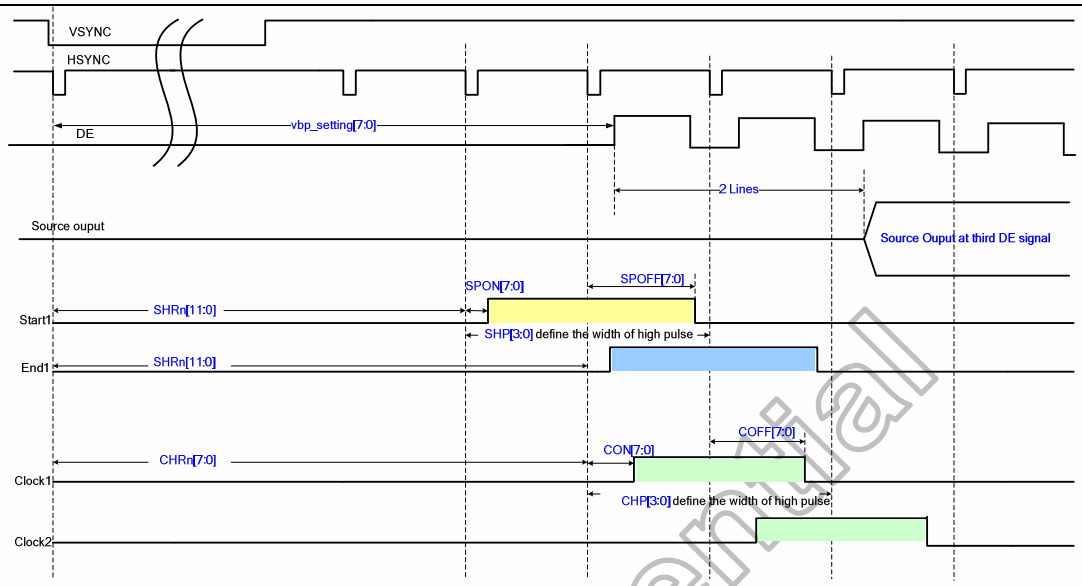
GPWR1/2 : one-side non-overlap , one-side in the same edge as below (when set **OVERLAP_OPT**=1)



USER_GIP_Gate[7:0]: Set the GIP dummy clock numbers for first CKV.

USER_GIP_Gate1[7:0]: Set the GIP dummy clock numbers for second CKV.

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Group0:
SHR0[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=0.
SHR0_GS[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=1.
SHR0_1 / SHR0_2 / SHR0_3[3:0]: Set the 2nd/3rd/4th Start / End signal delay from the 1st Start/End signal.

Group1:
SHR1[11:0]: Set the 1st Start/End siganl delay from VSYNC falling edge when GS=0.
SHR1_GS[11:0]: Set the 1st Start/End siganl delay from VSYNC falling edge when GS=1.

Group2:
SHR2[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=0.
SHR2_GS[11:0]: Set the 1st Start/End signal delay from VSYNC falling edge when GS=1.

SHR0/SHR1/SHR2[11:0] SHR0_GS/SHR1_GS/SHR2_GS[11:0]	Start signal output delay
0x000h	2 x Hsync
0x001h	3 x Hsync
0x002h	4 x Hsync
:	:
0xFFEh	4096 x Hsync
0xFFFh	4097 x Hsync

SHR0_1 SHR0_2 SHR0_3	2nd Start / End signal output delay 3th Start / End signal output delay 4th Start / End signal output delay
0000	0 x Hsync
0001	1 x Hsync
0010	2 x Hsync
:	:
1110	14 x Hsync
1111	15 x Hsync

SCP[3:0]: Numbers of output Start and End signal.

SCP3	SCP2	SCP1	SCP0	Start and End numbers
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
:				:
1	1	0	1	14

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1	1	1	0	15
1	1	1	1	16

SHP0/1/2[3:0]: Width of Start and End signal high pulse.

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x Hsync
0	0	0	1	2 x Hsync
0	0	1	0	3 x Hsync
:				:
1	1	1	0	15 x Hsync
1	1	1	1	16 x Hsync

CHR0[7:0]/CHR1[7:0]: Set the Clock signal delay from VSYNC falling edge when GS=0.
CHR0_GS[7:0]/CHR1_GS[7:0]: Set the Clock signal delay from VSYNC falling edge when GS=1.

CHR0[7:0]/CHR0_GS[7:0] CHR1[7:0]/CHR1_GS[7:0]	Clock signal output delay
0x00h	2 x HSYNC
0x01h	3 x HSYNC
0x02h	4 x HSYNC
:	:
0xFEh	256 x HSYNC
0xFFh	257 x HSYNC

CCP0[3:0]/CCP1[3:0]: Numbers of Output Clock signal.

CCP0[3:0]/CCP1[3:0]				Clock nunbers
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
:				:
1	1	1	0	15
1	1	1	1	16

CHP0[3:0]/CHP1[3:0]: Width of Clock signal high pulse.

CHP0[3:0]/CHP1[3:0]				Clock signal width
0	0	0	0	1 x Hsync
0	0	0	1	2 x Hsync
0	0	1	0	3 x Hsync
:				:
1	1	1	0	15 x Hsync
1	1	1	1	16 x Hsync

Restrictions: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.20 SETGIP_1: Set forward GIP sequence (D5h)

D5H	SETGIP_1(Set Forward GIP sequence)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	1	0	1	D5
1st parameter	1	Parameter 1st ~ parameter 35th are not OPEN in this datasheet. These parameters are GIP pin assignment for forward scan. Himax will provide this D5h setting in application note.								-
2nd parameter	1									-
3rd parameter	1									-
4th parameter	1									-
5th parameter	1									-
6th parameter	1									-
7th parameter	1									-
8th parameter	1									-
9th parameter	1									-
10th parameter	1									-
11st parameter	1									-
12nd parameter	1									-
13rd parameter	1									-
14th parameter	1									-
15th parameter	1									-
16th parameter	1									-
17th parameter	1									-
18th parameter	1									-
19th parameter	1									-
20th parameter	1									-
21st parameter	1									-
22nd parameter	1									-
23rd parameter	1									-
24th parameter	1									-
25th parameter	1									-
26th parameter	1									-
27th parameter	1									-
28th parameter	1									-
29th parameter	1									-
30th parameter	1									-
31st parameter	1									-
32nd parameter	1									-
33rd parameter	1									-
34th parameter	1									-
35th parameter	1									-
Description	Parameter 1st ~ parameter 35th are not OPEN in this datasheet. These parameters are GIP pin assignment for forward scan. Himax will provide this D5h setting in application note.									
Restrictions	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.21 SETGIP_2: Set backward GIP sequence (D6h)

D5H	SETGIP_2(Set backward GIP sequence)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	1	0	1	D6
1st parameter	1	Parameter 1st ~ parameter 32nd are not OPEN in this datasheet. These parameters are GIP pin assignment for Backward scan. Himax will provide this D6h setting in application note.								-
2nd parameter	1									-
3rd parameter	1									-
4th parameter	1									-
5th parameter	1									-
6th parameter	1									-
7th parameter	1									-
8th parameter	1									-
9th parameter	1									-
10th parameter	1									-
11st parameter	1									-
12nd parameter	1									-
13rd parameter	1									-
14th parameter	1									-
15th parameter	1									-
16th parameter	1									-
17th parameter	1									-
18th parameter	1									-
19th parameter	1									-
20th parameter	1									-
21st parameter	1									-
22nd parameter	1									-
23rd parameter	1									-
24th parameter	1									-
25th parameter	1									-
26th parameter	1									-
27th parameter	1									-
28th parameter	1									-
29th parameter	1									-
30th parameter	1									-
31st parameter	1									-
32nd parameter	1									-
Description	Parameter 1st ~ parameter 32nd are not OPEN in this datasheet. These parameters are GIP pin assignment for backward scan. Himax will provide this D6h setting in application note.									
Restrictions	-									
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In or Booster Off — Availability: Yes									

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6.3.22 SETGAMMA: Set gamma curve related setting (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1st Parameter	1	-	-	VRP0[5:0]						05
2nd parameter	1	-	-	VRP1[5:0]						0C
3rd parameter	1	-	-	VRP2[5:0]						13
4th parameter	1	-	-	VRP3[5:0]						20
5th parameter	1	-	-	VRP4[5:0]						39
6th parameter	1	-	-	VRP5[5:0]						3F
7th parameter	1	-	PRP0[6:0]							24
8th parameter	1	-	PRP1[6:0]							39
9th parameter	1	-	-	-	PKP0[4:0]					08
10th parameter	1	-	-	-	PKP1[4:0]					0A
11st parameter	1	-	-	-	PKP2[4:0]					0C
12nd parameter	1	-	-	-	PKP3[4:0]					16
13rd parameter	1	-	-	-	PKP4[4:0]					10
14th parameter	1	-	-	-	PKP5[4:0]					16
15th parameter	1	-	-	-	PKP6[4:0]					1A
16th parameter	1	-	-	-	PKP7[4:0]					17
17th parameter	1	-	-	-	PKP8[4:0]					17
18th parameter	1	-	-	-	PKP9[4:0]					06
19th parameter	1	-	-	-	PKP10[4:0]					0D
20th parameter	1	-	-	-	PKP11[4:0]					0F
21st parameter	1	-	-	-	PKP12[4:0]					12
22nd parameter	1	-	-	VRN0[5:0]						05
23rd parameter	1	-	-	VRN1[5:0]						0C
24th parameter	1	-	-	VRN2[5:0]						11
25th parameter	1	-	-	VRN3[5:0]						27
26th parameter	1	-	-	VRN4[5:0]						3B
27th parameter	1	-	-	VRN5[5:0]						3F
28th parameter	1	-	PRN0[6:0]							21
29th parameter	1	-	PRN1[6:0]							3A
30th parameter	1	-	-	-	PKN0[4:0]					04
31st parameter	1	-	-	-	PKN1[4:0]					07
32nd parameter	1	-	-	-	PKN2[4:0]					0B
33rd parameter	1	-	-	-	PKN3[4:0]					16
34th parameter	1	-	-	-	PKN4[4:0]					0F
35th parameter	1	-	-	-	PKN5[4:0]					15
36th parameter	1	-	-	-	PKN6[4:0]					17
37th parameter	1	-	-	-	PKN7[4:0]					15
38th parameter	1	-	-	-	PKN8[4:0]					16
39th parameter	1	-	-	-	PKN9[4:0]					06
40th parameter	1	-	-	-	PKN10[4:0]					0D
41st parameter	1	-	-	-	PKN11[4:0]					11
42nd parameter	1	-	-	-	PKN12[4:0]					17

Description

This command is to set gamma register.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	88-to-1 selector (voltage level of grayscale 52)
	PRP1 6-0	PRN1 6-0	88-to-1 selector (voltage level of grayscale 203)
Micro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 12)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 76)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 100)

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		PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 131)
		PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 155)
		PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 179)
		PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 227)
		PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 243)
		PKP9 4-0	PKN9 4-0	32-to-1 selector (voltage level of grayscale 20)
		PKP10 4-0	PKN10 4-0	32-to-1 selector (voltage level of grayscale 40)
		PKP11 4-0	PKN11 4-0	32-to-1 selector (voltage level of grayscale 215)
		PKP12 4-0	PKN12 4-0	32-to-1 selector (voltage level of grayscale 235)
	Offset Adjustment	VRP0 5-0	VRN0 5-0	64-to-1 selector (voltage level of grayscale 0)
		VRP1 5-0	VRN1 5-0	64-to-1 selector (voltage level of grayscale 4)
		VRP2 5-0	VRN2 5-0	64-to-1 selector (voltage level of grayscale 8)
		VRP3 5-0	VRN3 5-0	64-to-1 selector (voltage level of grayscale 247)
		VRP4 5-0	VRN4 5-0	64-to-1 selector (voltage level of grayscale 251)
		VRP5 5-0	VRN5 5-0	64-to-1 selector (voltage level of grayscale 255)
Restriction	SETEXTC turn on to enable this command.			

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

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6.3.23 SETCNCD/GETCNCD (FDh)

FDH	SETCNCD/GETCNCD (Set/Get Continue Command)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	1	1	1	0	1	FD
1st parameter	1	WR_CMD_CN[7:0]								-
Description	This function is use to instead of Register-Content interface mode. The parameter for SETCNCD will continue to write or read from the last command address automatically.									
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes									

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7. Layout Recommendation

7.1 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	5	Ω
VDD2	Power supply	5	Ω
VDD3, VDD3_P	Power supply	5	Ω
HS_VCC	Power supply	5	Ω
HS_VSS	Power supply	5	Ω
OTP_PWR	Power supply	5	Ω
VSSD, VSSD_P	Power supply	5	Ω
VSSA	Power supply	5	Ω
VSSAC	Power supply	20	Ω
IM[3:0]	Input	100	Ω
CSX, DCX, RESX, SCL_I2C_SCL	Input	100	Ω
HS, DE, VS, PCLK	Input	100	Ω
SDI_I2C_SDA	Input	100	Ω
SDO	Output	100	Ω
DB[23:0]	Input	100	Ω
NBWSEL	Input	100	Ω
GPO[3:0]	Output	100	Ω
CABC_PWM_OUT, CABC_LED_EN, TE_L, TE_R, IDLE_ON, LED_BOOST	Output	100	Ω
LED1,LED2	Output	10	Ω
VCOM	Output	10	Ω
HS_CLK_P, HS_CLK_N	Input	5	Ω
HS_D0P, HS_D0N	Input / Output	5	Ω
HS_D1P, HS_D1N,	Input	5	Ω
ERR	Output	100	Ω
DSWAP, PSWAP, LANSEL	Input	100	Ω
VDDD	Capacitor Connection	5	Ω
VCL	Capacitor Connection	10	Ω
VSP, VSN	Capacitor Connection	10	Ω
CSP,CSN	Input	10	Ω
VSPR, VSNR	Output	50	Ω
VREF	Capacitor Connection	20	Ω
VGH, VGL, VGL_REG	Capacitor Connection	10	Ω
VGH_REG	Capacitor Connection	50	Ω
VGHO_L/R, VGLO_L/R, LVGL_L/R	Output	10	Ω
HS_LDO	Capacitor Connection	5	Ω
HS_LDOL	Capacitor Connection	50	Ω
OSC	Input	100	Ω
C11P, C11N, C12P, C12N, C13P, C13N, C14P, C14N, C21P, C21N, C22P, C22N, C23P, C23N, C24P, C24N, C31P, C31N, C32P, C32N, C41P, C41N, C51P, C51N	Capacitor Connection	5	Ω
VCSW1, VCSW2	Output	10	Ω
CGOUT0_L/R~CGOUT15_L/R	Output	10	Ω
TEST[3:0]	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω

Table 7.1: Maximum Layout Resistance

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7.2 External Components Connection

Internal Charge Pump mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 μF
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)----| |--- (-)----- VSSA (Optional)	1.0 μF
VGL	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)----| |--- (-)----- VSSA	1.0 μF
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 μF
VGH_REG	C5	Connect to Capacitor (Max 25V): VGH_REG ---(+)----| |--- (-)-----VSSA (Optional)	1.0 μF
C11P – C11N	C11PN	Connect to Capacitor (Max 10V): C11P ---(+)----| |--- (-)-----C11N	1.0 μF
C12P – C12N	C12PN	Connect to Capacitor (Max 10V): C12P ---(+)----| |--- (-)-----C12N	1.0 μF
C13P – C13N	C13PN	Connect to Capacitor (Max 10V): C13P ---(+)----| |--- (-)-----C13N	1.0 μF
C14P – C14N	C14PN	Connect to Capacitor (Max 10V): C14P ---(+)----| |--- (-)-----C14N	1.0 μF
C21P – C21N	C21PN	Connect to Capacitor (Max 10V): C21P ---(+)----| |--- (-)-----C21N	1.0 μF
C22P – C22N	C22PN	Connect to Capacitor (Max 10V): C22P ---(+)----| |--- (-)-----C22N	1.0 μF
C23P – C23N	C23PN	Connect to Capacitor (Max 10V): C23P ---(+)----| |--- (-)-----C23N	1.0 μF
C24P – C24N	C24PN	Connect to Capacitor (Max 10V): C24P ---(+)----| |--- (-)-----C24N	1.0 μF
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)----| |--- (-)-----C31N	1.0 μF
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)----| |--- (-)-----C32N	1.0 μF
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)----| |--- (-)-----C41N	1.0 μF
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)----| |--- (-)-----C51N	1.0 μF
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)----| |--- (-)-----VSSA	2.2 μF
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)----| |--- (-)-----VSSA	2.2 μF
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(+)----| |--- (+)----- VSSA	2.2 μF
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 μF
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 μF
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA (Option)	1.0 μF
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F, Optional)	1.0 μF
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F)	1.0 μF
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 μF

Table 7.2: Adoptability of Components (Internal Charge Pump)

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HX5186-A/B/C mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 μF
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)----| |--- (-)----- VSSA (Optional)	1.0 μF
VGL	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)----| |--- (-)----- VSSA	1.0 μF
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 μF
VGH_REG	C5	Connect to Capacitor (Max 25V): VGH_REG ---(+)----| |--- (-)-----VSSA (Optional)	1.0 μF
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)----| |--- (-)-----C31N	1.0 μF
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)----| |--- (-)-----C32N	1.0 μF
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)----| |--- (-)-----C41N	1.0 μF
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)----| |--- (-)-----C51N	1.0 μF
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)----| |--- (-)-----VSSA	2.2 μF
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)----| |--- (-)-----VSSA	2.2 μF
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	2.2 μF
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 μF
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 μF
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA (Option)	1.0 μF
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F, Optional)	1.0 μF
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F)	1.0 μF
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 μF
HX5186-A/B/C	U1	Please refer HX5186-A/B/C datasheet	-
HX5186-A/B/C	C16	Please refer HX5186-A/B/C datasheet	1.0 uF
HX5186-A/B/C	C17	Please refer HX5186-A/B/C datasheet	1.0 uF
HX5186-A/B/C	C18	Please refer HX5186-A/B/C datasheet	1.0 uF

Table 7.3: Adoptability of Components (HX5186-A/B/C)

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VSN and VSP from External Charge Pump mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)----| |--- (-)----- VSSA (Optional)	1.0 µF
VGL	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)----| |--- (-)----- VSSA	1.0 µF
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
VGH_REG	C5	Connect to Capacitor (Max 25V): VGH_REG ---(+)----| |--- (-)-----VSSA (Optional)	1.0 µF
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)----| |--- (-)-----C31N	1.0 µF
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)----| |--- (-)-----C32N	1.0 µF
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)----| |--- (-)-----C41N	1.0 µF
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)----| |--- (-)-----C51N	1.0 µF
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)----| |--- (-)-----VSSA	2.2 µF
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	2.2 µF
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 µF
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA (Option)	1.0 µF
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F, Optional)	1.0 µF
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS (For MIPI DSI I/F)	1.0 µF
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 µF

Table 7.4: Adoptability of Components (VSN and VSP from External Charge Pump)

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8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~ VSSD	V	-0.3 to +3.6	Note(1),(2)
Power Supply Voltage 2	VDD2 ~ VSSA	V	-0.3 to +3.6	Note(1),(3)
Power Supply Voltage 3	VDD3 ~ VSSA	V	-0.3 to +3.6	Note(1) (4)
Power Supply Voltage 4	HS_VCC ~ HS_VSS	V	-0.3 to +3.6	Note(1) (5)
Power Supply Voltage 5	VSP ~ VSSA	V	-0.3 to +6.6	Note(6)
Power Supply Voltage 6	VSSA ~ VSN	V	0 to -6.6	Note(7)
Power Supply Voltage 7	VGH ~ VSSA	V	-0.3 to +25	Note(8)
Power Supply Voltage 8	VSSA ~ VGL	V	0 to -18	Note(9)
Operating Temperature	Topr	°C	-40 to +85	Note(10)
Storage Temperature	Tstg	°C	-55 to +110	Note(11)
Input Voltage	V_{IN}	V	-0.3 to VDD1+0.3	Note(12)
HS Input Voltage	V_{HSIN}	V	-0.3 to +2	Note(13)

Note: (1) VDD1, VSSD must be maintained.
(2) To make sure VDD1 ≥ VSSD.
(3) To make sure VDD2≥ VSSA.
(4) To make sure VDD3≥ VSSA.
(5) To make sure HS_VCC ≥ HS_VSS.
(6) To make sure VSP ≥ VSSA.
(7) To make sure VSSA ≥ VSN
(8) To make sure VGH ≥ VSSA.
(9) To make sure VSSA ≥ VGL, VGH +|VGL| < 30V
(10) For die and wafer products, specified up to +85℃.
(11) This temperature specifications apply to the TCP package.
(12) This specifications include input signals but without following: HS_CLK_P, HS_CLK_N, HS_D0P, HS_D0N, HS_D1P, HS_D1N.
(13) This specifications include following signals: HS_CLK_P, HS_CLK_N, HS_D0P, HS_D0N, HS_D1P, HS_D1N.

Table 8.1: Absolute Maximum Rating

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8.2 DC characteristics

(VDD2=2.5 ~3.6V, VDD3=2.5 ~ 3.6V, VDD1=1.65~3.3V, T_A=-40 ~ 85 °C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	VDD1=.65 ~ 13.3V VDD2= 2.5 ~ 3.6V VDD3= 2.5 ~ 3.6V	0.7 V_{DD1}	-	VDD1	V
Input low voltage	V_{IL}		0	-	0.3 V_{DD1}	V
OTP_PWR	V_{IH} V_{IL}	OTP_PWR	8.00V	8.25V	8.50V	V
Output high voltage (SDO, CABC_PWM_OUT, CABA_LED_EN, IDLE_ON, LED_BOOST)	V_{OH1}	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT, CABC_LED_EN, IDLE_ON, LED_BOOST)	V_{OL1}	VDD1= 1.65 ~ 3.6V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	µA
		RESX, DCX, CSX, SCL	-	-	1	µA
	I_{IHD}	DB[23:0], SDI, DCX	-	-	1	µA
		DB[23:0]	-	-	1	µA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		µA
		RESX, DCX, CSX, SCL	-1	-		µA
	I_{ILD}	DB[23:0], SDI, DCX	-1	-		µA
		DB[23:0]	-1	-		µA
Current consumption standby mode (LP-11)	$I_{ST(VDD2+VDD3)}$	VDD2/VDD3=2.8V, VDD1=1.8V HS_VCC=1.8V T_A =25°C	-	-	TBD	µA
Current consumption standby mode (LP-11)	$I_{ST(VDD1)}$		-		TBD	uA
Current consumption standby mode (LP-11)	$I_{ST(HS_VCC)}$			-	TBD	uA
Current consumption standby mode (ULPS)	$I_{ST(VDD2+VDD3)}$		-	-	TBD	µA
Current consumption standby mode (ULPS)	$I_{ST(VDD1)}$		-	-	TBD	uA
Current consumption standby mode (ULPS)	$I_{ST(HS_VCC)}$		-	-	TBD	uA

Note: The OTP_PWR pin is open on normal mode and in used while OTP programming condition.

Table 8.2: DC Characteristic

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8.3 AC characteristics

8.3.1 DBI Type C interface characteristics

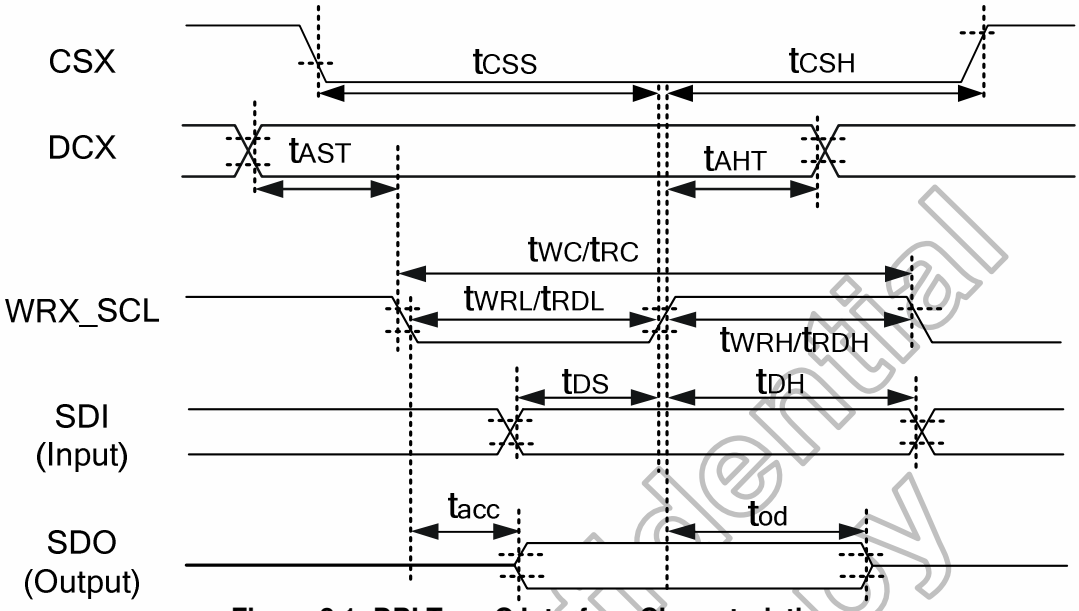


Figure 8.1: DBI Type C Interface Characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS} t_{CSH}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
DCX	t_{AST} I	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
WRX_SCL (Write)	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
WRX_SCL (Read)	t_{RC} t_{RDH} t_{RDL}	Read cycle Control pulse “H” duration Control pulse “L” duration	150 60 60	- - -	ns	-
SDI (Input)	t_{DS} t_{DT}	Data setup time Data hold time	30 30	- -	ns	For maximum C_L=30pF For minimum C_L=8pF
SDO (Output)	t_{RACC} t_{OD}	Read access time Output disable time	10 10	- 50	ns	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.3: DBI Type C Interface Characteristics

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8.3.2 DPI interface characteristics

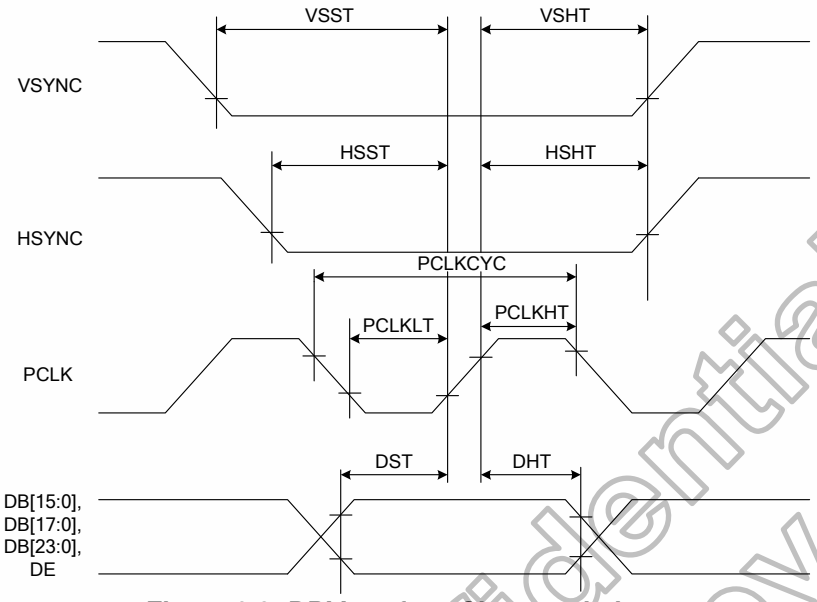


Figure 8.2: DPI Interface Characteristics

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR = Min . 50 Hz Max. 70 Hz	29.1(3)	-	46.2(4)	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR = Min . 50 Hz Max. 70 Hz	31(3)	-	49.2(4)	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 10 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) 30 MHz
(4) 27 MHz
(5) 26.7 MHz
(6) VRR : Vertical Refresh Rate, equal to VSYNC frequency.

Table 8.4: DPI Interface Characteristics

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Vertical timings for DPI I/F

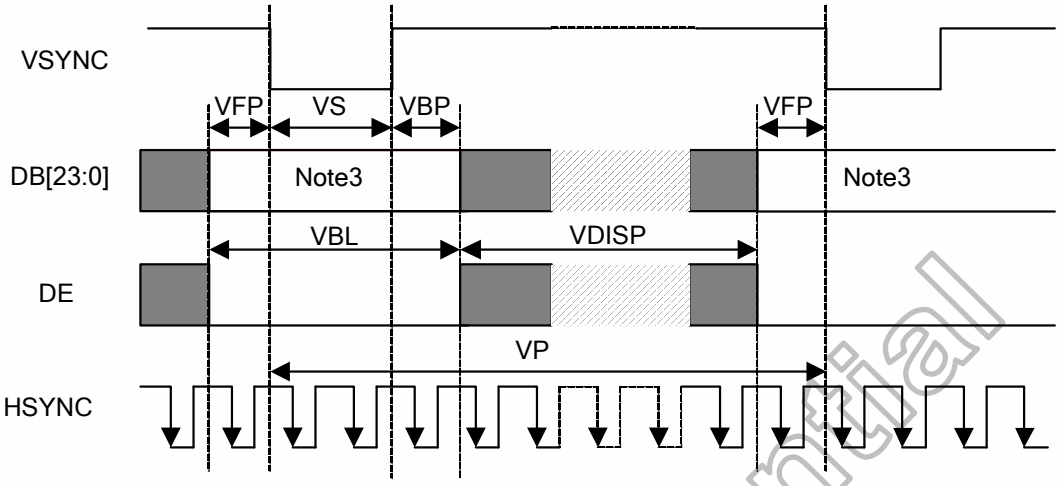


Figure 8.3: Vertical Timings for DPI I/F

Resolution=480x854(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Resolution=480x800(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 10 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(4) The VS and VBP pulse width are related to GIP and CLK timing. The GIP and CLK must be set at corresponding position for LCD normal display.

Table 8.5: Vertical Timings for DPI I/F

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Horizontal timings for DPI I/F

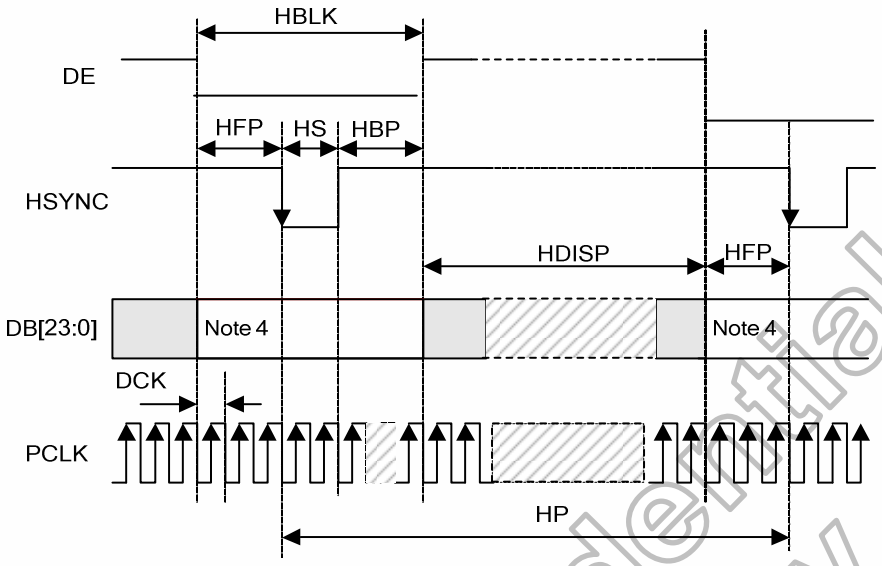


Figure 8.4: Horizontal Timing for DPI I/F

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	480	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = Min. 50Hz Max. 70Hz	21.6	-	34.3	MHz

Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	480	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = Min. 50Hz Max. 70Hz	20.3	-	32.2	MHz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight PCLK.
(4) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(5) HS+HBP must large than 1us.

Table 8.6: Horizontal Timing for DPI I/F

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8.3.3 Reset input timing

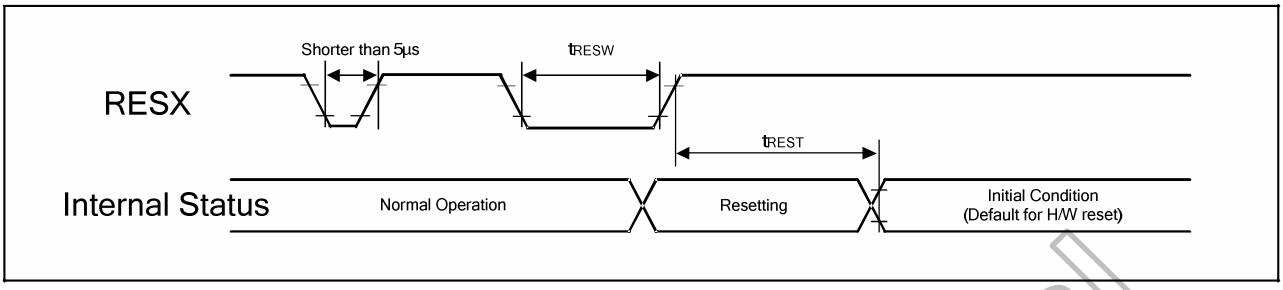


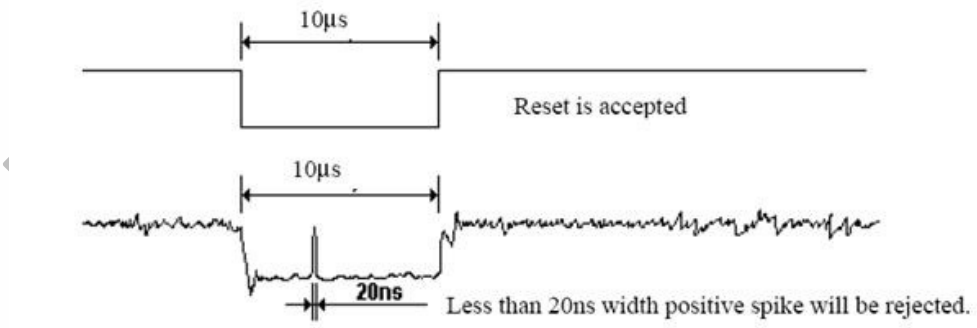
Figure 8.5: Reset Input Timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.7: Reset Timing

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8.3.4 DSI D-PHY electrical characteristics

8.3.4.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

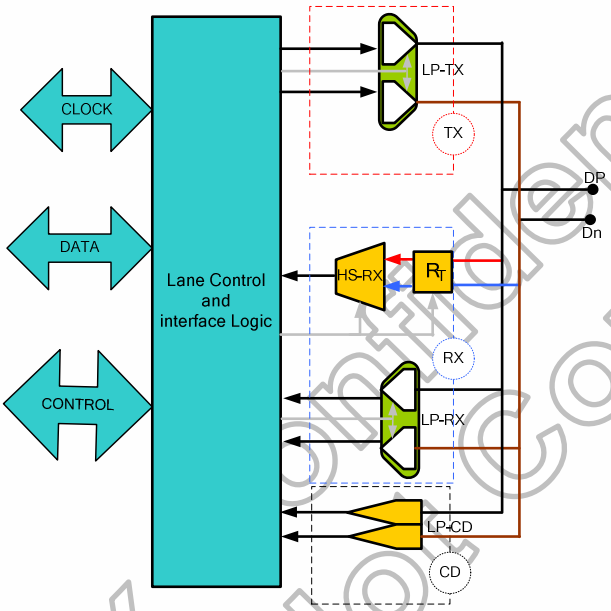


Figure 8.6: Electrical Functions of a Fully D-PHY Transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. Figure 8.7 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

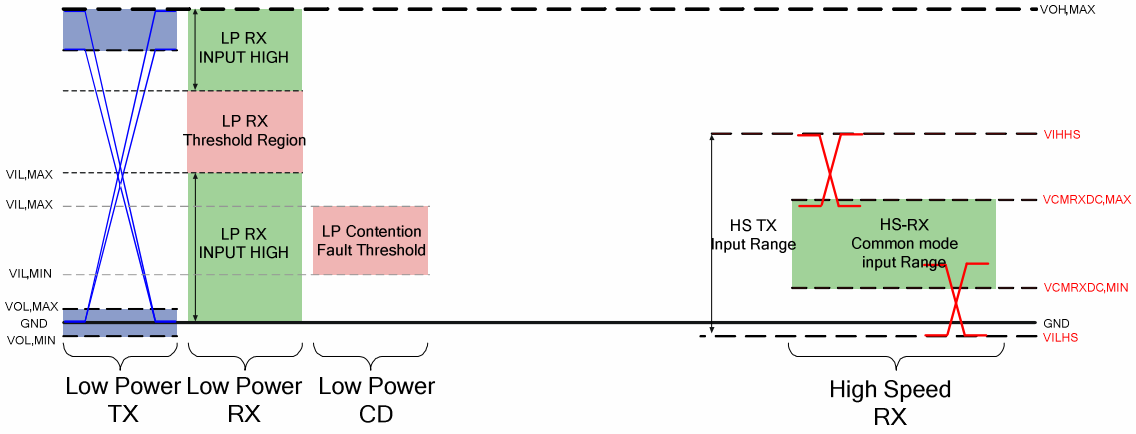


Figure 8.7: HS and LP Signal Levels

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8.3.4.2 Electrical characteristics of low-power transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.8: LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns	TX_OSC=0 (10)
		100	-	-	ns	TX_OSC=1 (10)
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(abs-max).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in mini-volts.
(9) When the output voltage is between 700 mV and 930 mV.
(10) TX_OSC is internal register setting.

Table 8.9: LP Transmitter AC Specifications

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8.3.4.3 Electrical characteristics of receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.3.4.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.10: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.11: HS Receiver AC Specifications

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8.3.4.5 Low-power receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.8 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

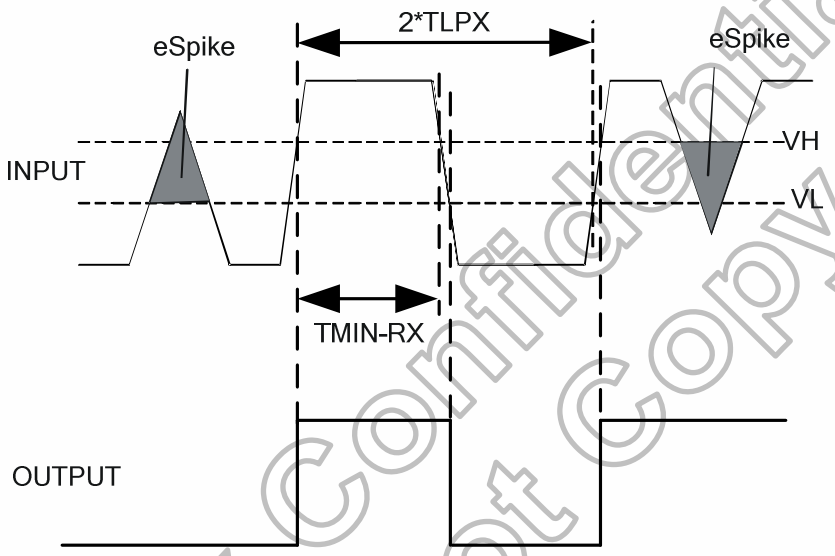


Figure 8.8: Input Glitch Rejections of Low-power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.12: LP receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	(1),(2), (3)
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	(4)
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 8.13: LP Receiver AC Specifications

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8.3.4.6 Line contention detection

Contention can be inferred from any of the following conditions:

A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL}.
B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{IL}.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.14: Contention Detector DC Specifications

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8.3.4.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

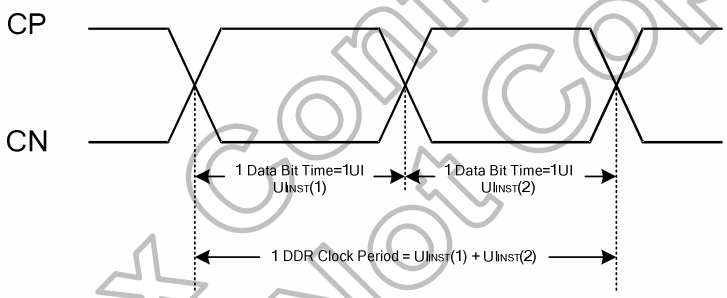


Figure 8.9: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

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The UI_{INST} specifications for the Clock signal are summarized in Table 8.15.

DSI Mode	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
550Mbps @ 2-lane	UI instantaneous	UI_{INST}	1.82	-	12.5	ns	(1) (2)

Note: (1) This value 1.82ns corresponds to a maximum 550 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate
(2) This value 1.82ns spec is base on 24bpp format.

Table 8.15: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

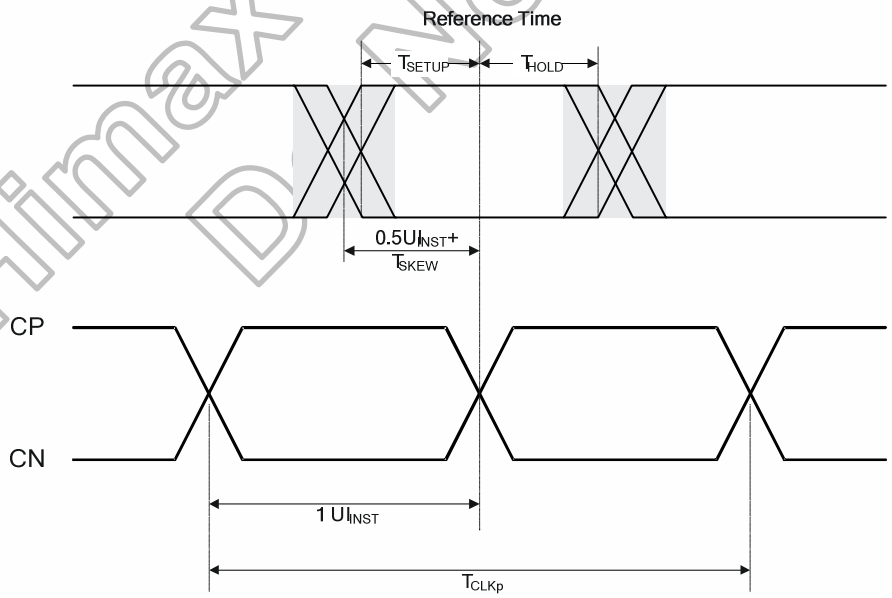


Figure 8.10: Data to Clock Timing Definitions

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8.3.4.8 Data-clock timing specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UI_{INST}, MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*U_{IINST}, i.e. ±0.2*UI_{INST} for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	1
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of 0.3*UI_{INST}.

Table 8.16: Data to Clock Timing Specifications

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8.3.5 Timings for DSI video mode

8.3.5.1 Vertical timings

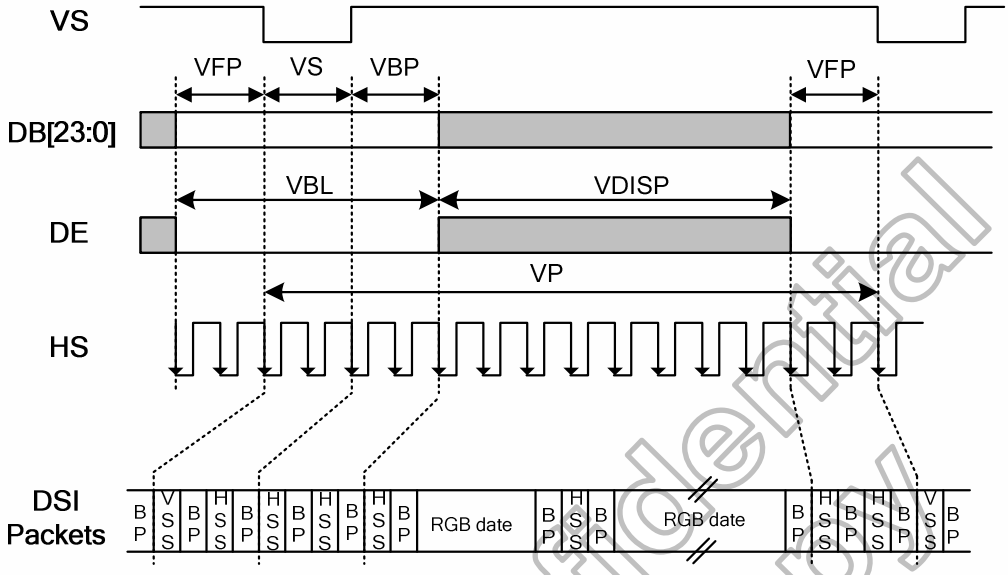


Figure 8.11: Vertical Timings for DPI I/F

Resolution=480x854(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	-	Line
Vertical low pulse width	VS	-	2	-	255(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	255(1)	Line
Vertical data start point	-	VS+VBP	4	-	255(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.17: Vertical Timings for DPI I/F

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8.3.5.2 Horizontal timings

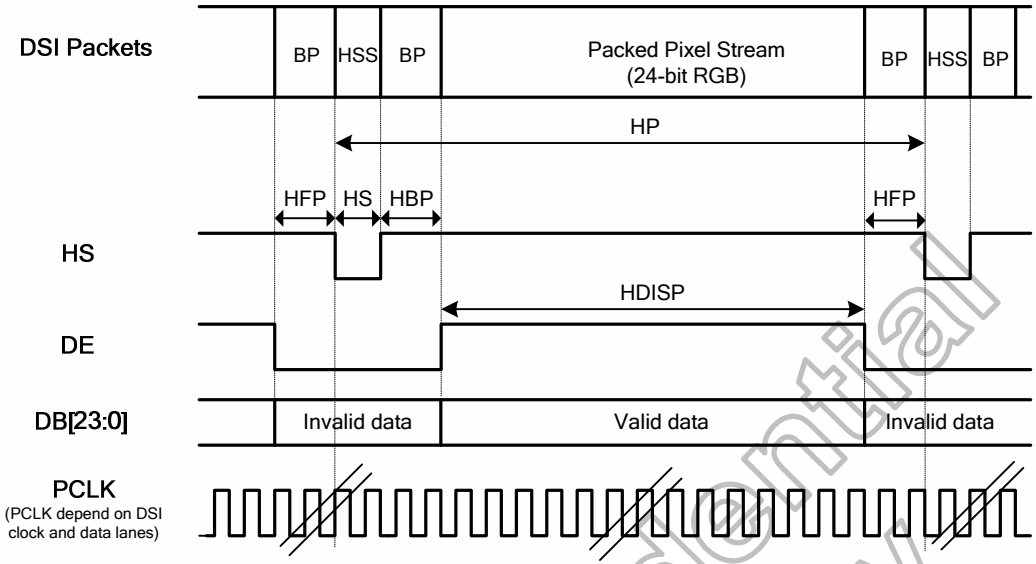


Figure 8.12: Horizontal Timing for DSI Video Mode I/F

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=HS_VCC=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	0.2	-		us
Horizontal back porch	HBP	-	1	-		us
Horizontal front porch	HFP	-	1	-		us
Horizontal data start point	-	HS+HBP	1.2	-		us
Horizontal blanking period	HBLK	HS+HBP+HFP	2.2	-		us
Horizontal active area	HDISP	-	-	480	-	DCK

Table 8.18: Horizontal Timings for DSI Video Mode I/F

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8.3.6 I2C AC characteristics

Characteristics of SDA and SCL bus lines for I2C-bus devices

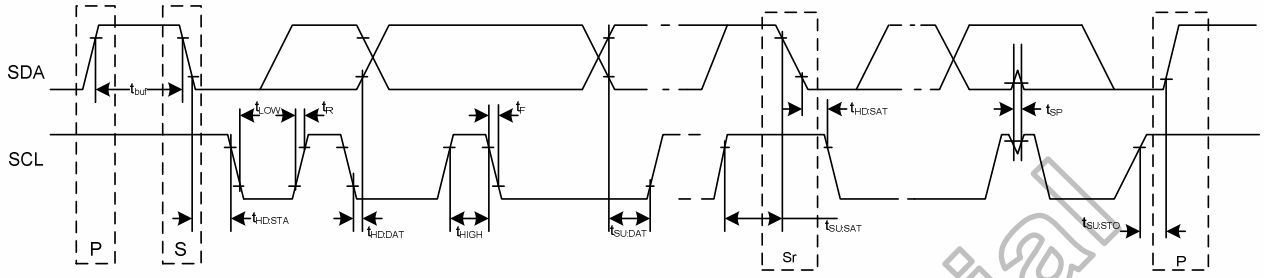


Figure 8.13 I2C Timing

Parameter	Symbol	Standard-Mode I2C-BUS		Fast-Mode I2C-BUS		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0	-	0.6	-	μs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	μs
Data hold time	$t_{HD:DAT}$	0	-	0	0.9	μs
Data set-up time	$t_{SU:DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	20+0.1 C_b	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	20+0.1 C_b	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	0.6	-	μs
Capacitive load for each bus line.	C_b	-	400	-	400	pF

Note: (1) All values are referred to VIH (0.7xVCCIO) and VIL (0.3xVCCIO) level.

(2) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

(3) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(4) A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{SU:DAT} \geqq$ 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max} + t_{SU:DAT}$ = 1000+250=1250ns (according to the standard-mode I2C-bus specification) before the SCL line is released.

(5) C_b = total capacitance of one bus line in pF.

Table 8.19: I2C Timing Spec.

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9. Ordering Information

Part No.	Package
HX8379-C000 PDxxx	PD: mean COG xxx: mean chip thickness (μm), (default: 200 μm)

10. Revision History

Version	Date	Description of Changes
01	2013/12/31	New Edition.

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