PHOENIX DISPLAY INTERNATIONAL, INC.

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SPECIFICATION FOR LCD MODULE

CUSTOMER	
PART NUMBER	PDIAT549FMS1
DESCRIPTION	5.49" FHD AMOLED
VERSION	10.0
ISSUE DATE	

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Reversion History			
Reversion. No	Date	Contents	Remark
01	2015-6-16	First version	
02	2015-10-12	Update mechanical test, JNCD, TP 72 pin description，Brightness，CR	
03	2015-11-02	Update mechanical test	
04	2015-12-14	Update Pin Define	
05	2016-01-14	Update Optical Spec	
06	2016-01-19	Update Outline Drawing	
07	2016-02-16	Update Optical Spec（W CIE）	
08	2016-03-18	Update Optical Spec（Red, Green CIE）, JNCD Spec	
09	2016-04-08	Update Optical Spec(Gray CCT, Duv), Touch Sensor Spec	
10	2016-04-19	Update Image retention Pattern	

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1 Scope

This Specification defines AMOLED manufactured by A-TOPS ELECTRONICSCO.,LTD In the case of any unspecified item, it may require both A-TOPS and the party designs this module into its product to work out a solution.

2 Features

2.1 Product Applications

mobile phone, portable GPS, handheld game console…

2.2 Product Features

2.2.1 Display color：16.7M (RGB x 8bits)

2.2.2 Display format：5.49”FHD(1080RGBx1920)

2.2.3 Pixel arrangement： Rendering

2.2.4 Interface： MIPI 4 lanes

2.2.5 Driver IC : RM67191 (Raydium)

2.2.6 Touch screen： On-Cell 72 Pin

2.2.7 Module type: Panel + IC(Panel without bonding IC, with polarizer)

3 Mechanical Specifications

Item	Specification	unit
Dimension outline	70.66 *128.36*0.64	mm
Encapsulation outline	70.66 *125.11	mm
Resolution	1080 RGB x 1920	dots
Active area	68.30 x 121.42	mm
Diagonal size	5.49	inch
Pixel pitch	31.62*63.24	μm
Glass thickness （LTPS/encapsulation glass）	0.20 / 0.30	mm

4 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
VCI I/O voltage	VCI_IF	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
VSP voltage	VSP	-0.3	-	6.6	V	-
VPP(OTP power)	VPP	-	-	8.64	V	-
Operating temperature	Top	-40		85	℃	
Storage temperature	Tstg	-55		125	℃	

5 Electrical Specifications

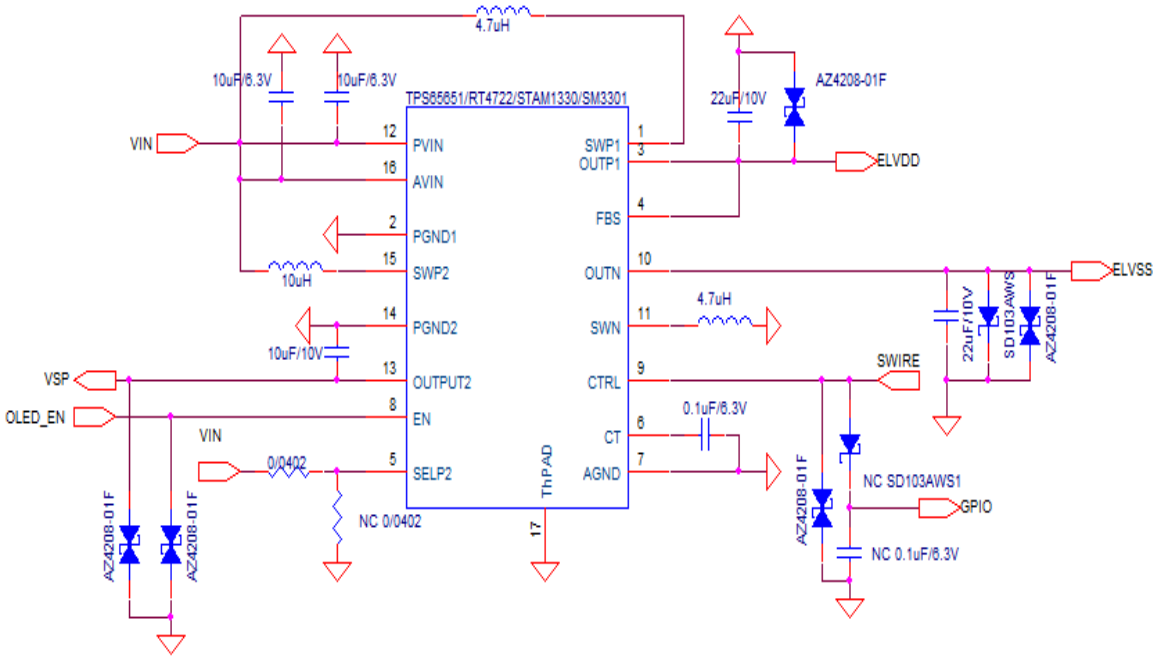
5.1 Electrical Characteristics

5.1.1 Current Characteristic：

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	-	4.6	-	V	
AMOLED power Negative	ELVSS	-	-2.5	-	V	Ref
Gamma Voltage	VSP	6.3	6.4	6.5	V	Ref
Digital Power supply	VDDI	1.65	1.8	3.6	V	Ref
Analog Power supply	VCI	2.5	3.3	4.8	V	Ref

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
350 nits @Gray 255	$I_{ELVDD/ELVSS}$	VELVDD=4.6V VELVSS=-2.5V VCI=3.3V VDDIO=1.8V VSP=6.4V	-	190	230	mA	
	I_{VCI}		-	2	3	mA	
	I_{VDDIO}		-	50	55	mA	
	I_{VSP}		-	15	150	mA	

5.1.2 Application circuit：



5.2 Pin Description

5.2.1 I/O Connection

Reference Number	Pin name	Type	Description
1	NC_1		NC
2	DR_R	I	NC
3	DG_R	I	NC
4	DB_R	I	NC
5	SW2_R	I	The potential pull VDD
6	SW1_R	I	The potential pull VDD
7	VEE_1	I	VGL regulated output voltage
8	VDD_1	I	VGH regulated output voltage.
9	VINT_1	O	Regulated output voltage
10	STER	O	NC
11	CKE2R	O	NC
12	CKE1R	O	NC
13	CKV1R	O	GEOA signal
14	CKV2R	O	GEOA signal
15	STVR	O	GEOA signal
16	NC_2		NC
17	ELVSS_1	I	AMOLED Power negative
18	ELVSS_2	I	

19	ELVSS_3	I	
20	NC_3		NC
21	ELVDD_1	I	AMOLED Power positive
22	ELVDD_2	I	
23	ELVDD_3	I	
24	NC_4		NC
25	ARSW4	I	The potential pull VDD
26	ARSW5	I	
27	ARSW6	I	
28	OLB1	O	FOG_L1 for panel test.
29	OLB2	O	FOG_L2 for panel test.
30	PASS1	O	NC
31	PADA	O	NC
32	PCD_L	O	Panel Crack Detection
33	PASS1_1	I/O	PASS1 ~ PASS3 are bypass path for panel used, current limited < 30mA and voltage limited < 20V.
34	PASS1_2		
35	MTP_PWR	P	Power supply for OTP. Float it for normal operation.
36	VDDI_1	P	Digital circuit I/O power supply
37	VDDI_2		
38	VDDI_3		
39	TE_L	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin.
40	AVSS_1	P	System ground for source OP system
41	AVSS_2		
42	AVSS_3		
43	VGHR_1	O	Output voltage generated from VGH.
44	VGHR_2		
45	VGHR_3		
46	VGLR_1	O	Output voltage generated from VGL.
47	VGLR_2		
48	VGL_1	O	Charge pump's output voltage.
49	VGL_2		
50	VGL_3		
51	C24N_1	I/O	Capacitor connection pins for the step_up circuit to generate VGL
52	C24N_2		
53	C24N_3		
54	C24P_1		
55	C24P_2		
56	C24P_3		
57	C23N_1		
58	C23N_2		
59	C23N_3		
60	C23P_1		

61	C23P_2		
62	C23P_3		
63	AVDD_1	I	PFM's output voltage.
64	AVDD_2		
65	AVDD_3		
66	VDDB_1	P	Power supply for DC/DC circuit
67	VDDB_2		
68	VDDB_3		
69	VSSB_1	P	System ground for DC/DC converter
70	VSSB_2		
71	VSSB_3		
72	AVEE_1	O	Output voltage generated from AVDD
73	AVEE_2		
74	AVEE_3		
75	C51N_1	I/O	Capacitor connection pins for the step_up circuit to generate AVEE
76	C51N_2		
77	C51N_3		
78	C51P_1		
79	C51P_2		
80	VCL_1	O	Output voltage generated from VDDB
81	VCL_2		
82	VCL_3		
83	C41N_1	I/O	Capacitor connection pins for the step_up circuit to generate VCL
84	C41N_2		
85	C41N_3		
86	C41P_1		
87	C41P_2		
88	C41P_3		
89	VSSA_1	P	System ground for Analog system.
90	VSSA_2		
91	VDDA_1	P	Power supply for Analog circuit.
92	VDDA_2		
93	VDDA_3		
94	DVSS_1	P	System ground for internal digital system.
95	DVSS_2		
96	DVSS_3		
97	DVDD_1	O	Regulator output for logic system power.
98	DVDD_2		
99	DVDD_3		
100	VCC_1	P	Power supply for DVDD regulator.
101	VCC_2		
102	VCC_3		
103	VDDAM_1	P	Power supply for MIPI analog regulator system.
104	VDDAM_2		
105	VDDAM_3		

106	MVDDA_1	O	Regulator output for internal MIPI/MDDI analog system.
107	MVDDA_2		
108	VSSAM_1	P	Ground for MIPI interface.
109	D3P_1	I	MIPI data input pin.
110	D3P_2		
111	D3N_1		
112	D3N_2		
113	VSSAM_2	P	Ground for MIPI interface
114	D0P_1	I	MIPI data input pin.
115	D0P_2		
116	D0N_1		
117	D0N_2		
118	VSSAM_3	P	Ground for MIPI interface
119	CLKP_1	I	MIPI clock input pin.
120	CLKP_2		
121	CLKN_1		
122	CLKN_2		
123	VSSAM_4	P	Ground for MIPI interface
124	D1P_1	I	MIPI data input pin.
125	D1P_2		
126	D1N_1		
127	D1N_2		
128	VSSAM_5	P	Ground for MIPI interface
129	D2P_1	I	MIPI data input pin.
130	D2P_2		
131	D2N_1		
132	D2N_2		
133	VSSAM_6	P	Ground for MIPI interface
134	DVSS	P	System ground for internal digital system.
135	AVSS_4	P	System ground for source OP system.
136	AVSS_5		
137	AVSS_6		
138	AVDD_4	P	Power supply for analog system.
139	VDDI_4	P	Power supply for interface system except MIPI interface.
140	VDDI_5		
141	VDDI_6		
142	VSSI_1	P	Ground for digital circuit.
143	VSSI_2		
144	VSSI_3		
145	D7	I	Test pins.
146	D6		
147	D5		
148	D4		
149	D3		
150	D2		

151	D1		
152	D0		
153	DE		
154	HS		
155	VS		
156	PLK		
157	VSSI_4	P	Ground for digital circuit.
158	BSTM[2]	I	Boost mode selection pin. Default=111
159	BSTM[1]		
160	BSTM[0]		
161	LANSEL[1]	I	Select number of data lanes in MIPI interface. LANSEL[1:0]=11 4 data lanes LANSEL[1:0]=10 3 data lanes
162	LANSEL[0]		
163	PSWAP	I	Change MIPI pin's polarity.
164	DSWAP[2]		
165	DSWAP[1]		
166	DSWAP[0]		
167	RSTN	I	Reset SD IC. This signal is active low.
168	DCX	I	Display data/command selection in 8-bit SPI DCX=”0”:Command DCX=”1”:Display data or Parameter.
169	SDI	I/O	SPI data input.
170	SDO	O	SPI data output.
171	SCL	I	SPI clock input.
172	CSX	I	SPI chip select. Default : Initial pull low.
173	AVDD_5	P	Power supply for analog system.
174	AVDD_6		
175	AVDD_7		
176	AVSS_7	P	System ground for source OP system
177	AVSS_8		
178	AVSS_9		
179	AVSS_10		
180	VSSI_5	P	Ground for digital circuit.
181	VSSI_6		
182	VDDI_7	P	Digital circuit I/O power supply
183	VDDI_8		
184	BIST_EN	I	Normal/BIST/Aging model selection 00:Normal mode 01:Aging mode 10:BIST mode 11:BISE mode (Note : BIST_EN has higher priority than AGING_EN.)
185	AGING_EN		
186	OLED_EN	O	Power IC enable control pin
187	SWIRE	O	Power IC Swire setting pin.

188	VSSA_19	P	System ground for Analog system.
189	VSSA_10_1		
190	IM1	I	Interface type selection. Default : 2'b00 IM[1:0]=2'b00, Display data : MIPI DSI, Command : MIPI DSI or 16_bit SPI IM[1:0]=2'b01, Display data : N/A, Command : 9 bit SPI(SCL rising edge trigger),SDI/SDO IM[1:0]=2'b10, Display data : N/A, Command : 8 bit SPI(SCL rising edge trigger),SDI/SDO IM[1:0]=2'b11, Display data : N/A, Command : 16 bit SPI
191	IM0		
192	ANA_TEST1	O	NC
193	ANA_TEST0		
194	VDDA_4	P	Power supply for Analog circuit.
195	VDDA_5		
196	VDDA_6		
197	VGMP	O	Output voltage generated from AVDD.
198	VGSP	O	Output voltage generated from AVDD.
199	VREF	O	Regulated output for internal reference voltage.
200	AVSS_11	P	System ground for source OP system.
201	AVSS_12		
202	AVDD_8	P	Power supply for analog system.
203	AVDD_9		
204	DB_MODE[2]	I	NC
205	DB_MODE[1]		
206	DB_MODE[0]		
207	PCD	O	Panel Crack Detection pin.
208	ERR_FLAG	O	Error Flag output pin. (0=Normal, 1=Error Occurred)
209	TEST14	I/O	NC
210	TEST13		
211	TEST12		
212	TEST11		
213	TEST10		
214	TEST9		
215	TEST8		
216	TEST7		
217	TEST6		
218	TEST5		
219	TEST4		
220	TEST3		
221	TEST2		
222	TEST1		
223	VCC_4	P	Power supply for DVDD regulator.

224	DVSS_5	P	System ground for internal digital system.
225	DVSS_6		
226	DVSS_7		
227	DVDD_4	O	Regulator output for logic system power.
228	DVDD_5		
229	DVDD_6		
230	VCC_5	P	Power supply for DVDD regulator.
231	VCC_6		
232	VCC_7		
233	VREFP5_1	O	NC
234	VREFP5_2		
235	VINT_2	O	Regulated output voltage.
236	VINT_3		
237	VCL_4	O	Charge pump's output voltage.
238	VCL_5		
239	VCL_6		
240	AVEE_4	O	Output voltage generated from AVDD
241	AVEE_5		
242	AVEE_6		
243	EXTN_1	O	NC
244	EXTN_2		
245	EXTN_3		
246	EXTP_1	O	NC
247	EXTP_2		
248	VDDR_1	P	Power supply for regulator system.
249	VDDR_2		
250	VDDR_3		
251	VSSR_1	P	System ground for regulator system.
252	VSSR_2		
253	VSSR_3		
254	AVSS_13	P	System ground for source OP system.
255	AVSS_14		
256	AVSS_15		
257	AVDD_10	P	Power supply for analog system.
258	AVDD_11		
259	AVDD_12		
260	C21N_1	I/O	Capacitor connection pins for the step_up circuit to generate VGH.
261	C21N _2		
262	C21N _3		
263	C21P_1		
264	C21P _2		
265	C21P_3		
266	C22N_1		
267	C22N _2		

268	C22N _3		
269	C22P_1		
270	C22P _2		
271	C22P_3		
272	VGH_1	O	Charge pump's output voltage.
273	VGH_2		
274	VGH_3		
275	VGHR_4	O	Output voltage generated from VGH.
276	VGHR_5		
277	VGHR_6		
278	VDDB_4	P	Power supply for Analog circuit.
279	VDDB_5		
280	VSSB_1	P	System ground for DC/DC converter.
281	VSSB_2		
282	VSSB_3		
283	VGLR_3	O	Output voltage generated from VGL.
284	VGLR_4		
285	VGLR_5		
286	TE_R	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin.
287	VDDI_9	P	Digital circuit I/O power supply
288	VEQ_SD	P	Capacitor connection to ground.
289	PASS3_1	I/O	PASS1 ~ PASS3 are bypass path for panel used, current limited < 30mA and voltage limited < 20V.
290	PASS3_2		
291	PCD_R	O	Panel Crack Detection
292	PADB	I	NC
293	PASS3	I	NC
294	OLB3	O	FOG_L1 for panel test.
295	OLB4	O	FOG_L2 for panel test.
296	SW3	I	The potential pull VDD
297	SW2	I	The potential pull VDD
298	SW1	I	The potential pull VDD
299	NC_5		NC
300	ELVDD_4	I	AMOLED Power Positive
301	ELVDD_5	I	
302	ELVDD_6	I	
303	NC_6		NC
304	ELVSS_4	I	AMOLED Power Negative
305	ELVSS_5	I	
306	ELVSS_6	I	

307	NC_7		NC
308	STVL	O	GEOA signal
309	CKV2L	O	GEOA signal
310	CKV1L	O	GEOA signal
311	CKE2L	O	GEOA signal
312	CKE1L	O	GEOA signal
313	STEL	O	GEOA signal
314	VINT_6	O	Regulated output voltage
315	VDD_2	I	VGH regulated output voltage
316	VEE_2	I	VGL regulated output voltage
317	SW1_L	I	The potential pull VDD
318	SW2_L	I	The potential pull VDD
319	DB_L	I	NC
320	DG_L	I	NC
321	DR_L	I	NC
322	NC_8		NC

5.2.2 Touch IC Pin Description (72 Pin)

	Pin name	I/O	Description
1	NC		NC
2	GND		GND
3	Guard0		GND or Guard
4	TX1	0	Transmitter
5	TX2	0	Transmitter
6	TX3	0	Transmitter
7	TX4	0	Transmitter
8	TX5	0	Transmitter
9	TX6	0	Transmitter
10	TX7	0	Transmitter
11	TX8	0	Transmitter
12	TX9	0	Transmitter
13	TX10	0	Transmitter
14	TX11	0	Transmitter
15	TX12	0	Transmitter
16	TX13	0	Transmitter
17	TX14	0	Transmitter
18	TX15	0	Transmitter
19	TX16	0	Transmitter
20	TX17	0	Transmitter
21	GND		GND or Guard
22	TX17	0	Transmitter
23	TX16	0	Transmitter
24	TX15	0	Transmitter

25	TX14	O	Transmitter
26	TX13	O	Transmitter
27	TX12	O	Transmitter
28	TX11	O	Transmitter
29	TX10	O	Transmitter
30	TX9	O	Transmitter
31	TX8	O	Transmitter
32	TX7	O	Transmitter
33	TX6	O	Transmitter
34	TX5	O	Transmitter
35	TX4	O	Transmitter
36	TX3	O	Transmitter
37	TX2	O	Transmitter
38	TX1	O	Transmitter
39	GND		GND or Guard
40	RX30	I	Receiver
41	RX29	I	Receiver
42	RX28	I	Receiver
43	RX27	I	Receiver
44	RX26	I	Receiver
45	RX25	I	Receiver
46	RX24	I	Receiver
47	RX23	I	Receiver
48	RX22	I	Receiver
49	RX21	I	Receiver
50	RX20	I	Receiver
51	RX19	I	Receiver
52	RX18	I	Receiver
53	RX17	I	Receiver
54	RX16	I	Receiver
55	RX15	I	Receiver
56	RX14	I	Receiver
57	RX13	I	Receiver
58	RX12	I	Receiver
59	RX11	I	Receiver
60	RX10	I	Receiver
61	RX9	I	Receiver
62	RX8	I	Receiver
63	RX7	I	Receiver
64	RX6	I	Receiver
65	RX5	I	Receiver
66	RX4	I	Receiver
67	RX3	I	Receiver
68	RX2	I	Receiver
69	RX1	I	Receiver

70	Guard		GND or Guard
71	GND		GND
72	NC		NC

5.3 Touch Spec

TP Panel Test 假压阶段。

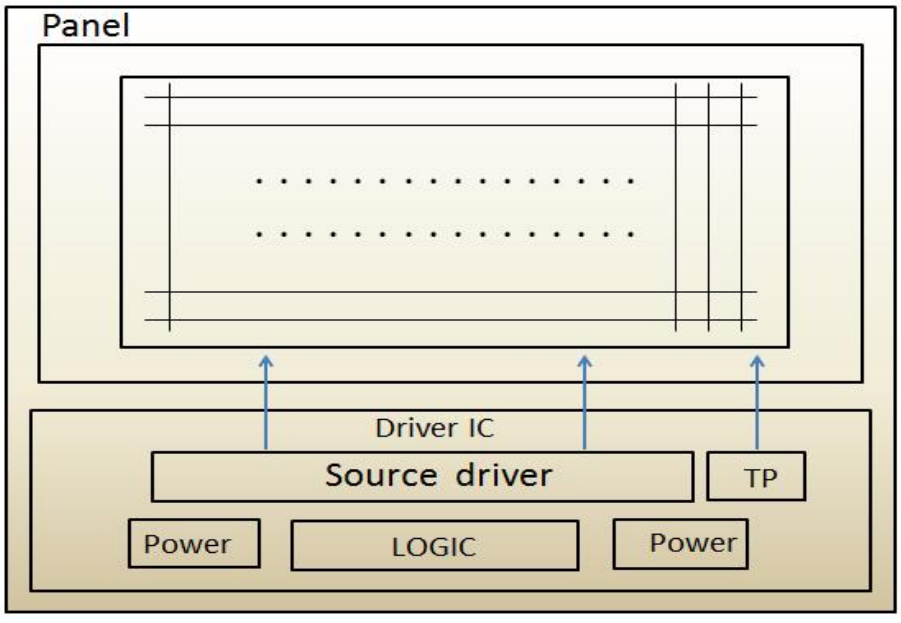
TP Panel Test 假压主要是通过软件测试 Panel 电容值的变化范围以确定 Panel 是否正常，电容值的变化在通过 IC 处理后以一定数值显示在软件中。

由于容值会受到外界复杂环境的影响，且 Touch IC 处理能力要求将 Rawdata 的变异量控制在一定的范围内，故在 Rawdata 的平均值基础上设定上下限，以保证制程导致的 Rawdata 的变异量能在 IC 处理范围以内。

因为偏光片距离 sensor 很近，且在其材质、厚度、大小都会对 Panel 电容值产生影响，经过验证的偏光片对 TP Panel Test 假压 Rawdata 的影响是均匀、同一的，故需重新设定上下限即可。

未偏贴偏光片 Rawdata 管控范围 ： 2800~3500
偏贴偏光片 Rawdata 管控范围 ： 3500~4200

6 Display Module Block Diagram



7 Electro-Optical Specification

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Brightness		Full White	315	350	385	cd/m^2	Center
Brightness Uniformity		Full White	75		-	%	Note2
Contrast Ratio	CR	Normal to surface	60,000		-	-	Note3

CIE Chromaticity	White	x	Normal to surface	0.28	0.30	0.32	-	
		y		0.30	0.32	0.34	-	
	Red	x		0.64	0.67	0.70	-	
		y		0.30	0.33	0.36	-	
	Green	x		0.16	0.20	0.24	-	
		y		0.68	0.72	0.76	-	
	Blue	x		0.10	0.13	0.16	-	
		y		0.03	0.06	0.09	-	
Color Gamut			vs. NTSC	90	105		%	
Viewing angle			U/D/L/R CR≥1000	80		-	°	
Color shift			@ 45 degree			4.5	JNCD	
Cross-talk			4% black or white window, 127 gray scale	-	-	2	%	Note4
Gamma			Full White	2.0	2.2	2.4	-	
Response time				-	-	2	ms	Note5
Color Temperature				6456	7356	8256	K	
Flicker			Normal Θ=Φ=0°			-40	dB	Note 6
Image Retention						3	min	Note 7
Color Uniformity			Full White Δu'v'			0.012		Note 8
Gray CCT			L64-L255			±300K		
Gray duv			L64-L255			0.006		

Note1: Temp.25℃，（Angle、distance）

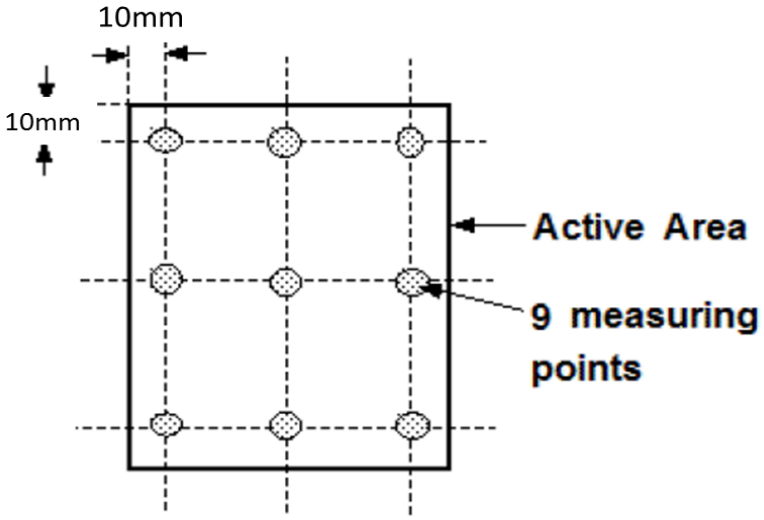
Environmental conditions：Temp.25℃±3℃, 65±20%RH, Dark Room.

Distance of OLED display center to measuring machine is 50cm.

Note2: Brightness Uniformity definition

Measure 9 points of Display Brightness,

Brightness Uniformity=L_{min}/L_{Max}×100%



Note3: Contrast Ratio

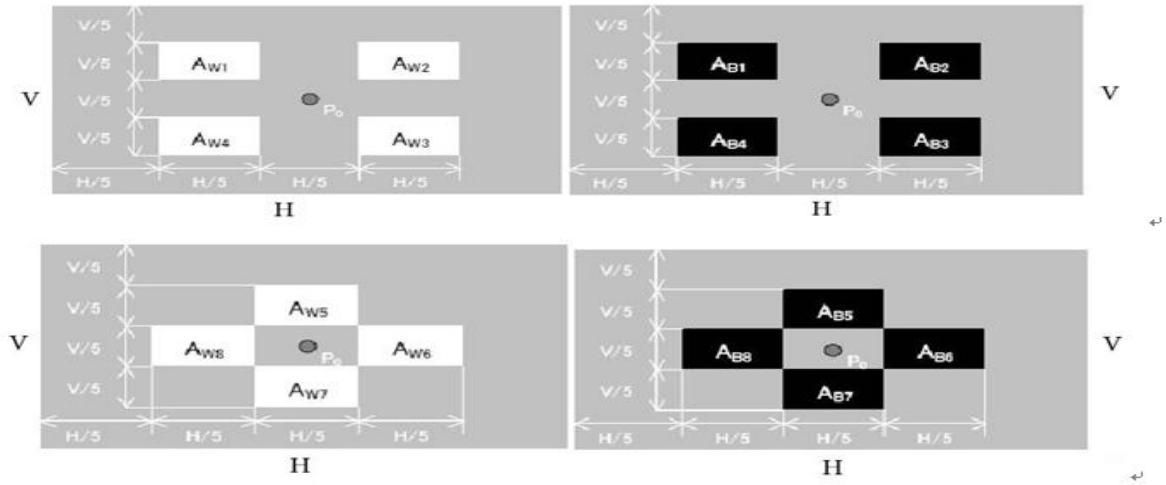
Dark Room C.R=LW/LB

LW: full white brightness of display center P0;

LB : full black brightness of display center P0.

Note4: Cross-talk

4% black or white window ， 127 gray background.



$$L_{W_OFF} = \frac{L_{w1} + L_{w2} + L_{w3} + L_{w4}}{4}$$

$$L_{B_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$CT = \frac{\left|L_{Wi_ON} - L_{W_OFF}\right|}{L_{W_OFF}} \times 100\% (i = 5\ to\ 8)$$

For white windows AWi (i = 5 to 8), and

$$CT = \frac{|L_{Bi_ON} - L_{B_OFF}|}{L_{B_OFF}} \times 100\% (i = 5 \text{ to } 8)$$

For black windows ABi (i = 5 to 8).
The maximum cross-talk value shall be noted in the measurement report.

Note5: Response Time

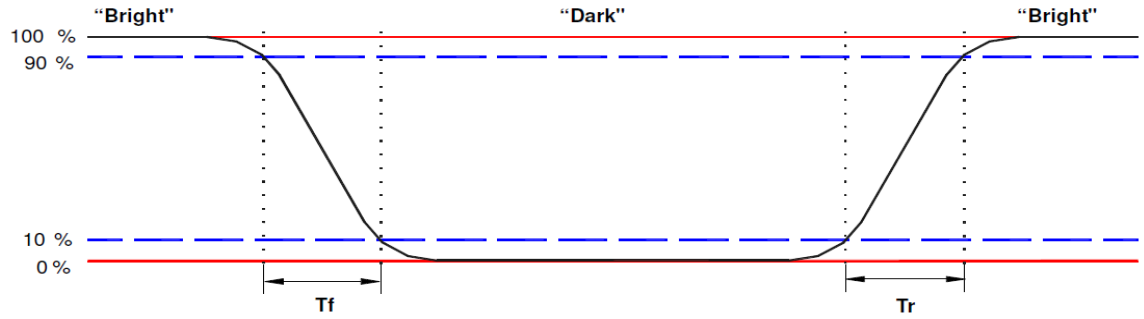
Response time=Pixel turn on and turn off time (White<=>Black).

It is measuring transition time from 10% to 90% of luminance.

Note5: Response Time

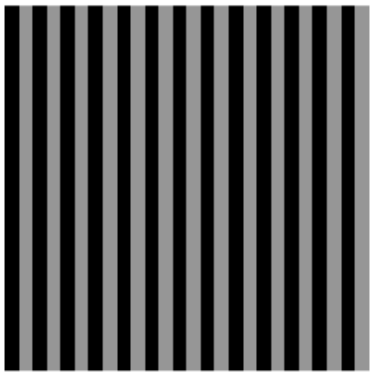
Response time=Pixel turn on and turn off time (White<=>Black).

It is measuring transition time from 10% to 90% of luminance.



Note 6: Flicker

Suggested Instruments: **Konica Minolta CA-310** or **Klein Instruments K-8**



Odd row : **L0** Black
Even row : **L186** gray level

Flicker Test Pattern

The flicker level is defined by **Fast Fourier Transformation (FTT)** as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad (dB)$$

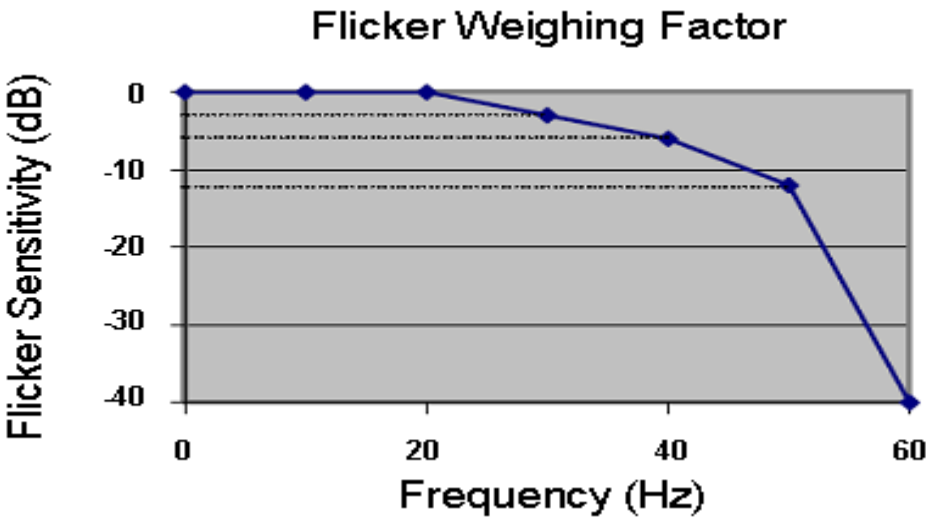
Where

$f_{FFTC}(n)$ is the n-th FFT coefficient.

$f_{FFTC}(0)$ is the 0-th FFT coefficient which is DC component.

FS(Hz) is the flicker sensitivity as a function of frequency.

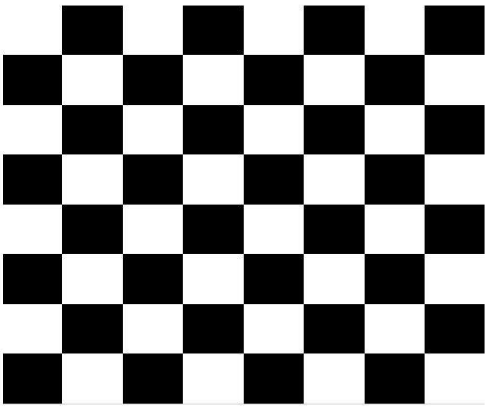
The peak flicker level shall be reported based on the calculation using above formula in which FS(Hz) is determined by the flicker weighing factor shown below.



Note7: Image Retention

Using chessboard pattern (8 * 8) light on 1hr, and switch to 127 gray.

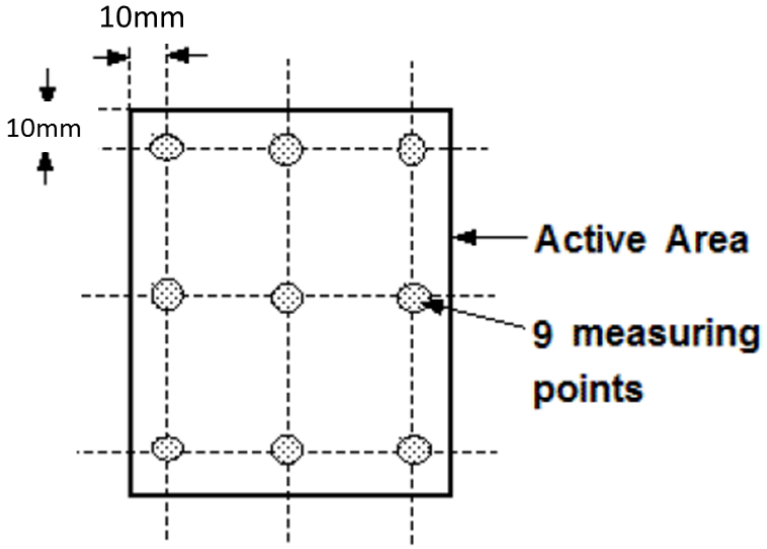
The Image retention should not be seen after 3 mins.



Note8: Color Uniformity

Total 9 measure points should set as shown in the following figures. The CIE 1967 Standards shall be used.The color difference is calculated by using following formula:

Max（△u'v'）（the max △u'v' value between two random point of 9 point）



8 Touch Sensor Specification

精度测试	参照图 1 所示的区域对 13 个圆形区域用接地的标准铜柱 φ6mm 进行触摸，测试触摸要 20 次以上，每次触摸 100ms，然后抬起 500ms。记录下 TP 报出的坐标，图 1 中区域划分成 4×4，长宽计算如图所示（W-5）/4 和（H-5）/4，青色为非边缘区（触摸点 1、2、3、4、5），蓝色为边缘区（触摸点 6、7、8、9、10、11、12、13）	记录下的坐标有无超出±1mm（非边缘区），±1.5mm（边缘区），超出结论为 NG，不超出结论为 OK。
抖动	参照图 1 所示，对每个点用接地标准铜柱 φ6mm 进行触摸，不动放置 5S，记录下坐标。	记录下坐标有无超出±1mm（非边缘区），±1.5mm（边缘区），超出结论为 NG，不超出结论为 OK。
SNR 测试	在 AMOLED R\G\B 画面切换状态下分别测试表面 9 个点（如图 1 中的 6.7.8.13.3.9.12.11.10point）的 SNR.	SNR 值应大于 30

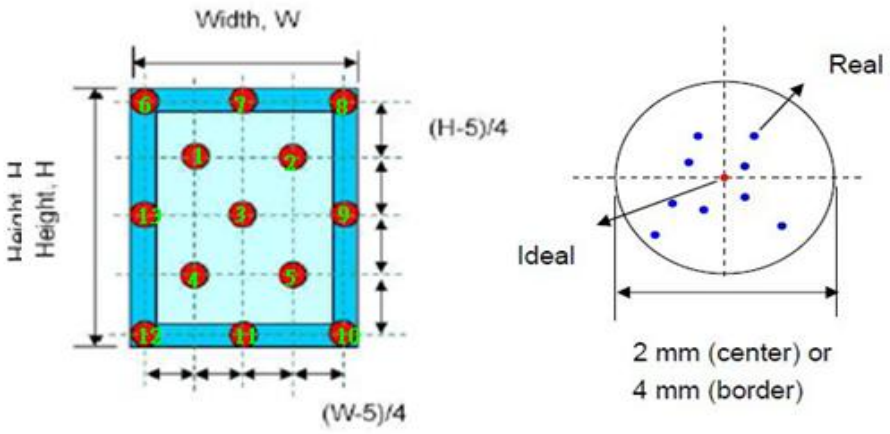


图 1、精度测试区域示意图

线性度	参照图 2 中左边三个所示的路径用接地标准铜柱 Φ6mm，分别以 5mm/s 和 50mm/s 画线，记录下坐标的偏离度，其中竖线路径从左到右分别为竖 1 到竖 5，从上到下为横 1 到横 5，从左上角到右下角为左对角，从右上角到左下角为右对角。	坐标的偏离度如图 2 所示偏离超出±1mm（非边缘区），±1.5mm（边缘区）超出结论为 NG，不超出结论为 OK。
两指最小间距	使用两个接地标准铜柱 Φ6mm,在 TP 上、中、下三部分区域逐渐接近至两点合为 1 点，然后又逐渐分离至 2 点，记录下最小的两点物理间距	最小的两点间距应小于 10mm（横向/竖向）
防水测试	TP 屏上滴上一滴 10mm 直径水滴，在 TP Development Kit 的 Points 中看是否有触摸点报出；将屏上的水擦拭干后，看是否有残留点；在屏上喷上一层水雾，在 Graph 中测试是否有触摸点报出和画线是否有断线；带着约 10mm 直径水滴画线看是否有断线和飞线	不应有误报点、断线和残留点

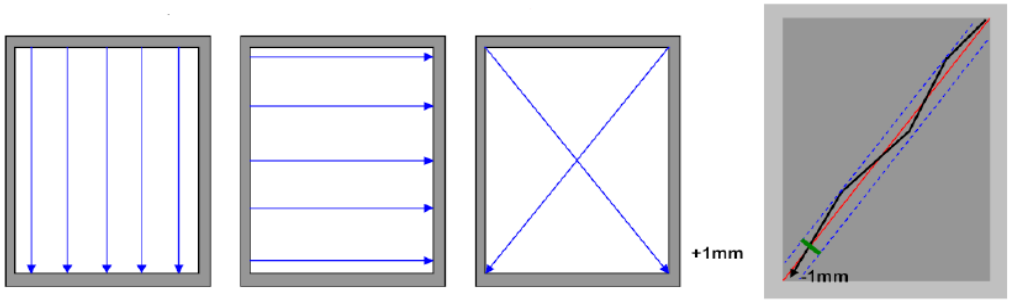


图 2、线性度路径示意图

灵敏度	参照图 3 对 TP 屏幕进行划分 Nx×Ny，Nx=W/Xmm，Ny=H/Ymm，按所示的路径用接地标准铜柱 Φ6mm 以 5mm/s 画线，记录下坐标的偏离度。(Nx、Ny>=5)	不应有断线，坐标的偏离度如超出划分所属区域则 NG，否则 OK

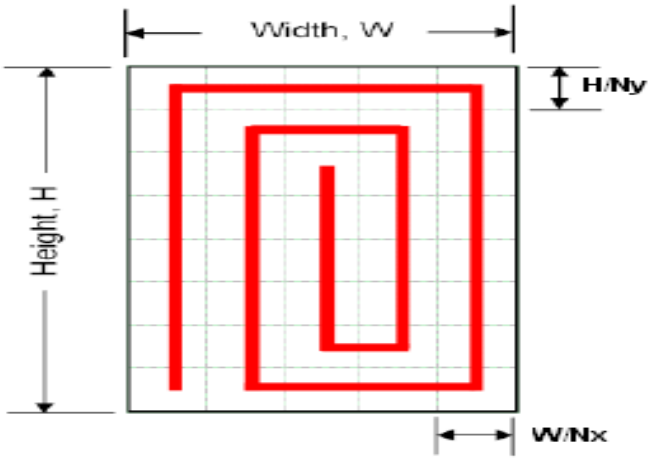


图 3、灵敏度测试路径示意图

9 Reliability

9.1 Environmental Test

No	Item	Conditions	Quantity	Remark
1	High Temperature Operation	70±2℃/ 120 hours	10 pcs	After testing - No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity test are permitted. - No function-related abnormalities.
2	Low Temperature Operation	-20±2℃/ 120 hours	10 pcs	
3	High Temperature Storage	85℃±2℃/ 240 hrs	10 pcs	
4	Low Temperature Storage	-40±2℃/ 240 hours	10 pcs	
5	High Temperature Humidity Storage	60℃/93% RH 240 hrs	10 pcs	
6	Thermal Shock	-40℃~85℃， 0.5hr, 32 cycles.	10 pcs	

9.2 Electrical Test

No	Item	Conditions	Note
1	Air Discharge (Center, 20 times)	±15kV, (Module level)	After testing - Hard defect should not happen. - If it would be recovered to normal state after resetting, it would be judged as a good state. (Class C)
2	Contact Discharge (Center, 20 times)	±8kV, (Module level)	

9.3 Mechanical Test

No	**Item**	Conditions	**Note**
1	Glass Strength Test	4PB，B10 >100MPa （stress） B10≥1500 u （strain）	
2	Drop Test	GB/T4857.18-19 Test Description For Packages (1 corner, 3 edges, 6 surfaces)	Package
3	Sinusoidal Vibration	Frequency range: 10~55Hz, Stroke:1.5mm, Sweep:10Hz~55Hz~10Hz 2hours for each direction of	Package

	Test	X.Y.Z.(6 hours for total, Package condition)	

10 Handling Precautions

10.1 When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution

10.2 Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity

10.3 Strong impact & pressure on module and packing is prohibited

10.4 Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display

10.5 Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available

10.6 Image sticking may occur if an image displays for an extended period of time

10.7 When interfered by system's overall mechanical design, an abnormal display may occur

10.8 After considering emitting energy, you should plan your design to satisfy EMI standards.

10.9 Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

11 Outline Dimension Drawing

