PHOENIX DISPLAY INTERNATIONAL, INC.

PHOENIX DISPLAY INTERNATIONAL, INC

SPECIFICATION FOR LCD MODULE

CUSTOMER	
PART NUMBER	PDIAT1195AM2
DESCRIPTION	1.19" (390x390) AMOLED
VERSION	3.0
ISSUE DATE	

COMPANY ADDRESS:
Phoenix Display International, Inc.
6150 W. Gila Springs Place Unit 2
Chandler, AZ 85226
USA
www.phoenixdisplay.com
(630) 359-5700 office
(630) 359-5701 fax

Reversion History			
Reversion. No	Date	Contents	Remark
01	2017-1-16	First Draft	
02	2017-2-22	明确 crosstalk 规格，更新亮度测试方法	
03	2017-3-8	更改 FPC 连接器,更新 pin 定义	

Contents

Contents 3
1 Scope 4
2 Features 4
2.1 Product Applications 4
2.2 Product Features 4
3 Mechanical Specifications 4
4 Maximum Rating 4
5 Electrical Specifications 5
5.1 Electrical Characteristics 5
5.2 I/O Connection and Block Diagrams 8
5.3 Recommended Operating Sequence 10
5.4 AC Characteristics（MIPI） 10
6 Electro-Optical Specification 13
7 Reliability 16
7.1 Environmental Test 16
7.2 Electrical Test 16
7.3 Mechanical Test 17
8 Handling Precautions 17
9 Outline Dimension Drawing 18

1 Scope

This Specification defines AMOLED manufactured by A-TOPS ELECTRONICS CO.,LTD In the case of any unspecified item, it may require both A-TOPS and the party desings this module into its product to work out a solution.

2 Features

2.1 Product Applications

Smart Watch

2.2 Product Features

1) Display color：16.7M (RGB x 8bits)
2) Display format：1.19”(390RGBx390)
3) Pixel arrangement：Real RGB arrangement
4) Interface：MIPI /SPI

3 Mechanical Specifications

Item	Specification	unit
Dimension outline	33.22 x 34.72 x 0.68	mm
LTPS Glass outline	33.22 x 34.72	mm
Encapsulation Glass outline	Φ30.42	mm
Number of dots	390(W) x RGB x 390(H)	dots
Active area	ϕ30.42	mm
Diagonal size	1.19	inch
Pixel pitch	78*78	μm
Glass thickness （LTPS/encapsulation glass）	0.2 / 0.2	mm
Weight	TBD	g

4 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	-	V	-
I/O voltage	VDDIO	-0.3	-	-	V	-
Operating temperature	Top	-20	-	60	℃	-
Storage temperature	Tstg	-30	-	70	℃	-

5 Electrical Specifications

5.1 Electrical Characteristics

5.1.1 Power Characteristic：

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	4.55	4.6	4.65	V	-
AMOLED power Negative	ELVSS	-2.45	-2.4	-2.35	V	Ref
Digital Power supply	VDDIO	1.65	1.8	1.95	V	Ref
Analog Power supply	VCI	2.7	2.8	2.9	V	Ref

1) Normal Mode

Power Supply: IVDDIO=1.8V VCI=2.8V

Frame Frequency: F_{frame} =60HZ @ 25degC, Brightness 300 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 350nits	IELVDD /ELVSS	-	18.5	22.5	mA	Ref
	IVCI	-	6.0	7.2	mA	Ref
	IVDDIO	-	6.0	7.2	mA	Ref
50% Pixel On 150nits	IELVDD /ELVSS	-	4.5	5.5	mA	Ref
	IVCI	-	6.6	8.0	mA	Ref
	IVDDIO	-	6.0	7.2	mA	Ref
10% Pixel On 50nits	IELVDD /ELVSS	-	0.4	0.5	mA	Ref
	IVCI	-	7.2	8.6	mA	Ref
	IVDDIO	-	6.0	7.2	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: F_{frame} =15HZ @ 25degC, Brightness 30 nits,

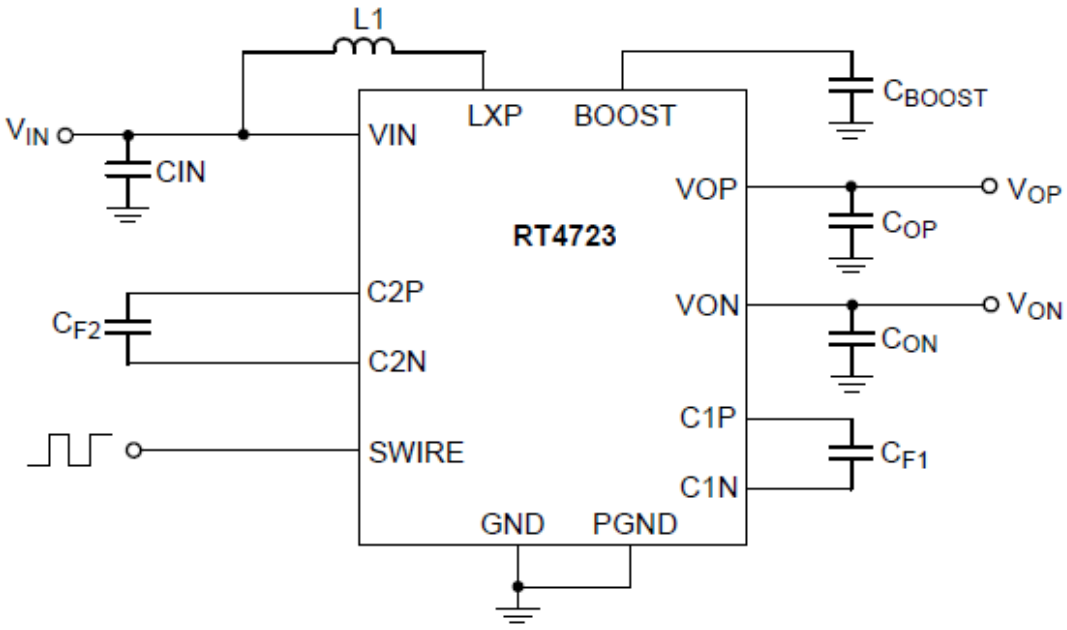
Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 30 nits	IELVDD /ELVSS	-	-	-	mA	Supplied by Driver IC
	IVCI	-	3.0	3.6	mA	Ref
	IVDDIO	-	1.0	1.2	mA	Ref

3) Deep Standby Mode

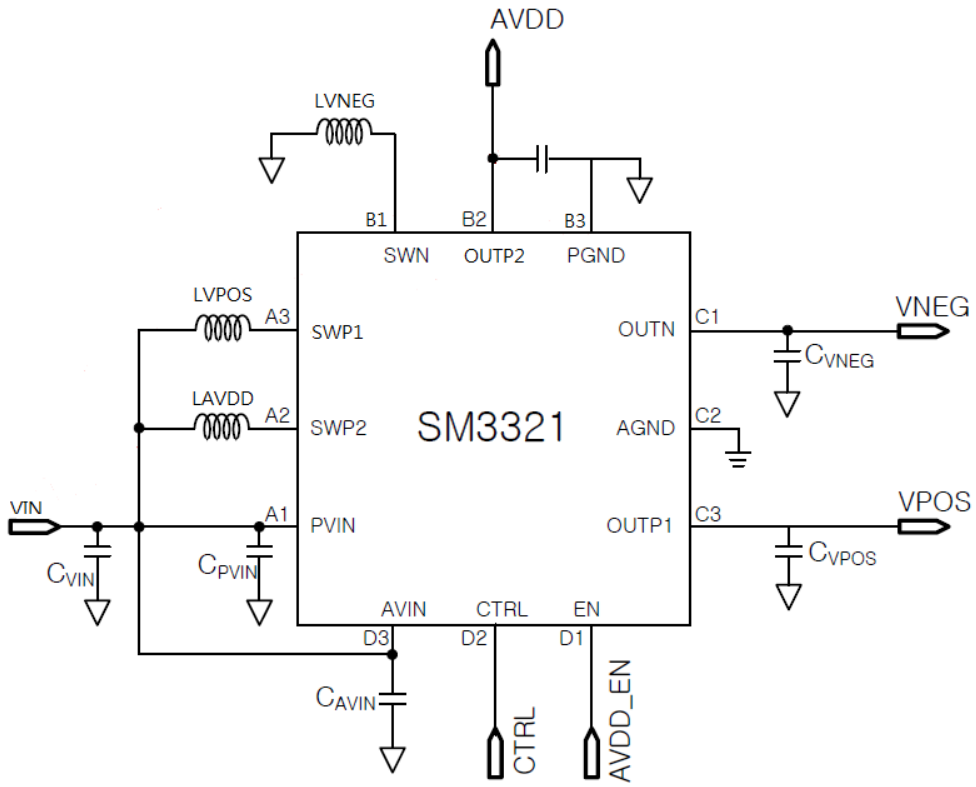
Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby	IVCI	-	-	1	uA	-
	IVDDIO	-	-	0	uA	-

5.1.2 Power supply circuit application (This is for reference only)：

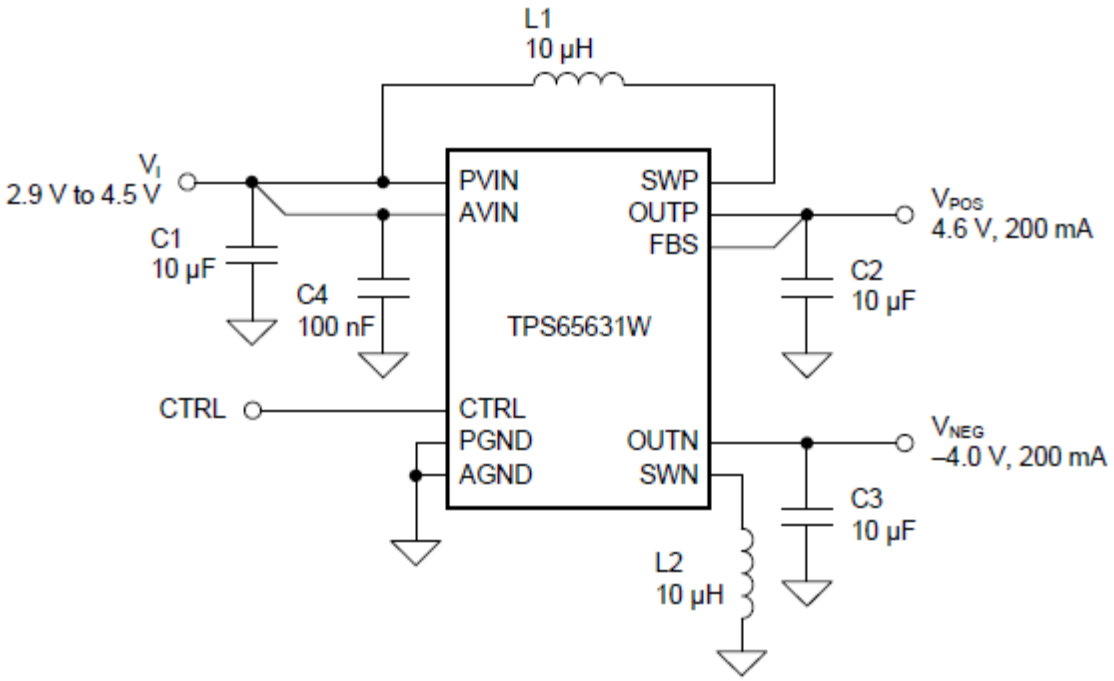
1) RT4723



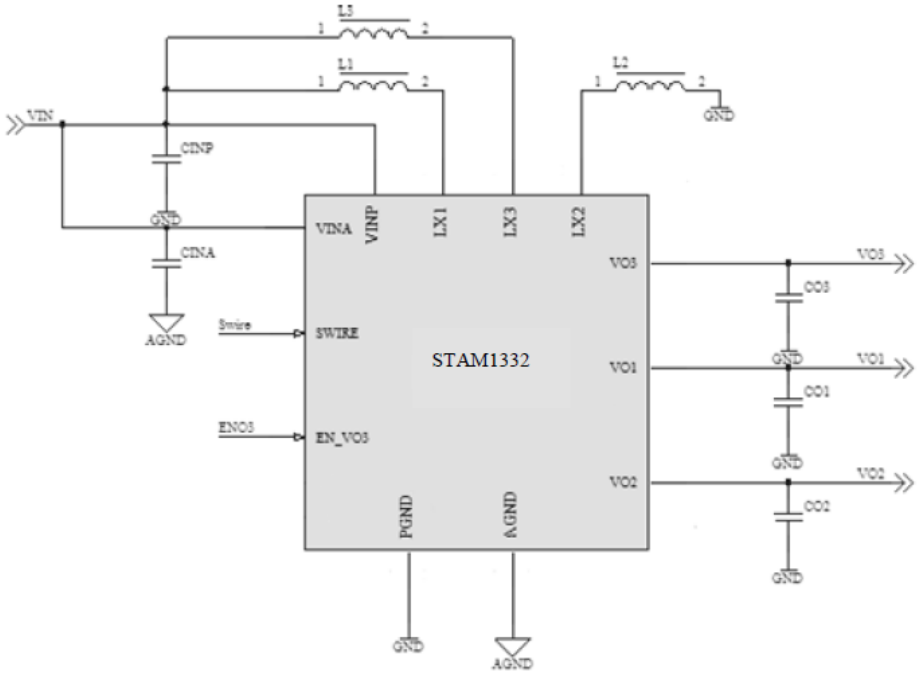
2) SM3321



3) TPS65631W


L1
10 µH
V_I
2.9 V to 4.5 V
C1
10 µF
C4
100 nF
PVIN
AVIN
SWP
OUTP
FBS
TPS65631W
V_POS
4.6 V, 200 mA
C2
10 µF
CTRL
CTRL
PGND
AGND
OUTN
SWN
V_NEG
–4.0 V, 200 mA
C3
10 µF
L2
10 µH

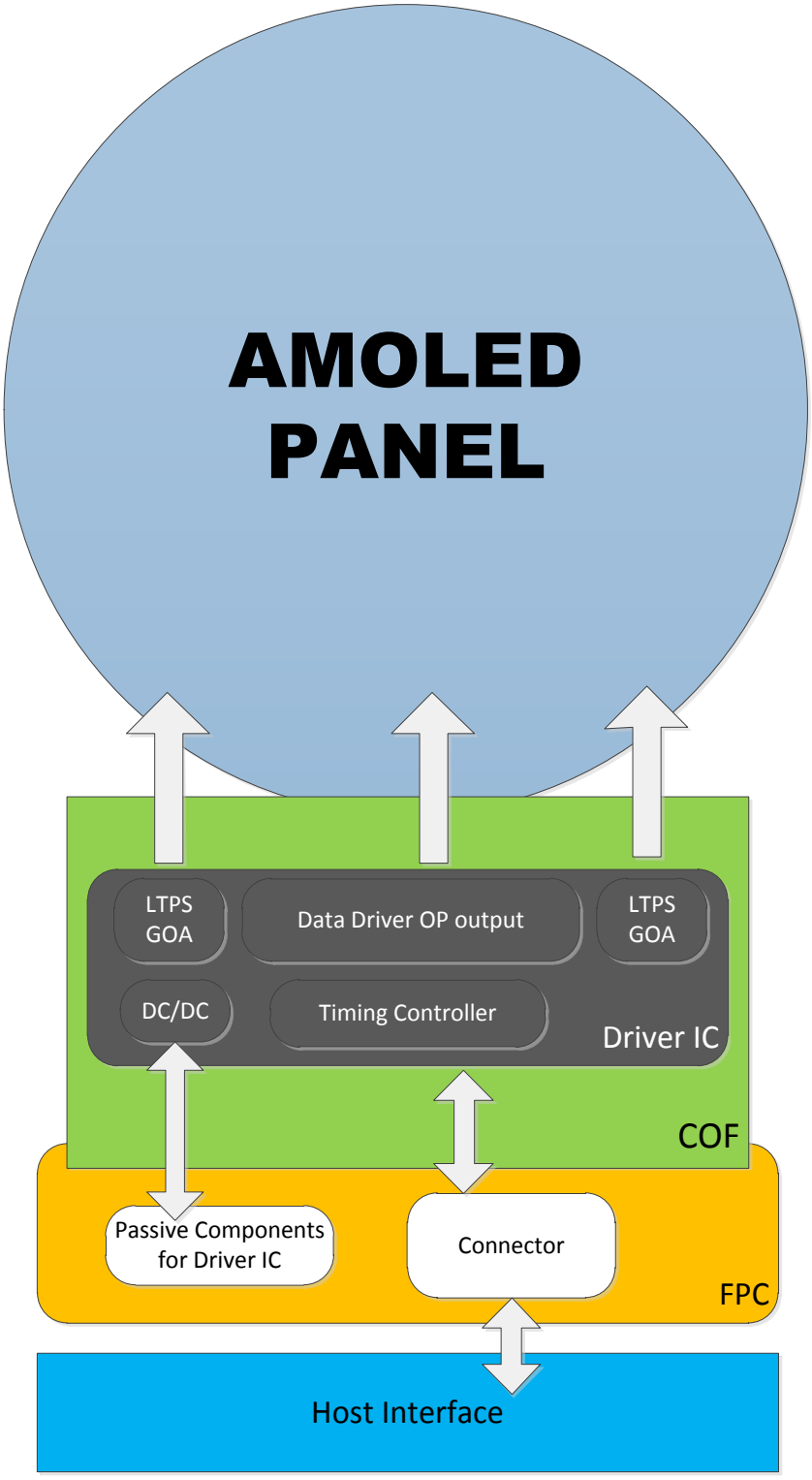
4) STAM1332


L3
L1
L2
VIN
CINP
GND
CINA
AGND
Swire
ENO3
VINA
VINP
LX1
LX3
LX2
SWIRE
EN_VO3
STAM1332
PGND
AGND
VO3
VO1
VO2
CO3
CO1
CO2
GND

5.2 I/O Connection and Block Diagrams

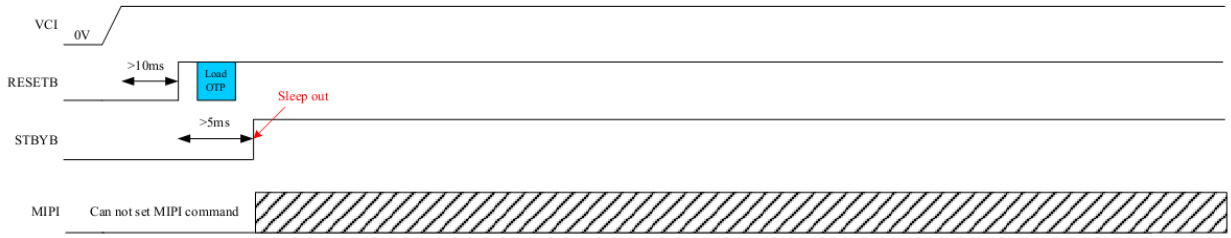
5.2.1 I/O Connection

#	Pin_name	I/O	Description
1	VPP	Power	Power supply for OTP. Leave the pin to open when not in use.
2	SWIRE	O	Swire protocol setting pin of Power IC
3	REST	I	This signal will reset the device and must be applied to properly initialize the chip. Active low.
4	GND4	Power	The power ground
5	GND	Power	The power ground
6	TE	O	Tear effect output
7	SDO	I/O	Data output pin of SPI interface
8	GND5	Power	The power ground
9	SDI	I/O	Data input pin of SPI interface
10	DSI_CLKP	I/O	MIPI DSI clock+
11	DCX	I	Data or command select pin of SPI interface
12	DSI_CLKN	I/O	MIPI DSI clock-
13	SCL	I	Clock of SPI interface
14	GND6	Power	The power ground
15	CSX	I	Chip select of SPI interface.
16	DSI_D0P	I/O	MIPI DSI data0+
17	GND2	Power	The power ground
18	DSI_D0N	I/O	MIPI DSI data0-
19	VDD1	Power	Driver IC analog supply
20	GND7	Power	The power ground
21	VDD2	Power	Driver IC analog supply
22	VDDIO	Power	Driver IC digital I/O supply
23	GND3	Power	The power ground
24	GND8	Power	The power ground
25	ELVSS1	Power	AMOLED power Negative
26	ELVDD1	Power	AMOLED power Positive
27	ELVSS2	Power	AMOLED power Negative
28	ELVDD2	Power	AMOLED power Positive
29	ELVSS3	Power	AMOLED power Negative
30	ELVDD3	Power	AMOLED power Positive

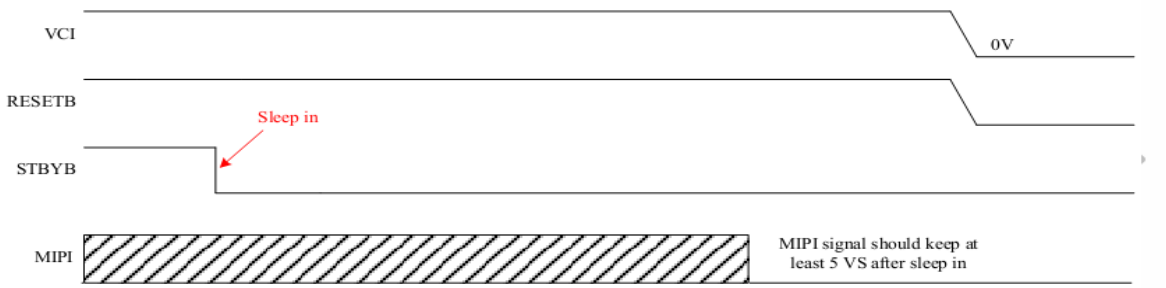

AMOLED
PANEL
LTPS
GOA
Data Driver OP output
LTPS
GOA
DC/DC
Timing Controller
Driver IC
COF
Passive Components
for Driver IC
Connector
FPC
Host Interface

5.3 Recommended Operating Sequence

5.3.1 Power on sequence

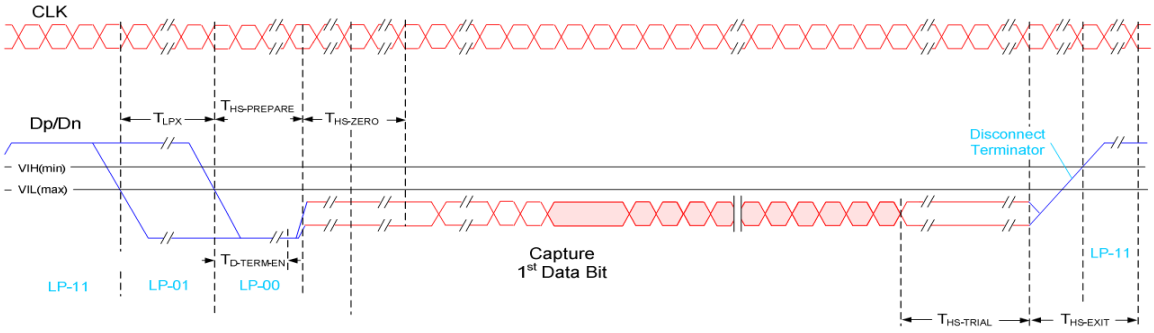


5.3.2 Power off sequence

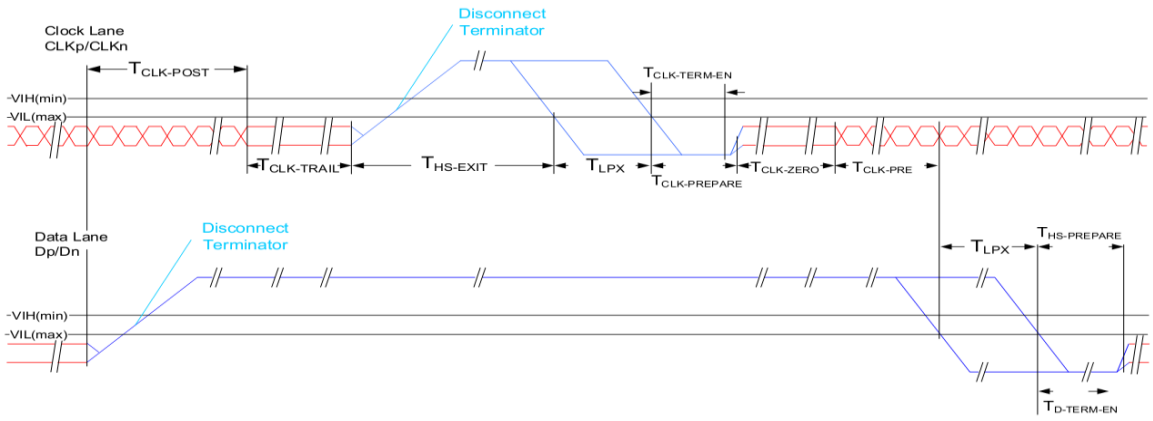


5.4 AC Characteristics（MIPI）

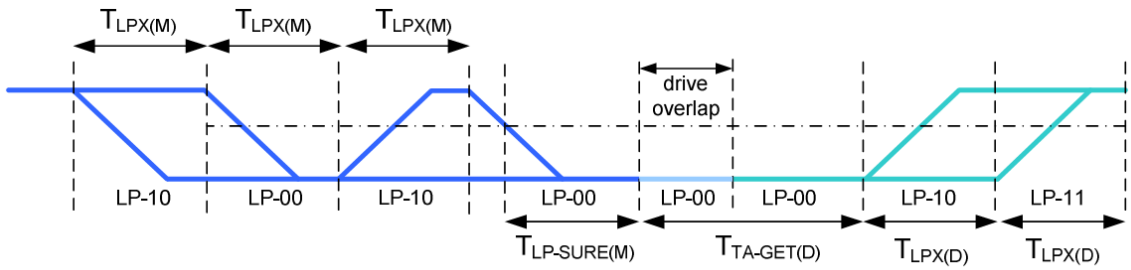
5.4.1 HS Data Transmission Burst



5.4.2 HS Clock Transmission



5.4.3 Turnaround Procedure



5.4.4 Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
TREOT	30%-85% rise time and fall time	-	-	35	ns
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
TCLK-POST*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60ns + 52*UI (For DCS)	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination,starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		38	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from	85 ns + 6*UI		145 ns + 10*UI	ns

	the beginning of THSPREPARE.				
TEOT	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	105ns+48*UI	ns
THS-EXIT(1)	time to drive LP-11 after HS burst	100	-	-	ns
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
TLPX	Length of any Low-Power state period	50	-	-	ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	ns
TTA-GET	Time to drive LP-00 by new TX	5*TLPX	5*TLPX	5*TLPX	ns
TTA-GO	Time to drive LP-00 after Turnaround Request	4*TLPX	4*TLPX	4*TLPX	ns
TTA-SURE	Time-out before new TX side starts driving	TLPX	-	2*TLPX	ns

5.4.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.

When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20℃~+70℃)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table: Reset timing



Figure: Reset timing

6 Electro-Optical Specification

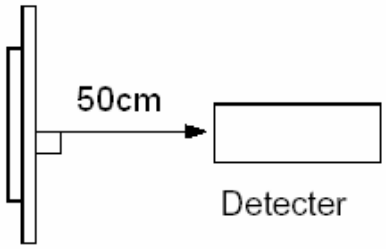
Test condition： IOVCC=1.8V , VCI=2.8V ,Ta=25℃

Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
Luminance			θ=0°	315	350	385	cd/m2	Note 1
Uniformity			Φ=0°	80		-	%	Note 2
Viewing Angle	Left	θ_L	Cr≥200	80	85	-	Deg.	Note 3
	Right	θ_R		80	85	-		
	Top	ψ_T		80	85	-		
	Bottom	ψ_B		80	85	-		
Contrast Ratio		CR	θ=0°	5000	10000	-	-	Note 4
Response Time		Tr+Tf	Φ=0°	-	2	4	ms	Note 5
Color Coordinate of CIE1931	Red	X	θ=0° Φ=0°	0.635	0.665	0.695	-	-
		Y		0.304	0.334	0.364		
	Green	X		0.17	0.22	0.27		
		Y		0.67	0.72	0.77		
	Blue	X		0.10	0.14	0.18		
		Y		0.003	0.04	0.08		
	White	X		0.28	0.30	0.32		
		Y		0.29	0.31	0.33		
NTSC Ratio		NTSC	CIE1931	85	100	-	%	-
Flicker		-	-	-	-30	-	dB	-
Gamma		-	-	1.9	2.2	2.5		Note 6
Crosstalk		Δ CT	-	-	-	1.1		Note 7

Note 1: Luminance measurement

The test condition is measured on the surface of AMOLED module at 25℃.

- Measurement equipment CS2000 or similar equipment (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measuring Pattern: Full white



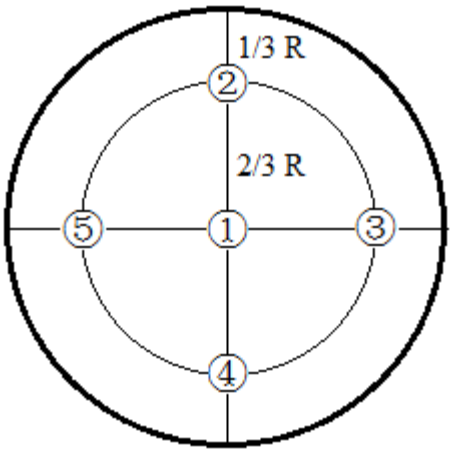
Note 2: Uniformity

The luminance uniformity is calculated by using following formula:

$$\Delta Bp = Bp\ (Min.) / Bp\ (Max.) \times 100\ (\%)$$

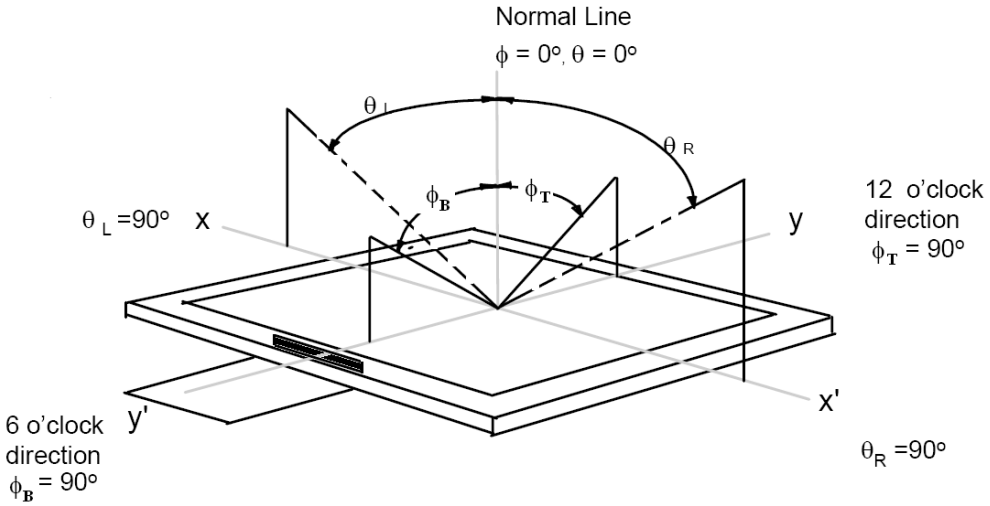
Bp (Max.) = Maximum brightness in 5 measured spots

Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: **The definition of Viewing Angle**

Refer to the graph below marked by ϑ and Φ



Note 4: **The definition of Contrast Ratio**:

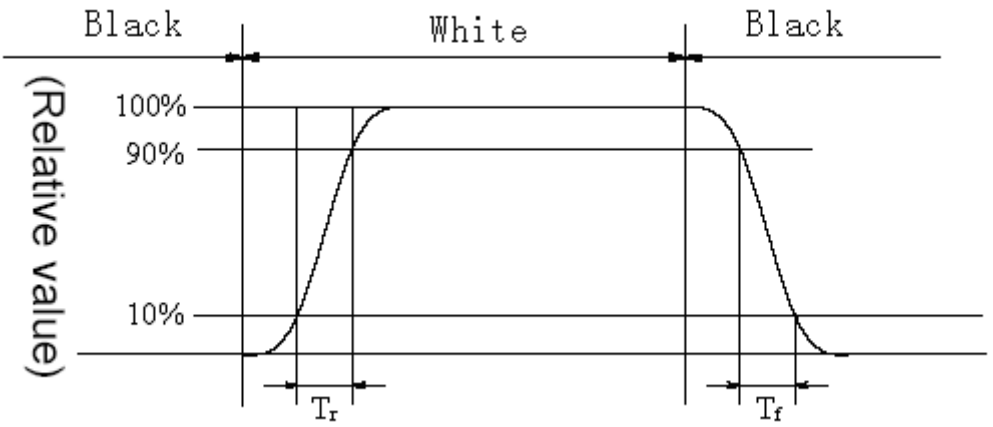
Luminance When AMOLED is at "White" state

Contrast Ratio (CR) = ——————————————————

Luminance When AMOLED is at “Black” state

Note 5: **Definition of Response time.**

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (Voltage falling time) and from “white” to “black” (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 6: Gamma curve

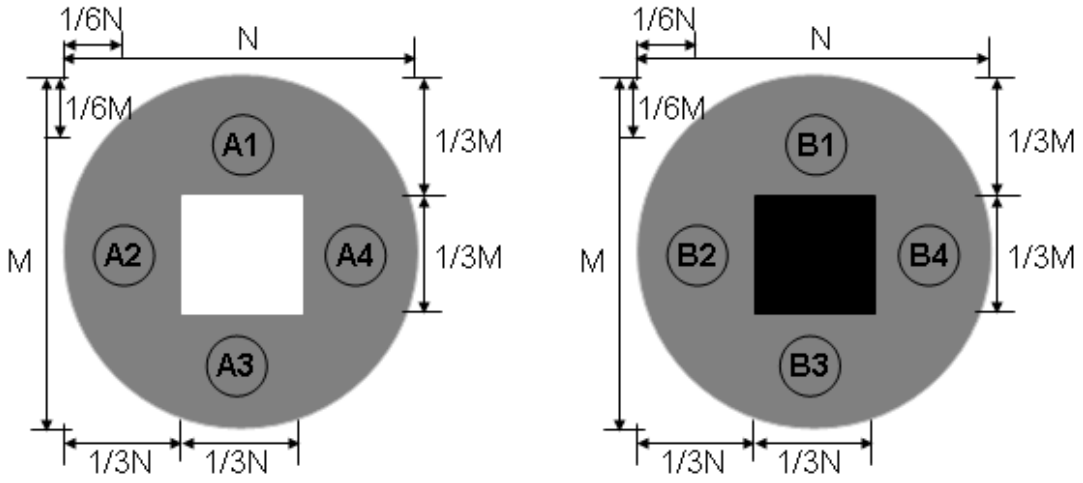
The whole curve’s tolerance must control within +/-0.3, test the gray scale below:
8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239,

Note 7: **Crosstalk**

- There should be no visible cross-talk in normal direction of the display when the two ”Cross-talk Test Patterns ” below are loaded.
- Measurement equipment: CS2000 or similar equipments
- The point should be marked is, the background of Cross-talk Test Pattern-“gray “ are defined as middle gray scale . For example, RGB 24bit “gray” defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- Δ Bpn = Bpn (gray) / Bpn (white)
- Which n means the dot No. In the Cross-talk Test Pattern ;
- Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern;
- Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;
- Δ Bp (Max.) = Maximum value in Δ Bp1~Δ Bp4.
- Δ Bp (Min.) = Minimum value in Δ Bp1~Δ Bp4.
- Δ CT=Δ Bp (Max.)/ Δ Bp(Min.).
- Δ CT must be less than 1.10



Cross-talk Test Pattern

7 Reliability

7.1 Environmental Test

Item	Main spec	No. of failures / No. of examinations	Note
High Temperature Operation	70℃/ 128hours	0/5	
Low Temperature Operation	-20℃/ 128hours	0/5	
High Temperature Storage	80℃/ 128hours	0/5	
Low Temperature Storage	-30℃/ 128hours	0/5	
High Temperature Humidity Operation	60℃/90%RH 128hours	0/5	
Thermal Shock	-40℃~80℃ 0.5hr, 30 cycles	0/5	

7.2 Electrical Test

Item	Main spec	Note
Air Discharge	±2kV , 150pF/330Ω (Module level)	5Points, Each 2times. No degradation of OLED performance after this test.
Contact Discharge	±2kV, 150pF/330Ω (Module level)	

7.3 Mechanical Test

Item	Main spec	Note
Drop Test	Drop the packing from 75cm height, 3 times for 6-faces, 3-edges and 1-corner	Package
Vibration-proof test	2g, f=10->55->10Hz apply in each of X, Y, and Z direction for 30 min	Package

8 Handling Precautions

8.1 When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution

8.2 Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity

8.3 Strong impact & pressure on module and packing is prohibited

8.4 Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display

8.5 Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available

8.6 Image sticking may occur if an image displays for an extended period of time

8.7 When interfered by system's overall mechanical design, an abnormal display may occur

8.8 After considering emitting energy, you should plan your design to satisfy EMI standards.

8.9 Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

9 Outline Dimension Drawing

