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ILI6123H

1200-Output Channel
TFT LCD Source Driver with TCON

Specification
Preliminary

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1. Introduction

ILI6123H is a 1200-channel output source driver with TTL interface timing controller (TCON). ILI6123H supports cascade mode to extend source channel to achieve more various resolution applications.

The interface follows digital 24-bit parallel RGB input format. The TCON generates the 800x480, 800x600, 640x480, 320x240 resolutions and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales. Operating parameters can be set via pin control for all control features. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation.

ILI6123H can be configured as dual-gate operation mode for reducing FPC amount and saving the cost. With wide range of supply voltages and many pin control features make this chip mode suitable for various applications.

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2. Features

◆ TCON

- Supports display resolution 800x480, 800x600, 640x480 and 320x240
- Supports digital 24-bit parallel RGB input mode
- Supports to configure CABC block via 3-line SPI mode
- Source output with 8-bit resolution for 256 gray scales (2-bit dithering)
- Supports dual-gate operation mode
- Supports Stripe CF configuration
- Maximum Operation frequency: 50 MHz
- Provide flip and mirror scan mode by pin control
- Supports stand-by mode for saving power consumption
- Logic operation Voltage Level 3.0V to 3.6V
- Support LED Backlight Enable Control Signal With CABC Function(CABC_PWM)
- Support cascade & Dual-Gate function
- Hardware Pin Control CABC Mode Selection

◆ Source Driver

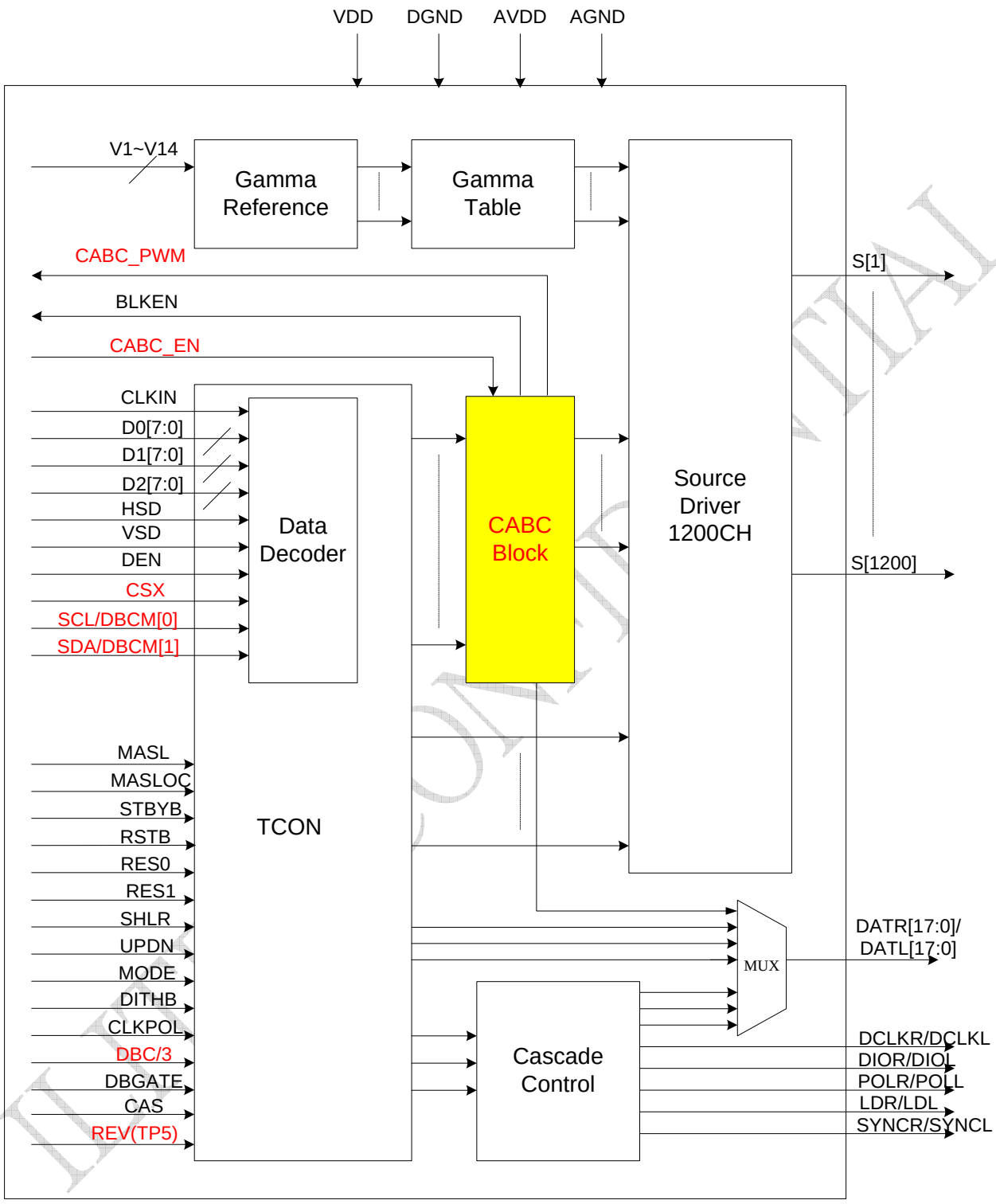
- 1200/960 channels output source driver for TFT LCD panel
- Embedded custom-made Gamma table for special custom request
- Supports external V1~V14 and V1~V10 pad for Gamma adjustment
- Output dynamic range : 0.1 ~ AVDD-0.1V
- Voltage deviation of outputs: ±20mV
- Power for source driver voltage (AVDD) : 6.5V ~ 13.5V

◆ Others

- COG package
- Supports CABC (Content Adaptive Brightness Control) function

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3. Block Diagram

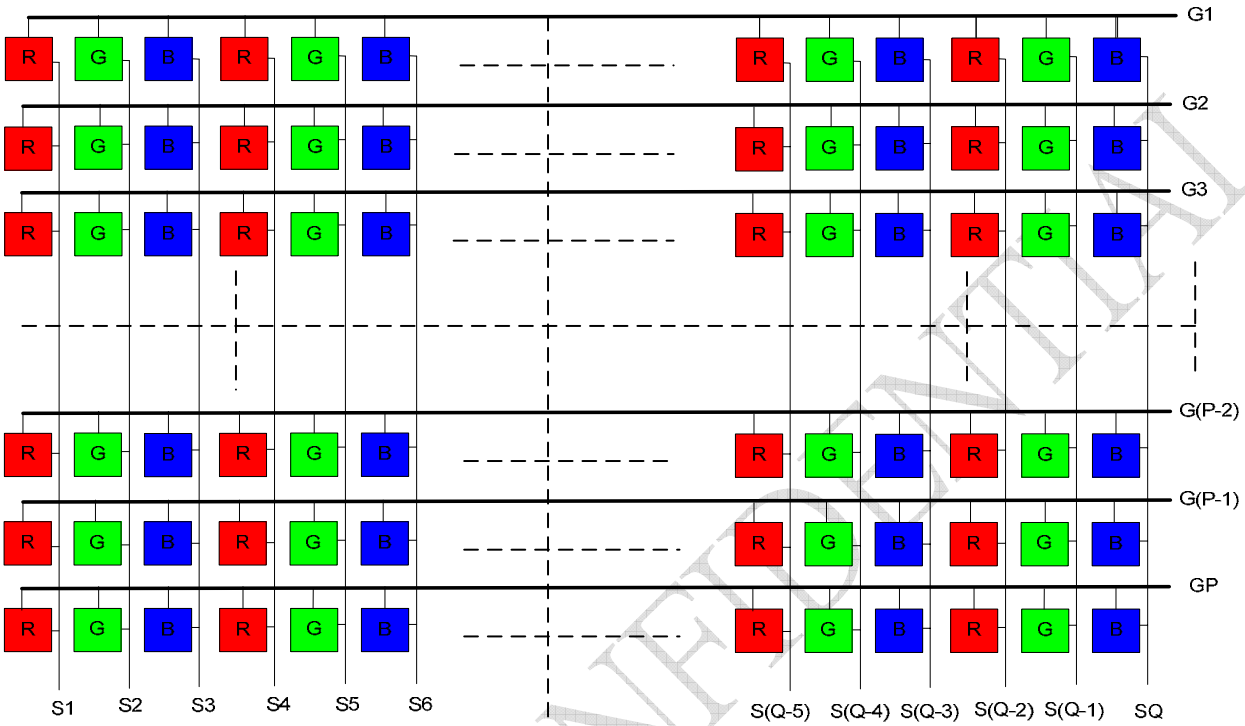


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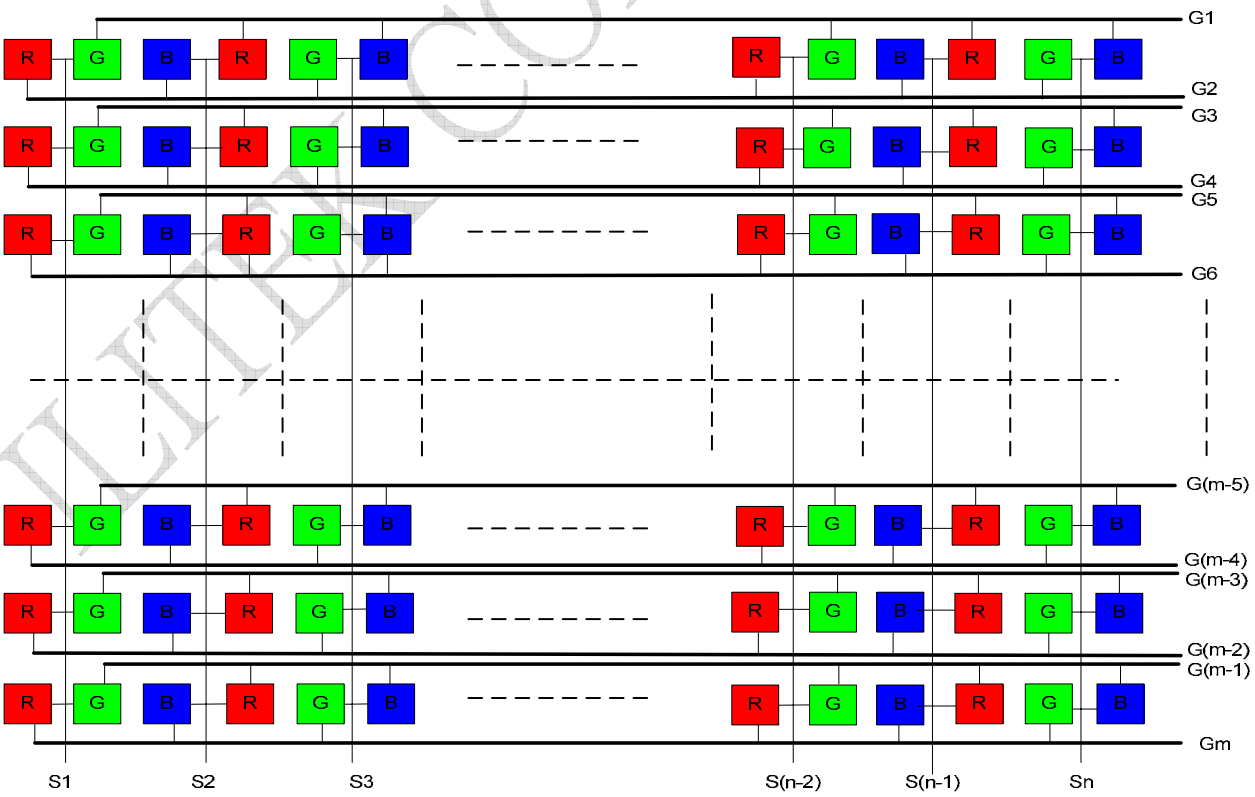
4. Application Diagram

Color Filter Application Type

A. Cascade Application:

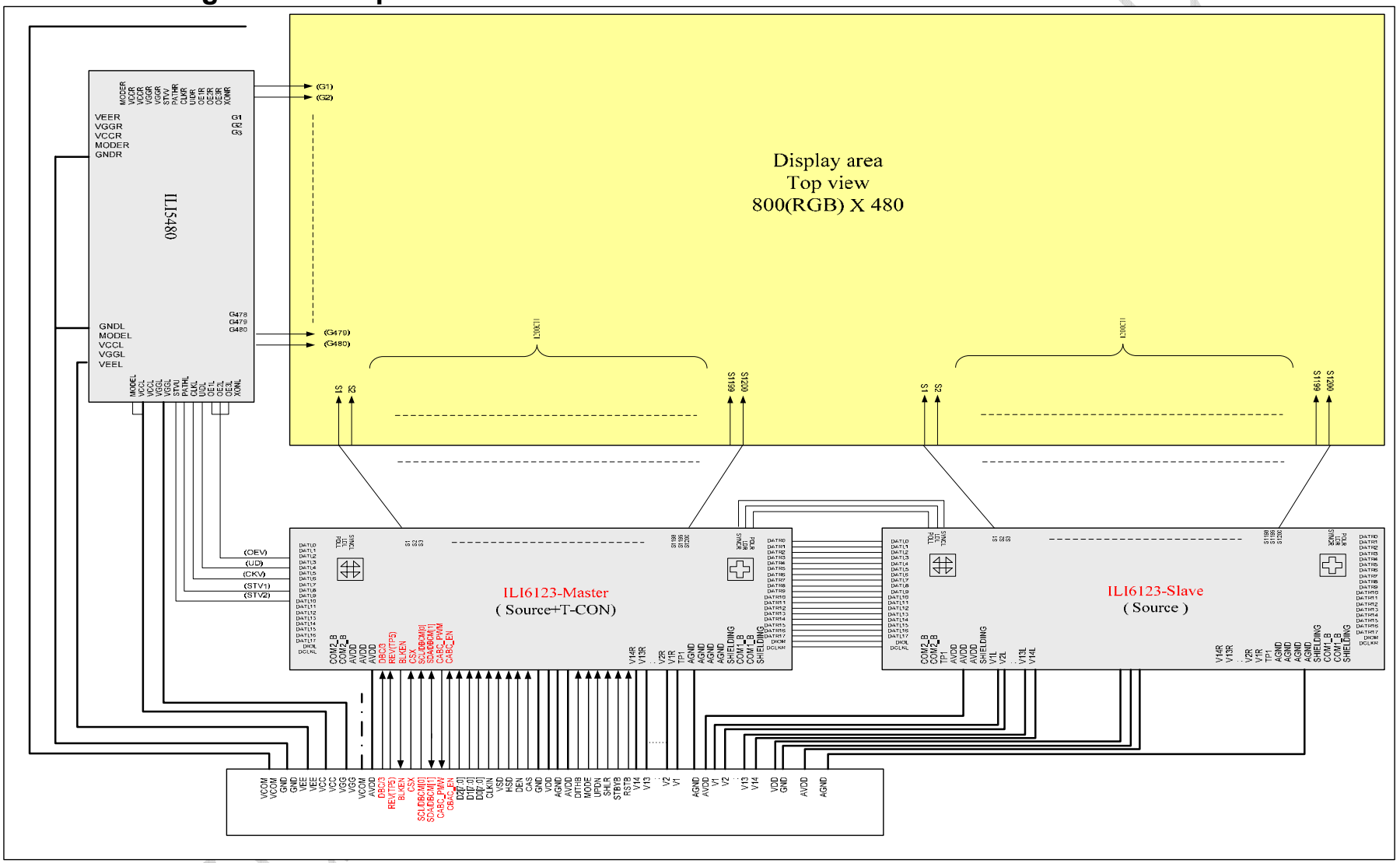


B. Dual–Gate Application:

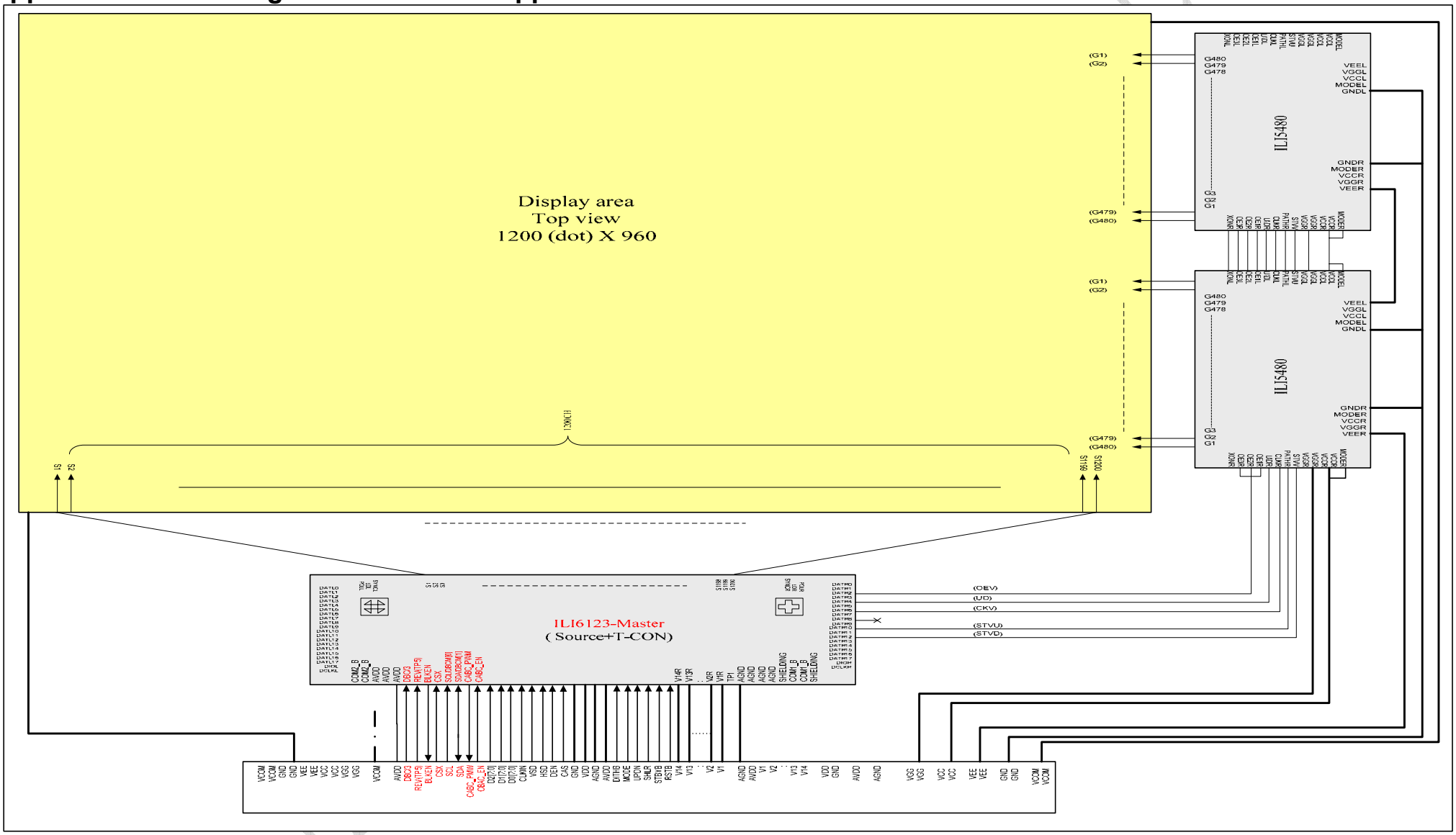


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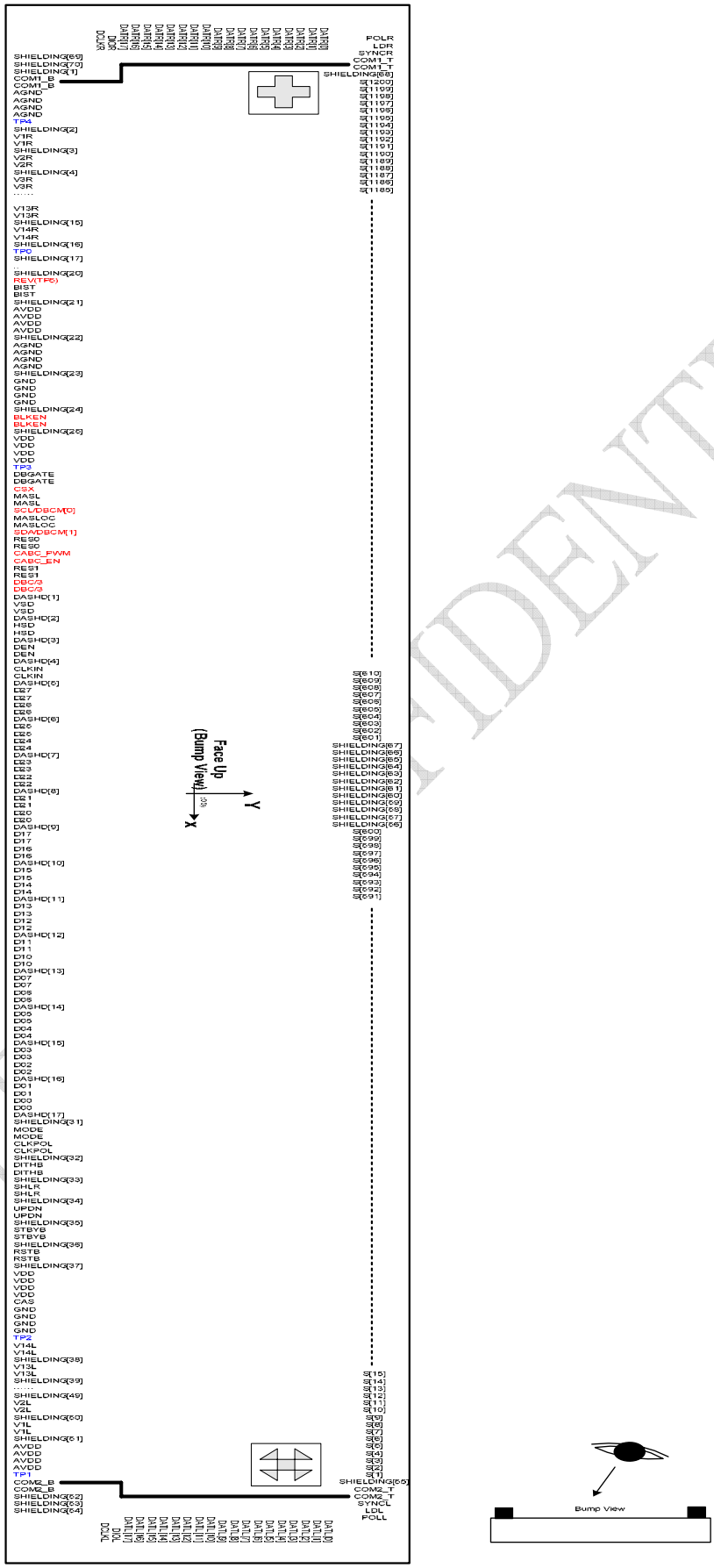
Application Block Diagram – 2 Chip Cascade



Application Block Diagram – Dual Gate Application



5. Pad Sequence (Bump Side)



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6. Pin Descriptions

Pin Name	I/O	Descriptions
CLKIN	I	Clock for input data. Data latched at rising/falling edge of this signal. Default is falling edge.
D0[7:0] D1[7:0] D2[7:0]	I	Digital data input. Dx0 is LSB and Dx7 is MSB. D0[7:0] = R[7:0] data; D1[7:0] = G[7:0] data; D2[7:0]=B[7:0] data When 18-bit RGB interface (disable dithering function), please use Dx[7:2] as 6-bit input and connect Dx[1:0] to DGND.
HSD	I	Horizontal sync input in digital parallel RGB. Negative polarity.
VSD	I	Vertical sync input in digital parallel RGB. Negative polarity.
DEN	I	Input data enable control. When DE mode, active High to enable data input. **Note: Normal pull low**
MODE	I	DE / SYNC mode select. MODE="L", for entering SYNC mode. MODE="H", for entering DE mode. **Note: Normal pull high**
CSX	I	A chip select signal. CSX="L", the chip is selected and accessible CSX="H", the chip is not selected and not accessible ***Fix to the VDD level when not in use.*** **Note: Normal pull high**
SCL/DBCM[0]	I	Multi-Function Selection: When DBC/3="H", this pin act as 3-wire "SCL" pin. Serial clock input. This pin is used for CABC command set only. When DBC/3="L", this pin act as DBC mode select pin LSB (DBCM[0]) **Note: Normal pull high and *Fix to the VDD level when not in use.***
SDA/DBCM[1]	I/O	Multi-Function Selection: When DBC/3="H", this pin act as 3-wire "SDA" pin. Serial data input / output. This pin is used for CABC command set only. When DBC/3="L", this pin act as DBC mode select pin MSB (DBCM[1]) **Note: Normal pull high and *Fix to the VDD level when not in use.***
RSTB	I	Hardware global reset. Low active. **Note: Normal pull high**
RES[1:0]	I	Display resolution selection. RES[1:0]="00", for 800(RGB)x480 display resolution. RES[1:0]="01", for 800(RGB)x600 display resolution. RES[1:0]="10", for 640(RGB)x480 display resolution. RES[1:0]="11", for 320(RGB)x240 display resolution. **Note: Normal pull "LL"**
DITHB	I	Dithering function enable control. DITHB="L", to enable internal dithering function. DITHB="H", to disable internal dithering function. **Note: Normal pull high**
CLKPOL	I	Input clock edge selection. CLKPOL="L", latch data at CLKIN falling edge. CLKPOL="H", latch data at CLKIN rising edge. **Note: Normal pull low**
DBC/3	I	DBC/3-wire selection pin DBC/3="L", Select DBC hardware control function. DBC/3="H", Select 3-wire SPI interface function. (Default) **Note: Normal pull high**
V1 ~ V14	I/O	Gamma correction reference voltage. These input voltages must be offered by

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Pin Name	I/O	Descriptions
		user. The relationship between V1~V14 must be : AGND<V14<V12<V11<V10<V8<V7<V5<V4<V3<V1<AVDD **V2, V6, V9 and V13 are disabled! Please make sure AVDD-1>V1**
MASL	I	Master and Slave Mode selection. Normally pull high. MASL="H", for master mode. MASL="L", for slave mode. Only the master chip will issue the gate and cascade control signal. **Note: Normal pull high**
MASLOC	I	Master location definition pin. Normally pull low MASLOC="H", Master location is on the left side (panel top view). MASLOC="L", Master location is on the right side (panel top view).**(Default)** **Note: Normal pull low**
DBGATE	I	Dual gate function enables control. Normally pull low. DBGATE="H", enable dual gate function. DBGATE="L", disable dual gate function. **(Default)** **Note: cascade function ; Note: Normal pull low**
STBYB	I	Standby mode control. STBYB="L", enter standby mode for power saving. Timing controller and source driver will turn off, all outputs are Hi-Z. STBYB="H", normal operation. **Note: Normal pull high**
SHLR	I	Source shift direction control. SHLR="L", shift direction is "S1200 → S1199→ 1198 → • • • S3→ → S2 → S1" SHLR="H", shift direction is "S1 → S2→ S3 → • • • → S1198 → S1199 → S1200". **Note: Normal pull high**
UPDN	I	Gate scan direction control UPDN="L", STV2 outputs the vertical start pulse and UD pin outputs "L" to Gate driver. UPDN="H", STV1 outputs the vertical start pulse and UD pin outputs "H" to Gate driver. **Note: Normal pull low**
BIST	I	Normal operation / BIST pattern select. BIST="L", Normal operation BIST="H", BIST (DCLK input is not needed) **Note: Normal pull low**
CABC_EN	I	CABC Function Enable Control. CABC_EN="H", CABC_PWM pin is used to be backlight control signal for external backlight controller. (CABC Function Disable) CABC_EN="L", ILI6123 will refer the gray scale content of display image to output a PWM frequency to LED driver via CABC_PWM pin. (CABC Function Enable) **Note: Normal pull "H"**
BLKEN	O	The backlight control signal for external backlight controller. BLKEN="L", turn off the external backlight controller. BLKEN="H", turn on the external backlight controller. ***Note: Keep Open when not in use.***
CABC_PWM	O	The backlight control signal for external backlight controller. CABC_PWM ="L", turn off the external backlight controller. CABC_PWM ="H", turn on the external backlight controller. Note: Refer to the Power ON/OFF sequence for the detail information when CABC_EN is set to "L". ***Note: Keep Open when not in use.***
CAS	I	Cascade function select. CAS="H" enable cascade function. CAS="L" disable cascade function. **Note: Normal pull high**
REV(TP5)	I	Data input code Inverted control Pin. REV="L"; Input Data code Inverted Function was disable. REV="H"; Input Data code Inverted Function was enable.

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Pin Name	I/O	Descriptions
		Input Code / REV=L / REV=H 00H / 00H / 3FH 0AH / 0AH / 35H 3FH / 3FH / 00H Note: Normal pull "L".
DATR[17:0]	I/O	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKR	I/O	Master and slave cascade control signal.
DIOR	I/O	Master and slave cascade control signal.
POLR	I/O	Master and slave cascade control signal.
LDR	I/O	Master and slave cascade control signal.
SYNCR	I/O	Master and slave cascade control signal.
DATL[17:0]	I/O	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKL	I/O	Master and slave cascade control signal.
DIOL	I/O	Master and slave cascade control signal.
POLL	I/O	Master and slave cascade control signal.
LDL	I/O	Master and slave cascade control signal.
SYNCL	I/O	Master and slave cascade control signal.
AVDD	P	Power supply for analog block.
AGND	P	Ground level for analog block.
VDD	P	Power supply for digital block.
DGND	P	Ground level for digital block.
S1 ~ S1200	O	Source driver output signals.
ALIGN	M	For assembly alignment.
COM1_B COM2_B	S	Internal link together between input side and out side
COM1_T COM2_T	S	Internal link together between input side and out side
TP0 ~ TP4	T	Test pin for ILITEK only Float those pins for normal operation.
SHIELDING	--	IC shielding pads. Those pins are internally connected to AGND level.
DASHD	--	Data bus shielding pad. Those pins are internally connected to DGND level.
DUMMY	--	Dummy pads. Please leave it open when not in use.

Note:
I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, C: Capacitor pin.

Pass line description

Pass Line No:	Pad Name	
1	COM1_B	COM1_T
2	COM2_B	COM2_T

DBC/3 for CABC Function Control description:

Pin Name	DBC/3	
	H (Default)	L
CSX SCL SDA	Enable SPI Function	Disable SPI Function, CABC Function mode by Hardware Pin control

SDA/DBCM[1]	SCL/DBCM[0]	Mode
0	0	User interface image
0	1	CABC OFF
1	0	Moving image
1	1	Still picture
Remark: Default Still Mode		

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Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value(Ω)
VDD	<25	SHLR	<1K
AVDD	<5	UPDN	<1K
GND	<25	BIST	<1K
AGND	<5	CAS	<1K
V1~V14	<20	DATR[17:0]	< 200 & 20 pf
D00~D07	<200	DCLKR	< 200 & 20 pf
D10~D17	<200	DIOR	< 200 & 20 pf
D20~D27	<200	POLR	< 200 & 20 pf
DEN	<200	LDR	< 200 & 20 pf
MODE	<1K	SYNCR	< 200 & 20 pf
RES[1:0]	<1K	DATRL17:0]	< 200 & 20 pf
DITHB	<1K	DCLKL	< 200 & 20 pf
CLKPOL	<1K	DIOL	< 200 & 20 pf
BLKEN	<1K	POLL	< 200 & 20 pf
DBC/3	<1K	LDL	< 200 & 20 pf
DBGATE	<1K	CASCADE V1~V14	<50
RSTB	<1K	CLKIN	<50
MASL	<1K	HSD	<200
MASLOC	<1K	VSD	<200
CSX	<1K	CABC_PWM	<1K
SCL/DBCM[0]	<1K	SDA/DBCM[1]	<1K

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7. DATR[17:0] / DATL[17:0] pin mapping table

DATR [17:0]	DBGATE = "0" MASL = "1" MASLOC = "0" CAS = "1" (Default)	DBGATE = "0" MASL = "1" MASLOC = "1" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "0" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "1" CAS = "1"	DBGATE = "1" MASL = "1" MASLOC = "X" CAS = "0"	DBGATE = "0" MASL = "1" MASLOC = "X" RES[1:0]= "1X" CAS = "0"
Description	Master for cascade. Master locate on panel right side	Master for cascade. Master locate on panel left side	Slave for cascade. Master locate on panel right side	Slave for cascade. Master locate on panel left side	Dual Gate Mode	Single Source Mode
DATR0	X	DAT0	DAT0	X	X	X
DATR1	X	DAT1	DAT1	X	X	X
DATR2	OEV	DAT2	DAT2	X	OEV	OEV
DATR3	X	DAT3	DAT3	X	X	X
DATR4	UD	DAT4	DAT4	X	UD	UD
DATR5	X	DAT5	DAT5	X	X	X
DATR6	CKV	DAT6	DAT6	X	CKV	CKV
DATR7	X	DAT7	DAT7	X	X	X
DATR8	STV1	DAT8	DAT8	X	STV1	STV1
DATR9	X	DAT9	DAT9	X	X	X
DATR10	STV2	DAT10	DAT10	X	STV2	STV2
DATR11	X	DAT11	DAT11	X	X	X
DATR12	STV1	DAT12	DAT12	X	STV1	STV1
DATR13	X	DAT13	DAT13	X	X	X
DATR14	X	DAT14	DAT14	X	X	X
DATR15	X	DAT15	DAT15	X	X	X
DATR16	STBN	DAT16	DAT16	X	STBN	STBN
DATR17	X	DAT17	DAT17	X	X	X
DCLKR	X	DCLK	DCLK	X	X	X
DIOR	X	DIO	DIO	X	X	X
LDR	X	LD	LD	X	X	X
SYNCR	X	SYNC	SYNC	X	X	X

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DATL [17:0]	DBGATE = “0” MASL = “1” MASLOC = “0” CAS = “1” (Default)	DBGATE = “0” MASL = “1” MASLOC = “1” CAS = “1”	DBGATE = “0” MASL = “0” MASLOC = “0” CAS = “1”	DBGATE = “0” MASL = “0” MASLOC = “1” CAS = “1”	DBGATE = “1” MASL = “1” MASLOC = D “X” CAS = “0”	DBGATE = “0” MASL = “1” MASLOC = “X” RES[1:0]= “1X” CAS = “0”
Description	Master for cascade. Master locate on panel right side	Master for cascade. Master locate on panel left side	Slave for cascade. Master locate on panel right side	Slave for cascade. Master locate on panel left side	Dual Gate Mode	Single Source Mode
DATL0	DAT0	X	X	DAT0	X	X
DATL1	DAT1	X	X	DAT1	X	X
DATL2	DAT2	OEV	X	DAT2	OEV	OEV
DATL3	DAT3	X	X	DAT3	X	X
DATL4	DAT4	UD	X	DAT4	UD	UD
DATL5	DAT5	X	X	DAT5	X	X
DATL6	DAT6	CKV	X	DAT6	CKV	CKV
DATL7	DAT7	X	X	DAT7	X	X
DATL8	DAT8	STV1	X	DAT8	STV1	STV1
DATL9	DAT9	X	X	DAT9	X	X
DATL10	DAT10	STV2	X	DAT10	STV2	STV2
DATL11	DAT11	X	X	DAT11	X	X
DATL12	DAT12	STV1	X	DAT12	STV1	STV1
DATL13	DAT13	X	X	DAT13	X	X
DATL14	DAT14	X	X	DAT14	X	X
DATL15	DAT15	X	X	DAT15	X	X
DATL16	DAT16	STBN	X	DAT16	STBN	STBN
DATL17	DAT17	X	X	DAT17	X	X
DCLKL	DCLK	X	X	DCLK	X	X
DIOL	DIO	X	X	DIO	X	X
LDL	LD	X	X	LD	X	X
SYNCL	SYNC	X	X	SYNC	X	X

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8. Relationship between input data and output channels

1. DBGATE="0", CFSEL="1": Dual Gate Disable and Color Filter with Stripe Type.
   (1) SHILR="1", right shift (Default)

Output	S1	S2	S3	---	S1198	S1199	S1200
Order	First data			→	Last data		
Odd Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

   (2) SHILR="0", left shift

Output	S1	S2	S3	---	S1198	S1199	S1200
Order	Last data			←	First data		
Odd Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

2. DBGATE="1", CFSEL="1": Dual Gate Enable and Color Filter with Stripe Type.
   (1) SHILR="1", right shift (Default)

Output	S1	S2	S3	---	S1198	S1199	S1200
Order	First data			→	Last data		
G1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
G2	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
G(m-1)	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Gm	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10

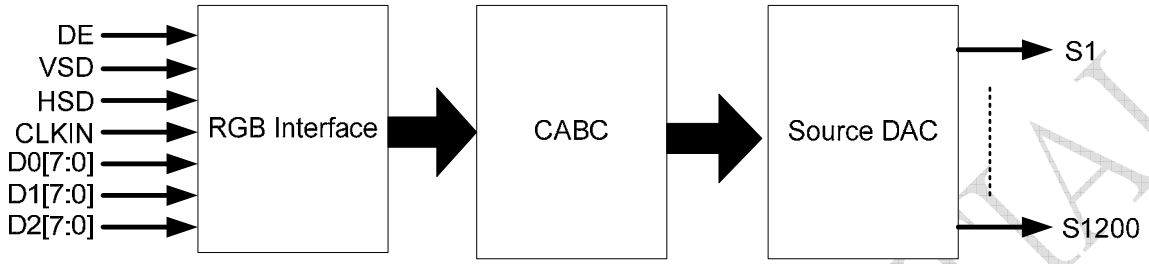
   (2) SHILR="0", Left shift

Output	S1	S2	S3	---	S1198	S1199	S1200
Order	Last data			←	First data		
G1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
G2	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
G(m-1)	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Gm	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10

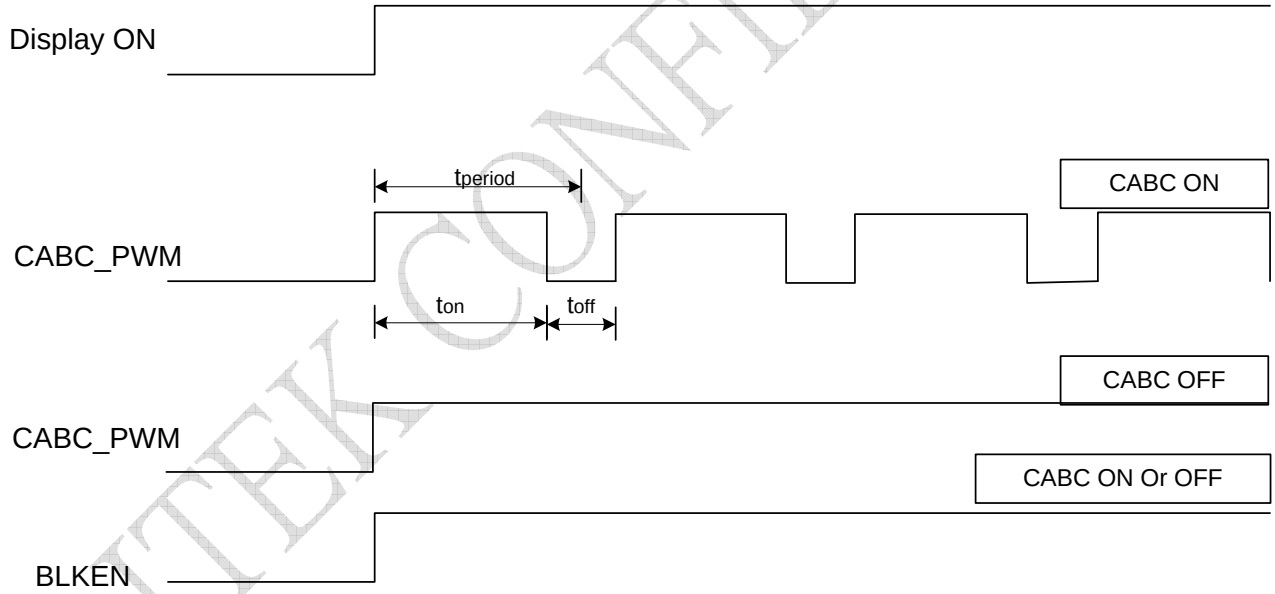
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9. CABC (Content Adaptive Brightness Control)

ILI61230 provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. ILI6123 will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.



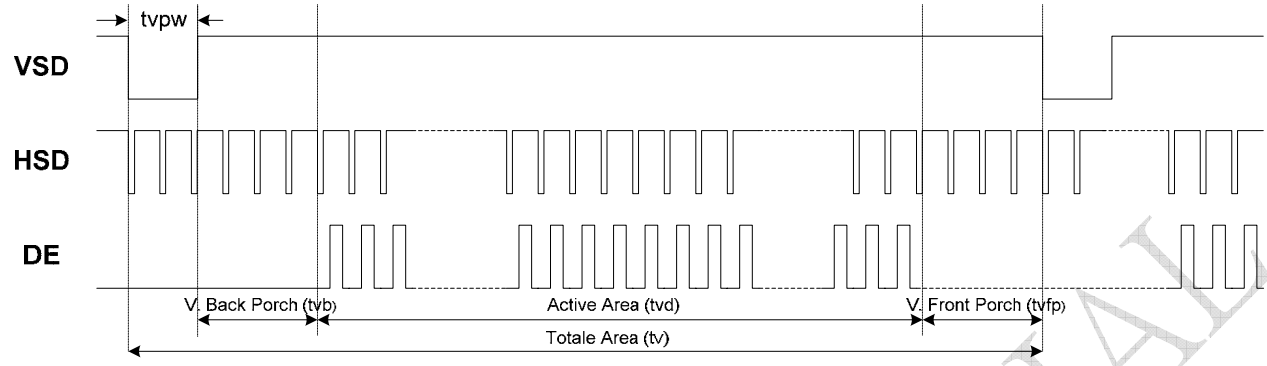
The CABC function can be turned ON/OFF via external pin as CABC_EN and also can be configured by software commands via SPI mode for performance optimization. IL6123 can calculate the backlight brightness level and send a PWM pulse to LED driver via CABC_EN pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied ILI6123 to control LED driver.



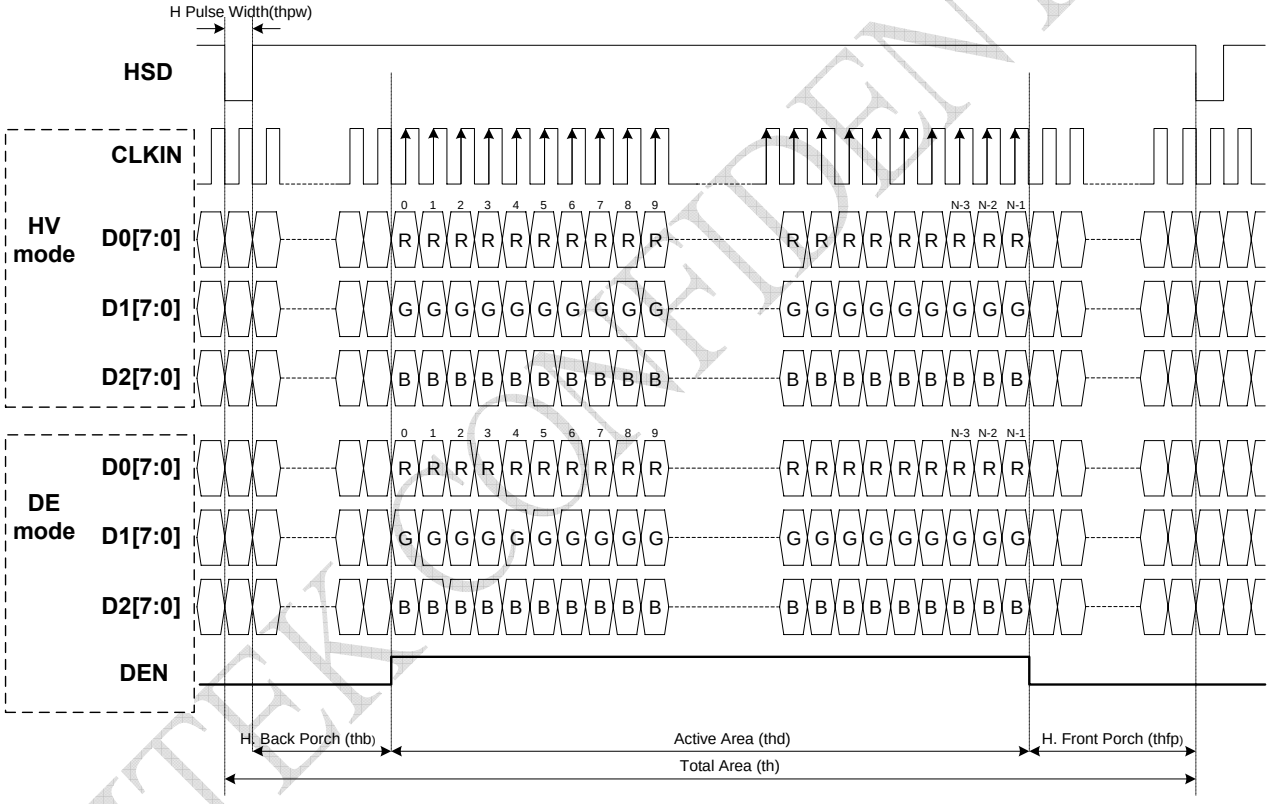
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10. Display Data Input Timing

10.1. Vertical Input Timing



10.2. Horizontal Input Timing



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10.3. Timing Characteristic

Resolution 800*480

Horizontal input timing

Parameter		Symbol	Value			Unit	Note
Horizontal display area		thd		800		DCLK	
DCLK frequency		fclk	Min.	Typ.	Max.		
			-	33.3	50	MHz	
1 Horizontal Line		th		928		DCLK	
HSD pulse width	Min.	thpw		1			thb+thpw=88 DCLK is fixed.
	Typ.			48			
	Max.			-			
HSD Back Porch (Blanking)		thb	-	40	-		
HSD Front Porch		thfp	-	40	-		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd		480		H	
VSD period time	tv	-	525	-	H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	3	-	H	
VSD Back Porch (Blanking)	tvb	-	29	-	H	
VSD Front Porch	tvfp	-	13	-	H	

Resolution 800*600

Horizontal input timing

Parameter		Symbol	Value			Unit	Note
Horizontal display area		thd		800		DCLK	
DCLK frequency		fclk	Min.	Typ.	Max.		
			-	40	50	MHz	
1 Horizontal Line		th		1000		DCLK	
HSD pulse width	Min.	thpw		1			thb+thpw=88 DCLK is fixed.
	Typ.			48			
	Max.			-			
HSD Back Porch (Blanking)		thb	-	40	-		
HSD Front Porch		thfp	-	112	-		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd		600		H	
VSD period time	tv	-	660	-	H	tvpw+tvb=39H Is fixed
VSD pulse width	tvpw	1	3	-	H	
VSD Back Porch (Blanking)	tvb	-	36	-	H	
VSD Front Porch	tvfp	-	21	-	H	

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Resolution 640*480
Horizontal input timing

Parameter		Symbol	Value			Unit	Note
Horizontal display area		thd	640			DCLK	
DCLK frequency		fclk	Min.	Typ.	Max.		
			-	24	50	MHz	
1 Horizontal Line		th	760			DCLK	
HSD pulse width	Min.	thpw	1				thb+thpw=88 DCLK is fixed.
	Typ.		48				
	Max.		-				
HSD Back Porch (Blanking)		thb	-	40	-		
HSD Front Porch		thfp	-	32	-		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	480			H	
VSD period time	tv	-	525		H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	3		H	
VSD Back Porch (Blanking)	tvb	-	29		H	
VSD Front Porch	tvfp	-	13		H	

Resolution 320*240
Horizontal input timing

Parameter		Symbol	Value			Unit	Note
Horizontal display area		thd	320			DCLK	
DCLK frequency		fclk	Min.	Typ.	Max.		
			-	7.1	50	MHz	
1 Horizontal Line		th	440			DCLK	
HSD pulse width	Min.	thpw	1				thb+thpw=88 DCLK is fixed.
	Typ.		48				
	Max.		-				
HSD Back Porch (Blanking)		thb	40				
HSD Front Porch		thfp	32				

Vertical input timing

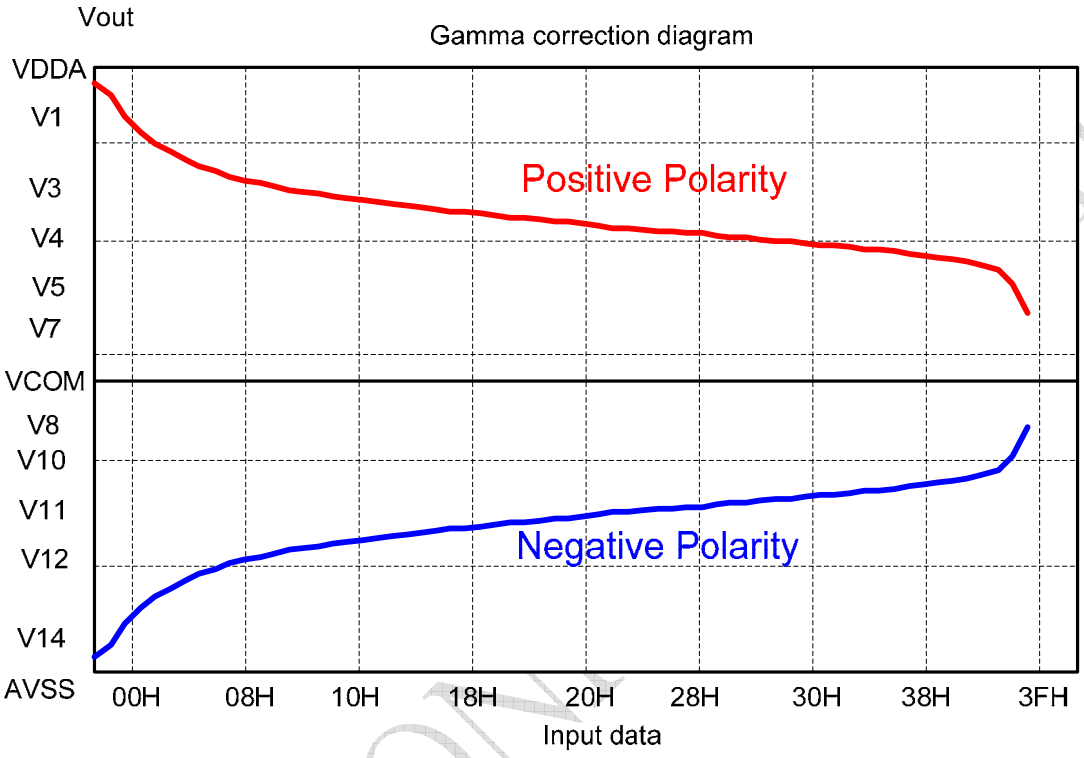
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	240			H	
VSD period time	tv	270			H	tvpw+tvb=17H Is fixed
VSD pulse width	tvpw	1			H	
VSD Back Porch (Blanking)	tvb	-	16		H	
VSD Front Porch	tvfp	-	13		H	

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11. Relationship between gamma correction and output voltage

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V14 gamma correction reference voltage inputs. The figure in the following shows the relationship between the input data and the output voltage. Refer the next page for the relative values and voltage calculation method.

11.1. Gamma correction characteristic curve:



Note: AVDD-1 > V1 > V3 > V4 > V5 > V7; V8 >V10 > V11 > V12 > V14 > AGND+0.1V

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11.2. Gamma correction resistor ratio

	Name	Ration		Name	Ration	
V1/V14	R0	12.9		R32	1	V4/V11
	R1	11.5		R33	1	
	R2	10		R34	1	
	R3	8.6		R35	1	
	R4	7.2		R36	1	
	R5	5.7		R37	1	
	R6	4.8		R38	1	
	R7	4		R39	1	
	R8	3.5		R40	1	
	R9	3		R41	1	
	R10	2.7		R42	1	
	R11	2.5		R43	1	
	R12	2.2		R44	1	
	R13	2.1		R45	1	
	R14	2		R46	1.1	
	R15	1.8		R47	1.1	
V3/V12	R16	1.7		R48	1.1	V5/V10
	R17	1.6		R49	1.1	
	R18	1.5		R50	1.1	
	R19	1.5		R51	1.2	
	R20	1.4		R52	1.3	
	R21	1.4		R53	1.3	
	R22	1.3		R54	1.4	
	R23	1.3		R55	1.6	
	R24	1.2		R56	1.7	
	R25	1.2		R57	1.9	
	R26	1.2		R58	2.2	
	R27	1.1		R59	2.6	
	R28	1.1		R60	3.2	
	R29	1.1		R61	5.6	
	R30	1.1		R62	44	
V4/V11	R31	1		R63		V7/V8

Ratio→ 1: 62

Total Ratio= 192.7

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11.3. Output Voltage VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage	Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14	20H	V4	V11
01H	V3 + (V1 – V3) X 71.6 / 84.5	V14+ (V12 – V14)X 12.9 / 84.5	21H	V5 + (V4 – V5) X 15.2 / 16.2	V11 + (V10 – V11) X 1 / 16.2
02H	V3 + (V1 – V3)X 60.1 / 84.5	V14+ (V12 – V14)X 24.4 / 84.5	22H	V5 + (V4 – V5) X 14.2 / 16.2	V11 + (V10 – V11) X 2 / 16.2
03H	V3 + (V1 – V3) X 50.1/ 84.5	V14+ (V12 – V14)X 34.4 / 84.5	23H	V5 + (V4 – V5) X 13.2 / 16.2	V11 + (V10 – V11) X 3 / 16.2
04H	V3 + (V1 – V3) X 41.5 / 84.5	V14+ (V12 – V14)X 43 / 84.5	24H	V5 + (V4 – V5) X 12.2 / 16.2	V11 + (V10 – V11) X 4 / 16.2
05H	V3 + (V1 – V3) X 34.3 / 84.5	V14 + (V12 – V14)X 50.2/ 84.5	25H	V5 + (V4 – V5) X 11.2 / 16.2	V11 + (V10 – V11) X 5 / 16.2
06H	V3 + (V1 – V3) X 28.6 / 84.5	V14 + (V12 – V14)X 55.9 / 84.5	26H	V5 + (V4 – V5) X 10.2 / 16.2	V11 + (V10 – V11) X 6 / 16.2
07H	V3 + (V1 – V3) X 23.8 / 84.5	V14 + (V12 – V14)X 60.7 / 84.5	27H	V5 + (V4 – V5) X 9.2 / 16.2	V11 + (V10 – V11) X 7 / 16.2
08H	V3 + (V1 – V3) X 19.8 / 84.5	V14 + (V12 – V14)X 64.7 / 84.5	28H	V5 + (V4 – V5) X 8.2 / 16.2	V11 + (V10 – V11) X 8 / 16.2
09H	V3 + (V1 – V3) X 16.3 / 84.5	V14 + (V12 – V14)X 68.2 / 84.5	29H	V5 + (V4 – V5) X 7.2 / 16.2	V11 + (V10 – V11) X 8 / 16.2
0AH	V3 + (V1 – V3) X 13.3 / 84.5	V14 + (V12 – V14)X 71.2 / 84.5	2AH	V5 + (V4 – V5) X 6.2 / 16.2	V11 + (V10 – V11) X 10 / 16.2
0BH	V3 + (V1 – V3) X 10.6 / 84.5	V14 + (V12 – V14)X 73.9 / 84.5	2BH	V5 + (V4 – V5) X 5.2 / 16.2	V11 + (V10 – V11) X 11 / 16.2
0CH	V3 + (V1 – V3) X 8.1 / 84.5	V14 + (V12 – V14)X 76.4 / 84.5	2CH	V5 + (V4 – V5) X 4.2 / 16.2	V11 + (V10 – V11) X 12 / 16.2
0DH	V3 + (V1 – V3) X 5.9 / 84.5	V14 + (V12 – V14)X 78.6 / 84.5	2DH	V5 + (V4 – V5) X 3.2 / 16.2	V11 + (V10 – V11) X 13/ 16.2
0EH	V3 + (V1 – V3) X 3.8 / 84.5	V14 + (V12 – V14)X 80.7 / 84.5	2EH	V5 + (V4 – V5) X 2.2 / 16.2	V11 + (V10 – V11) X 14 / 16.2
0FH	V3 + (V1 – V3) X 1.8 / 84.5	V14 + (V12 – V14)X 82.7 / 84.5	2FH	V5 + (V4 – V5) X 1.1 / 16.2	V11 + (V10 – V11) X 15.1/ 16.2
10H	V3	V12	30H	V5	V10
11H	V4 + (V3 – V4) X 19 / 20.7	V12 + (V11 – V12)X 1.7 / 20.7	31H	V7 + (V5 – V7) X 70.2 / 71.3	V10 + (V8 – V10) X 1.1 / 71.3
12H	V4 + (V3 – V4) X 17.4 / 20.7	V12 + (V11 – V12)X 3.3 / 20.7	32H	V7 + (V5 – V7) X 69.1 / 71.3	V10 + (V8 – V10) X 2.2 / 71.3
13H	V4 + (V3 – V4) X 15.9 / 20.7	V12 + (V11 – V12)X 4.8 / 20.7	33H	V7 + (V5 – V7) X 68 / 71.3	V10 + (V8 – V10) X 3.3 / 71.3
14H	V4 + (V3 – V4) X 14.4 / 20.7	V12 + (V11 – V12)X 6.3 / 20.7	34H	V7 + (V5 – V7) X 66.8 / 71.3	V10 + (V8 – V10) X 4.5 / 71.3
15H	V4 + (V3 – V4) X 13 / 20.7	V12 + (V11 – V12)X 7.7 / 20.7	35H	V7 + (V5 – V7) X 65.5 / 71.3	V10 + (V8 – V10) X 5.8 / 71.3
16H	V4 + (V3 – V4) X 11.6 / 20.7	V12 + (V11 – V12)X 9.1 / 20.7	36H	V7 + (V5 – V7) X 64.2 / 71.3	V10 + (V8 – V10) X 7.1 / 71.3
17H	V4 + (V3 – V4) X 10.3 / 20.7	V12 + (V11 – V12)X 10.4 / 20.7	37H	V7 + (V5 – V7) X 62.8 / 71.3	V10 + (V8 – V10) X 8.5 / 71.3
18H	V4 + (V3 – V4) X 9 / 20.7	V12 + (V11 – V12)X 11.7 / 20.7	38H	V7 + (V5 – V7) X 61.2 / 71.3	V10 + (V8 – V10) X 10.1 / 71.3
19H	V4 + (V3 – V4) X 7.8 / 20.7	V12 + (V11 – V12)X 12.9 / 20.7	39H	V7 + (V5 – V7) X 59.5 / 71.3	V10 + (V8 – V10) X 11.8 / 71.3
1AH	V4 + (V3 – V4) X 6.6 / 20.7	V12 + (V11 – V12)X 14.1 / 20.7	3AH	V7 + (V5 – V7) X 57.6 / 71.3	V10 + (V8 – V10) X 13.7 / 71.3
1BH	V4 + (V3 – V4) X 5.4 / 20.7	V12 + (V11 – V12)X 15.3 / 20.7	3BH	V7 + (V5 – V7) X 55.4 / 71.3	V10 + (V8 – V10) X 15.9 / 71.3
1CH	V4 + (V3 – V4) X 4.3 / 20.7	V12 + (V11 – V12)X 16.4 / 20.7	3CH	V7 + (V5 – V7) X 52.8 / 71.3	V10 + (V8 – V10) X 18.5 / 71.3
1DH	V4 + (V3 – V4) X 3.2 / 20.7	V12 + (V11 – V12)X 17.5 / 20.7	3DH	V7 + (V5 – V7) X 49.6 / 71.3	V10 + (V8 – V10) X 21.7 / 71.3
1EH	V4 + (V3 – V4) X 2.1 / 20.7	V12 + (V11 – V12)X 18.6 / 20.7	3EH	V7 + (V5 – V7) X 44 / 71.3	V10 + (V8 – V10) X 27.3 / 71.3
1FH	V4 + (V3 – V4) X 1 / 20.7	V12 + (V11 – V12)X 19.7 / 20.7	3FH	V7	V8

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12. Power ON/OFF Sequence

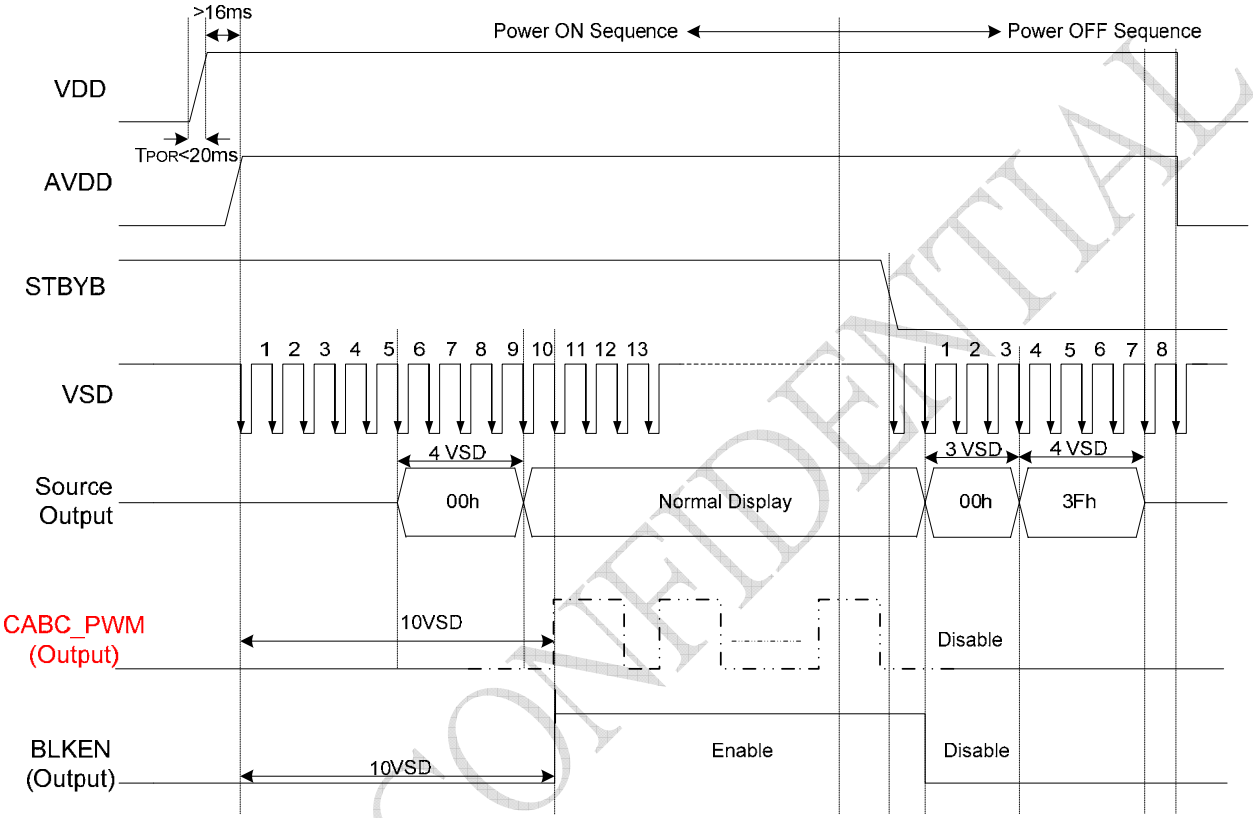
12.1. Normal mode power on/ off

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VDD, DGND→ AVDD, AGND → V1 to V14

Power OFF: V1 to V14 → AVDD, AGND→ VDD, DGND

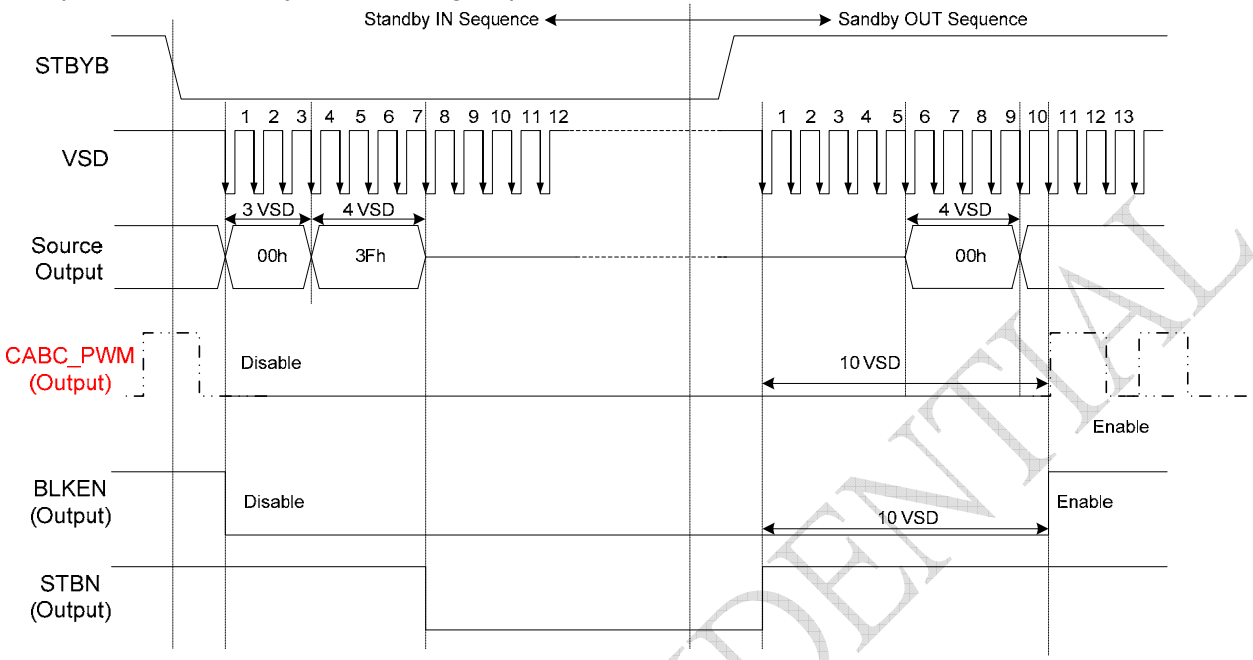
In order to prevent ILI6123 from power ON reset fail, the rising time (t_{POR}) of the digital power supply VDD should be maintained within given specifications. The power ON/OFF timing sequence is illustrated as below:



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12.2. Standby ON/OFF Control

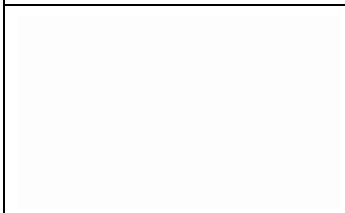
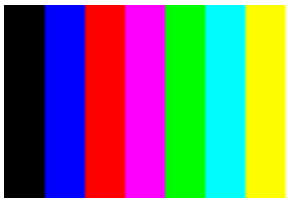
ILI6123 supports Standby mode for saving power consumption, the source driver will turn off and all source output channel will be Hi-Z state when chip in Standby mode. The Standby mode can be controlled via STBYB pin and the Standby ON/FF timing sequence is illustrated as below:



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13. The BIST Patterns for Aging Mode Test

ILI6123 supports the function to generate BIST patterns for Aging mode test automatically. When external BIST pin goes “H” level, then ILI6123 will leave Normal operation mode and starts to generate the BIST patterns to LCD panel without external clock signal, The BIST patterns is illustrated as below:

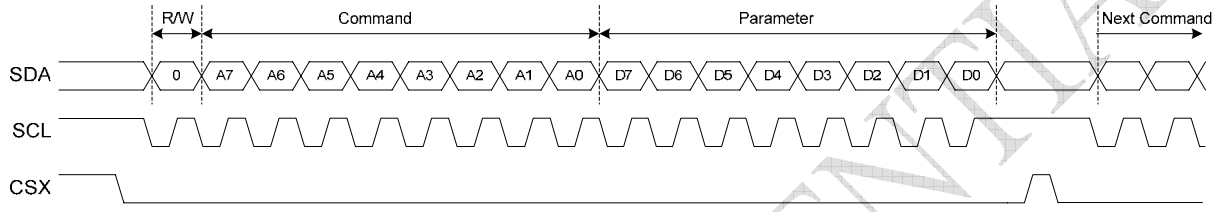
1	2	3	4
Red	Green	Blue	Black
			
5	6	7	8
White	Vertical 8-color stripe	Horizontal 64-gray scale	Vertical 64-gray scale
			
9	10	11	12
Gray with black block	Gray with black dot	Gray with black line	Black with white frame
			

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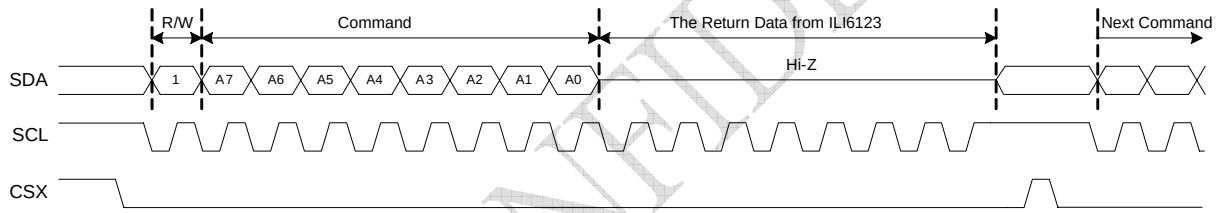
14. The Command Format for 3-line Serial Interface

ILI6123 using the 3-line serial port as communication interface for all the commands and parameters of CABC function. This 3-line serial communication can be bi-directional controlled by the “R/W” bit in address field. Under read mode, the 3-line engine in ILI6123 will return the data during “Data phase”. The returned data should be latched at the rising edge of SPCK by external controller. Data in the “Hi-Z phase” will be ignored by 3-line engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under “Hi-Z phase” and “Data phase”.
Each Read/Write operation should be exactly 17 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 17 bit data during a CSX Low period will be ignored by 3-line engine.
The timing diagram of read/write operation is illustrated as below:

Write Operation



Read Operation



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14.1. Command List

Command Function	D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Display Brightness	0	0	0	1	0	1	0	0	0	1	51h
	1	0	DBV[7:0]								XX
Read Display Brightness Value	0	0	0	1	0	1	1	0	1	0	52h
	1	1	X	X	X	X	X	X	X	X	XX
	1	1	DBV[7:0]								XX
Write CTRL Display	0	0	0	1	0	1	0	0	1	1	53h
	1	0	0	0	BCTRL	0	DD	BL	0	0	XX
Read CTRL Display	0	0	0	1	0	1	0	1	0	0	54h
	1	1	X	X	X	X	X	X	X	X	XX
	1	1	0	0	BCTRL	0	DD	BL	0	0	XX
Write Content Adaptive Brightness Control	0	0	1	0	0	0	0	0	1	0	82h
	1	0	0	0	C[1:0]		0	0	0	0	XX
Read Content Adaptive Brightness Control	0	0	1	0	0	0	0	0	1	0	82h
	1	1	0	0	C[1:0]		0	0	0	0	XX
Write CABC Minimum Brightness	0	0	0	1	0	1	1	1	1	0	5Eh
	1	0	CMB[7:0]								XX
Read CABC Minimum Brightness	0	0	0	1	0	1	1	1	1	1	5Fh
	1	1	CMB[7:0]								XX
CABC Control 1	0	0	0	1	1	0	0	0	0	0	60h
	1	0	PWM_DIV[7:0]								XX
CABC Control 2	0	0	0	1	1	0	0	0	0	1	61h
	1	0	THRES_MOV[3:0]				THRES_STILL[3:0]				XX
CABC Control 3	0	0	0	1	1	0	0	0	1	0	62h
	1	0	0	0	0	0	THRES_UI[3:0]				XX
CABC Control 4	0	0	0	1	1	0	0	0	1	1	63h
	1	0	DTH_MOV[3:0]				DTH_STILL[3:0]				XX
CABC Control 5	0	0	0	1	1	0	0	1	0	0	64h
	1	0	0	0	0	0	DTH_UI[3:0]				XX
CABC Control 6	0	0	0	1	1	0	0	1	0	1	65h
	1	0	DIM_OPT2[3:0]					DIM_OPT1[2:0]			XX

Note : 1. These commands above can be transmitted from host to driver IC via 3-line SPI mode only.
2. When D/C in the table above is '0', it means the data on SDA pin is treated as "Command" and the data is treated as "Parameter" when D/C is set to '1'.
3. When R/W in the table above is '0', it means the "Write" operation is executed and the "Read" operation is executed when R/W is set to '1'

14.2. Command Description

14.2.1. Write Display Brightness Value (51h)

51h	WRDISBV (Write Display Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	0	1	51h
Parameter	DBV[7:0]								XX
Description	This command is used to adjust the brightness value of the display. **DBV[7:0]**: 8 bit, for display brightness of manual brightness setting and CABC in ILI6123. There is a PWM output signal, CABC_PWM pin to control the LED driver IC in order to control display brightness.								

14.2.2. Read Display Brightness Value (52h)

52h	RDDISBV (Read Display Brightness Value)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	1	0	51h
Parameter	DBV[7:0]								XX
Description	This command is used to return the brightness value of the display. DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when BCTRL bit is '1'. When bit BCTRL of "Write CTRL Display (53h)" command is '1' and C1/C0 bit of "Write Content Adaptive Brightness Control (55h)" command are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (51h)" command.								

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14.2.3. Write CTRL Display Value (53h)

53h	WRCTRLD (Write Control Display)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	1	1	53h
Parameter	X	X	BCTRL	X	DD	BL	X	X	XX

Description

This command is used to control display brightness.
BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.
When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.
X = Don't care

14.2.4. Read CTRL Display Value (54h)

54h	RDCTRLD (Read Control Display Value)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	0	0	54h
Parameter	X	X	BCTRL	X	DD	BL	X	X	XX

Description

This command is used to control display brightness.
BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

X = Don't care

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14.2.5. Write Content Adaptive Brightness Control Value (82h)

82h	WRCABC (Write Content Adaptive Brightness Control)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	1	0	0	0	0	0	1	0	82h
Parameter	0	0	C[1:0]		0	0	0	0	XX
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. C[1:0] / Description 0 0 / CABC OFF 0 1 / User Interface Image 1 0 / Still Picture 1 1 / Moving Image X = Don't care								

Remark: D3~D0 must write parameter with "0000" code.

14.2.6. Read Content Adaptive Brightness Control Value (82h)

82h	RDCABC (Read Content Adaptive Brightness Control)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	1	0	0	0	0	0	1	0	82h
Parameter	0	0	C[1:0]		0	0	0	0	XX
Description	This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality which are defined on the table below. C[1:0] / Description 0 0 / CABC OFF 0 1 / User Interface Image 1 0 / Still Picture 1 1 / Moving Image * = Don't care								

14.2.7. Write CABC Minimum Brightness (5Eh)

5Eh	WRCABCMB (Write CABC Minimum Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	5Eh
Parameter	CMB[7:0]								XX
Description	This command is used to set the minimum brightness value of the display for CABC function. **CMB[7:**0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.								

14.2.8. Read CABC Minimum Brightness (5Fh)

5Fh	RDCABCMB (Read CABC Minimum Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	1	5Fh
Parameter	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command.								

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14.2.9. CABC Control 1 (60h)

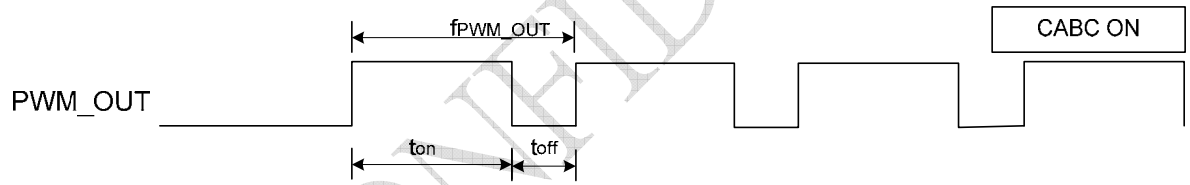
60h	CABCCTRL1 (CABC Control 1)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	60h
Parameter	PWM_DIV[7:0]								XX

Description

PWM_DIV[7:0]: BLK_EN output period control. This command is used to adjust the PWM waveform period of BLK_EN. The PWM period can be calculated using the equation in the following.

$$f_{PWM_OUT} = \frac{8MHz}{(PWM_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0]								f_{BLK_EN}
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	TBD
0	0	0	0	0	0	0	1	TBD
0	0	0	0	0	0	1	0	TBD
0	0	0	0	0	0	1	1	TBD
0	0	0	0	0	1	0	0	TBD
:								:
1	1	1	1	1	0	1	1	TBD
1	1	1	1	1	1	0	0	TBD
1	1	1	1	1	1	0	1	TBD
1	1	1	1	1	1	1	0	TBD
1	1	1	1	1	1	1	1	TBD



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

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14.2.10. CABC Control 2 (61h)

61h	CABCCTRL2 (CABC Control 2)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	1	61h
Parameter	THRES_MOV[3:0]				THRES_STILL[3:0]				XX

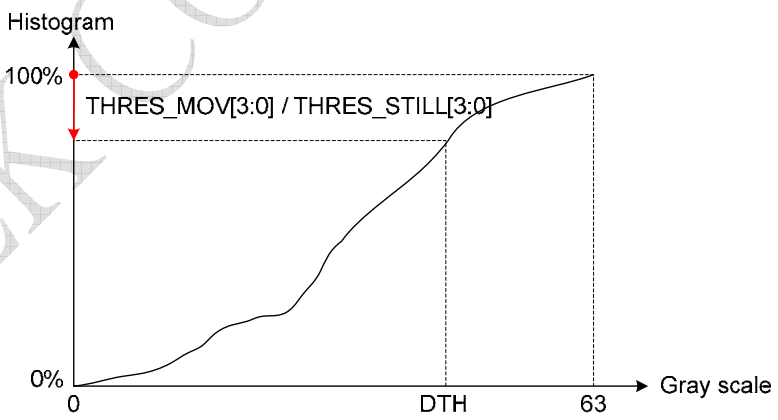
Description

THRES_MOV[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_MOV[3:0]				Description	THRES_MOV[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	99 %	1	0	0	0	84 %
0	0	0	1	98 %	1	0	0	1	82 %
0	0	1	0	96 %	1	0	1	0	80 %
0	0	1	1	94 %	1	0	1	1	78 %
0	1	0	0	92 %	1	1	0	0	76 %
0	1	0	1	90 %	1	1	0	1	74 %
0	1	1	0	88 %	1	1	1	0	72 %
0	1	1	1	86 %	1	1	1	1	70 %

THRES_STILL[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_STILLI[3:0]				Description	THRES_STILL[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	99 %	1	0	0	0	84 %
0	0	0	1	98 %	1	0	0	1	82 %
0	0	1	0	96 %	1	0	1	0	80 %
0	0	1	1	94 %	1	0	1	1	78 %
0	1	0	0	92 %	1	1	0	0	76 %
0	1	0	1	90 %	1	1	0	1	74 %
0	1	1	0	88 %	1	1	1	0	72 %
0	1	1	1	86 %	1	1	1	1	70 %



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14.2.11. CABC Control 3 (62h)

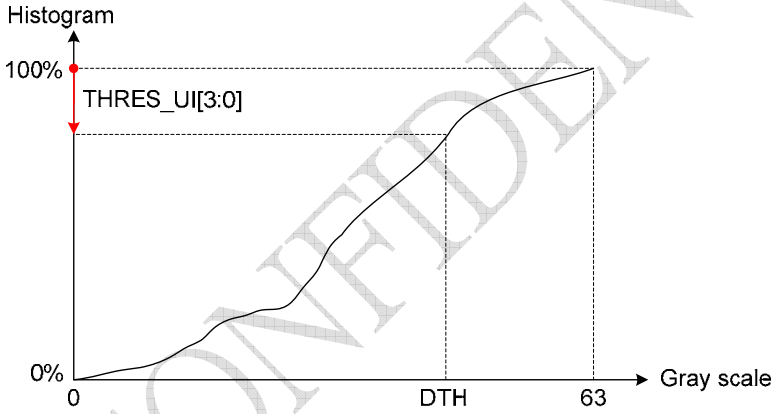
62h	CABCCTRL3 (CABC Control 3)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	0	62h
Parameter	0	0	0	0	THRES_UI[3:0]				XX

Description

THRES_UI[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



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14.2.12. CABC Control 4 (63h)

63h	CABCCTRL4 (CABC Control 4)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	1	63h
Parameter	DTH_MOV[3:0]				DTH_STILL[3:0]				XX

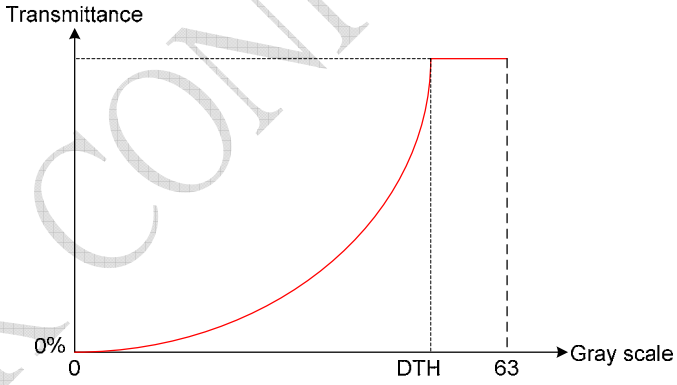
Description

DTH_MOV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.

DTH_MOV[3:0]				Description	DTH_MOV[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	224	1	0	0	0	192
0	0	0	1	220	1	0	0	1	188
0	0	1	0	216	1	0	1	0	184
0	0	1	1	212	1	0	1	1	180
0	1	0	0	208	1	1	0	0	176
0	1	0	1	204	1	1	0	1	172
0	1	1	0	200	1	1	1	0	168
0	1	1	1	196	1	1	1	1	164

DTH_OPT[2:0]: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.

DTH_STILLI[3:0]				Description	DTH_STILL[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	224	1	0	0	0	192
0	0	0	1	220	1	0	0	1	188
0	0	1	0	216	1	0	1	0	184
0	0	1	1	212	1	0	1	1	180
0	1	0	0	208	1	1	0	0	176
0	1	0	1	204	1	1	0	1	172
0	1	1	0	200	1	1	1	0	168
0	1	1	1	196	1	1	1	1	164



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14.2.13. CABC Control 5 (64h)

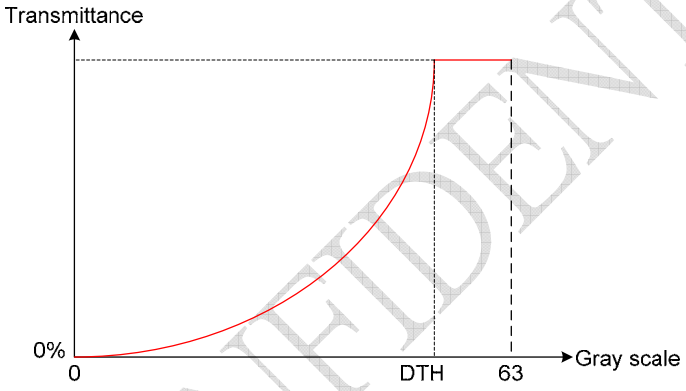
64h	CABCCTRL5 (CABC Control 5)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	0	64h
Parameter	0	0	0	0	DTH_UI[3:0]				XX

Description

DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.

DTH_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	2-4
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



14.2.14. CABC Control 6 (65h)

65h	CABCCTRL6 (CABC Control 6)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	65h
Parameter	DIM_OPT2[3:0]				0	DIM_OPT1[2:0]			XX

Description

DIM_OPT1[3:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision.

DIM_OPT1[2:0]			Description
D2	D1	D0	
0	0	0	1 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	4 frames
1	0	0	8 frames
1	0	1	16 frames
1	1	0	32 frames
1	1	1	64 frames

DIM_OPT2[2:0]: This parameter is used to set the imitation of minimum brightness change. If this parameter is large than the difference between target brightness and current brightness, then the brightness will not change.

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15. DC Characteristic

15.1. Absolute Maximum Rating (DGND = AGND=0V, Ta=25℃)

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.5	--	+5.0	V
Power supply voltage 2	VDDA	-0.5	--	+15	V
Operation temperature	TOPR	-20	--	+85	°C
Storage temperature	TSTG	-55	--	+125	°C

*Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

15.2. DC Electrical Characteristics (DGND=AGND=0V, Ta=25℃)

Note: VDD=3.0 ~ 3.6V, VDDA=6.5~13.5V, DGND=AGND=0V, Ta=-20~+85℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Low level input voltage	Vil	0	-	0.3xVDD	V	For the digital circuit
High level input voltage	Vih	0.7xVDD	-	VDD	V	For the digital circuit
Input leakage current	Ii	-	-	±1	uA	For the digital circuit
High level output voltage	Voh	VDD-0.4	-	VDD	V	Ioh= -400mA
Low level output voltage	Vol	DGND	-	GND+0.4	V	Iol= +400mA
Pull low/high resistor	Ri	200K	250K	300K	ohm	For the digital input pin @ VDD=3.3V
Digital Operation current	Idd	-	T.B.D	T.B.D	mA	Fclk=50 MHz, FLD=48KHz, VDD=3.3V
Digital Stand-by current	Ist1	-	T.B.D	T.B.D	ua	Clock & all functions are stopped
Analog Operating Current	Idda	-	T.B.D	T.B.D	mA	No load, Fclk=50MHz, FLD=48KHz @ VDDA=10V,V1=8V, V14=0.4V
Analog Stand-by current	Ist2	-	T.B.D	T.B.D	ua	No load, clock and all functions are stopped
Input level of V1 ~ V7	Vref1	0.4* AVDD	-	AVDD-1	V	Gamma correction voltage input
Input level of V8 ~ V14	Vref2	0.1	-	0.6* AVDD	V	Gamma correction voltage input
Output Voltage deviation	Vod1	-	±20	±35	mV	Vo = AGND+0.1V ~ AGND+0.5V & Vo = VDDA-0.5V ~ VDDA-0.1V
Output Voltage deviation	Vod2	-	±15	±20	mV	Vo = AGND+0.5V ~ VDDA-0.5V
Output Voltage offset between Chips	Voc	-	-	±20	mV	Vo = AGND+0.5V ~ VDDA-0.5V
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	S1 ~ S1200
Sinking Current of Outputs	IOLy	80	-	-	uA	S1 ~ S1200; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	S1 ~ S1200; Vo=13.4V v.s 12.5V , VDDA=13.5V
Resistance of Gamma Table	Rg	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn: Internal gamma resistor

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15.3. AC Electrical Characteristics

Note: VDD=3.0 ~ 3.6V, VDDA=6.5~13.5V, DGND=AGND=0V, Ta=-20~+85℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power On Slew rate	TPOR	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	TRst	50	-	-	us	CLKIN = 50MHz
CLKIN cycle time	Tcph	20	-	-	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	8	-	-	ns	
VSD hold time	Tvhd	8	-	-	ns	
HSD setup time	Thst	8	-	-	ns	
HSD hold time	Thhd	8	-	-	ns	
Data set-up time	Tdsu	8	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to CLKIN
Data hold time	Tdhd	8	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to CLKIN
DE setup time	Tesu	8	-	-	ns	
DE hold time	Tehd	8	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target voltage. CL=120pF, R=10K ohm

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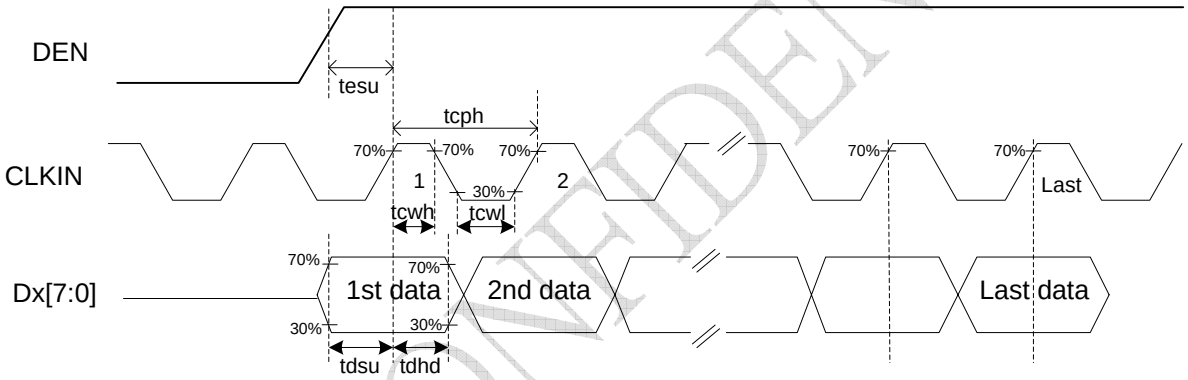
16. Timing

16.1. Parallel 24-bit RGB Mode

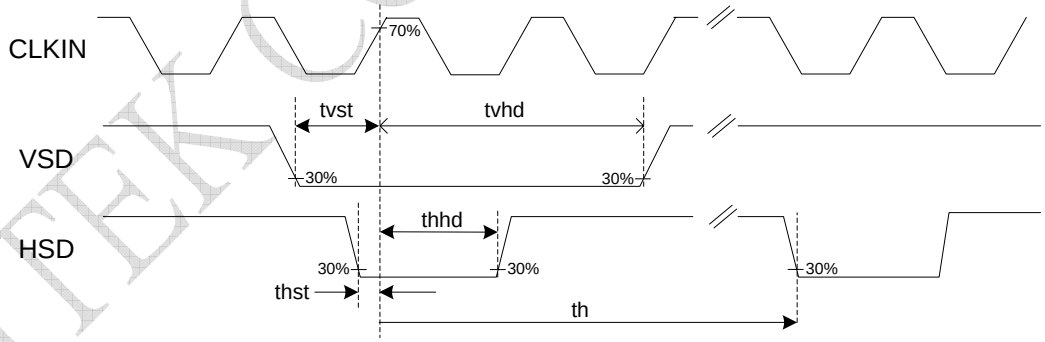
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN Frequency	Fclk	-	40	50	MHz	VDD = 3.0V ~3.6V
CLKIN Cycle Time	Tclk	20	25	-	ns	
CLKIN Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	CLKIN	
Time from HSD to LD	Thld	-	64	-	CLKIN	
Time from HSD to STV	Thstv	-	2	-	CLKIN	
Time from HSD to CKV	Thckv	-	20	-	CLKIN	
Time from HSD to OEV	Thoev	-	4	-	CLKIN	
LD Pulse Width	Twld	-	10	-	CLKIN	
CKV Pulse Width	Twckv	-	66	-	CLKIN	
OEV Pulse Width	Twoev	-	74	-	CLKIN	

16.2. Input Clock and Data Timing Diagram

DE Mode

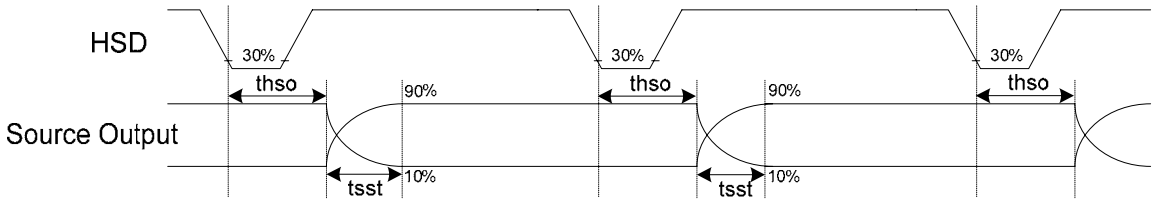


HV Mode

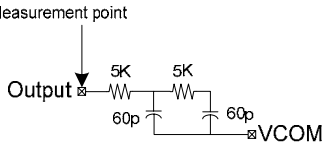


Source output timing diagram

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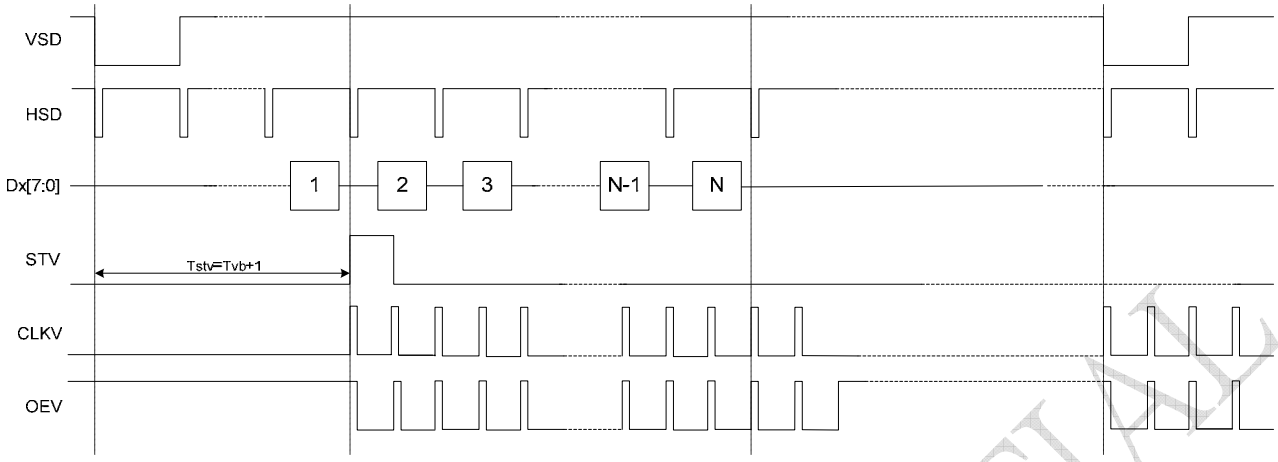


Output Loading condition

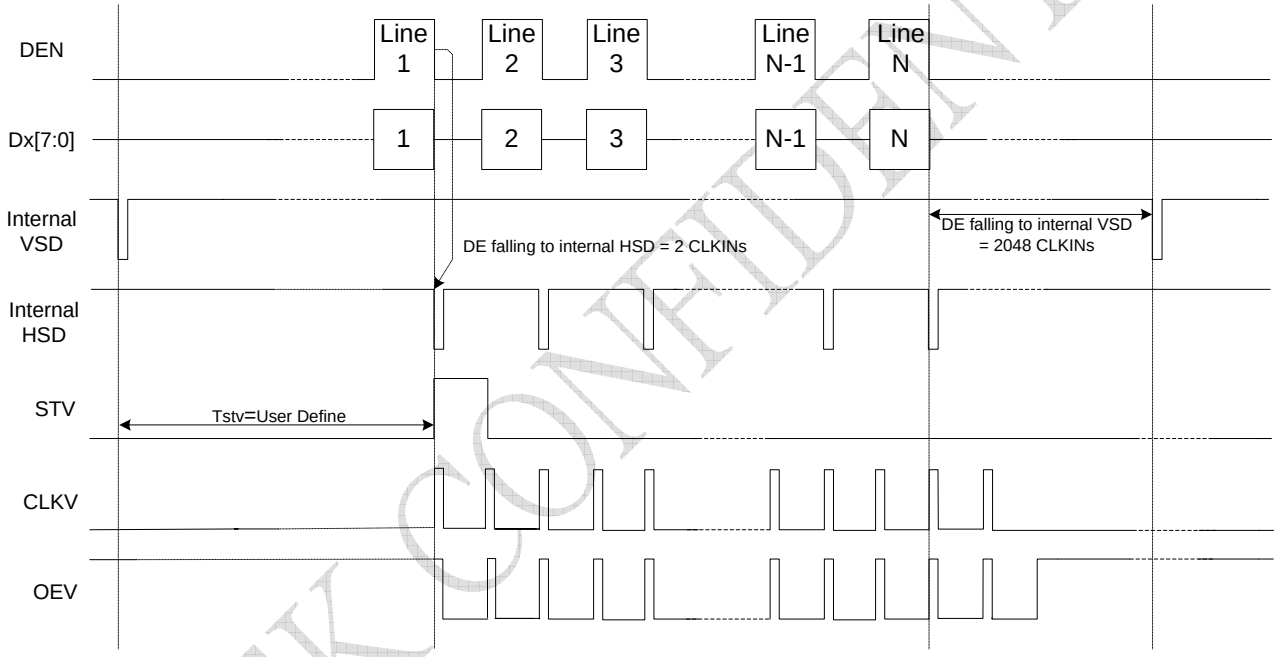


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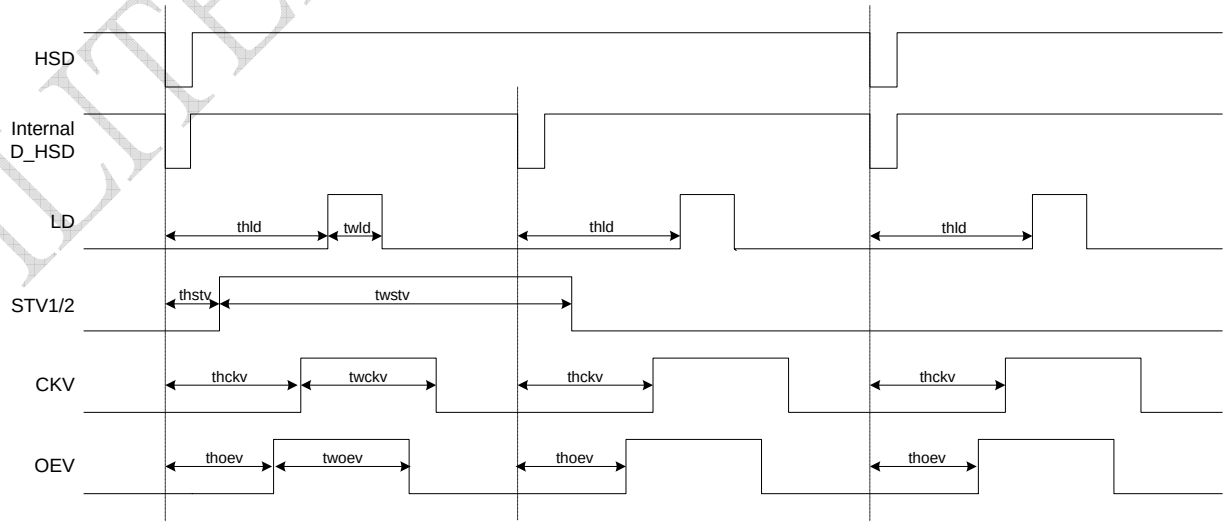
Vertical Timing Diagram of HV Mode (Dual Gate)



Vertical Timing Diagram of DE Mode (Dual Gate)

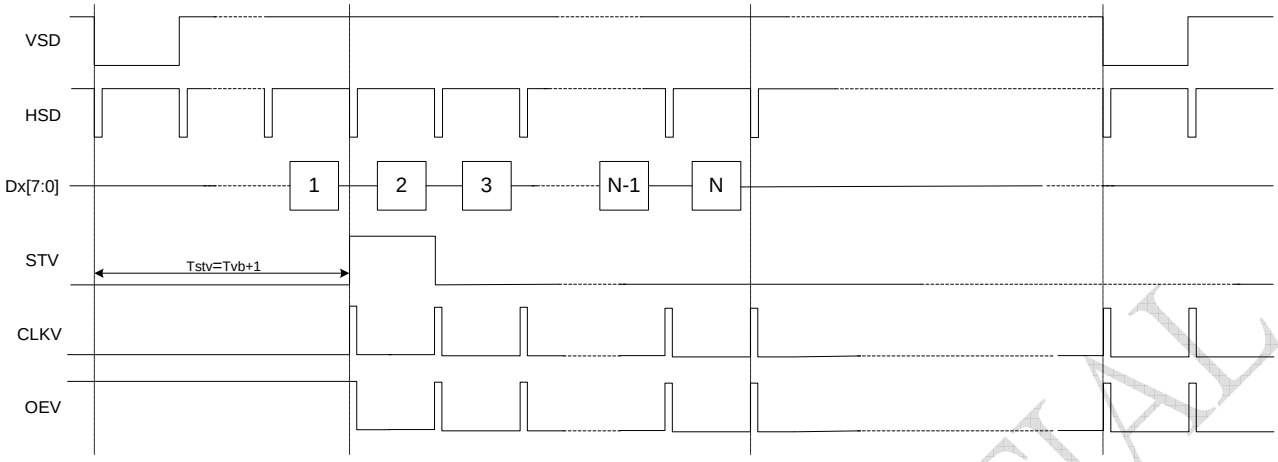


Gate Output Timing Diagram (Dual Gate)

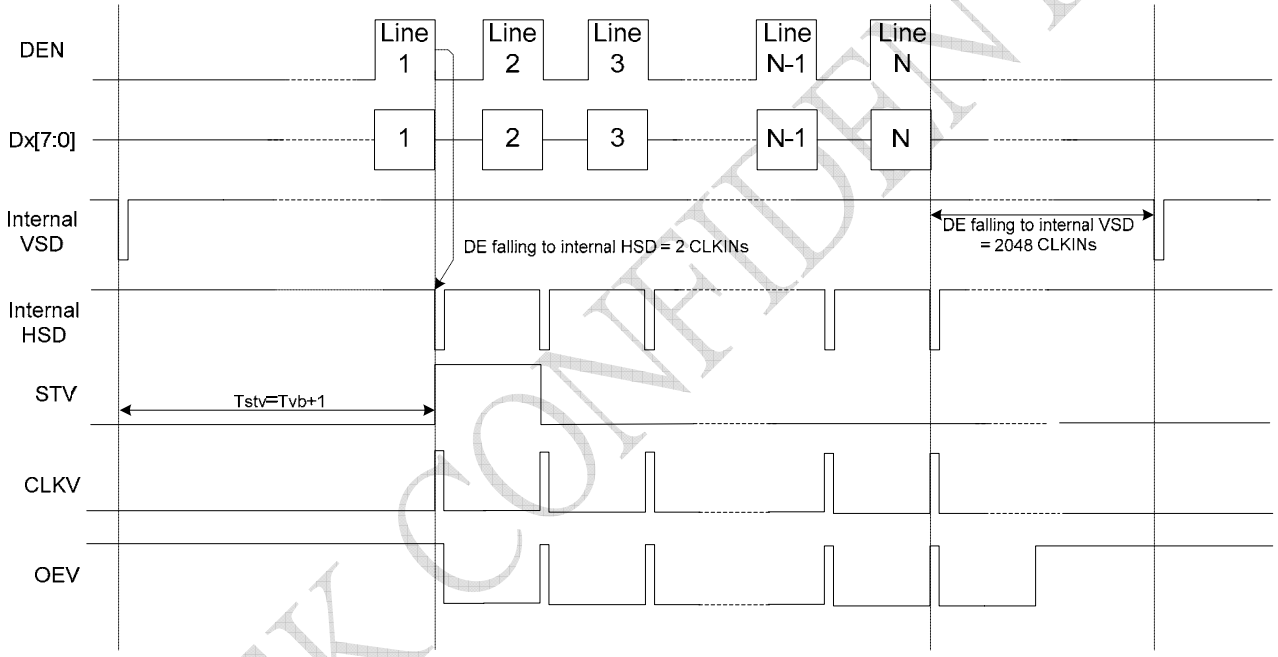


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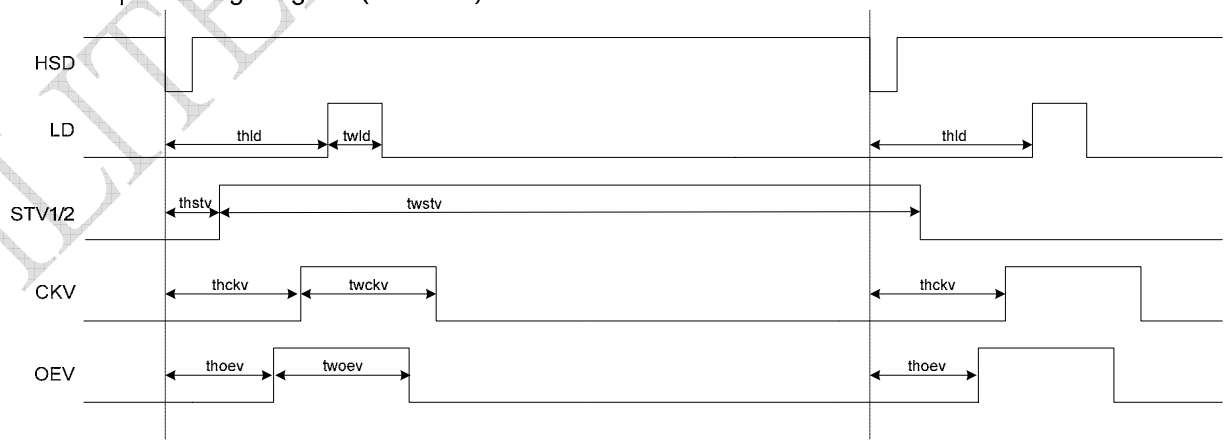
Vertical Timing Diagram of HV Mode (Cascade)



Vertical Timing Diagram of DE Mode (Cascade)

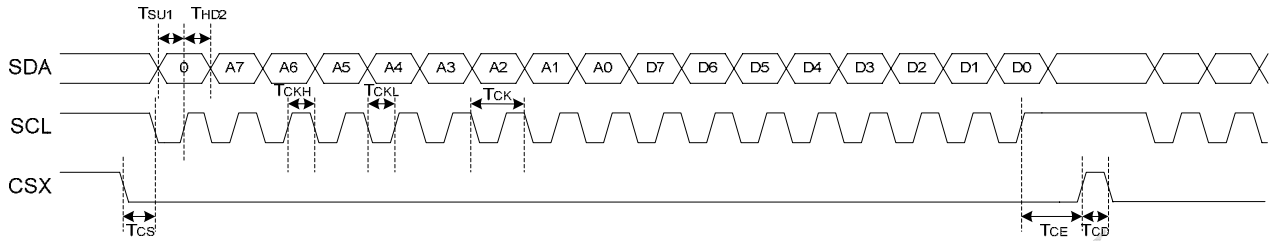


Gate Output Timing Diagram (Cascade)



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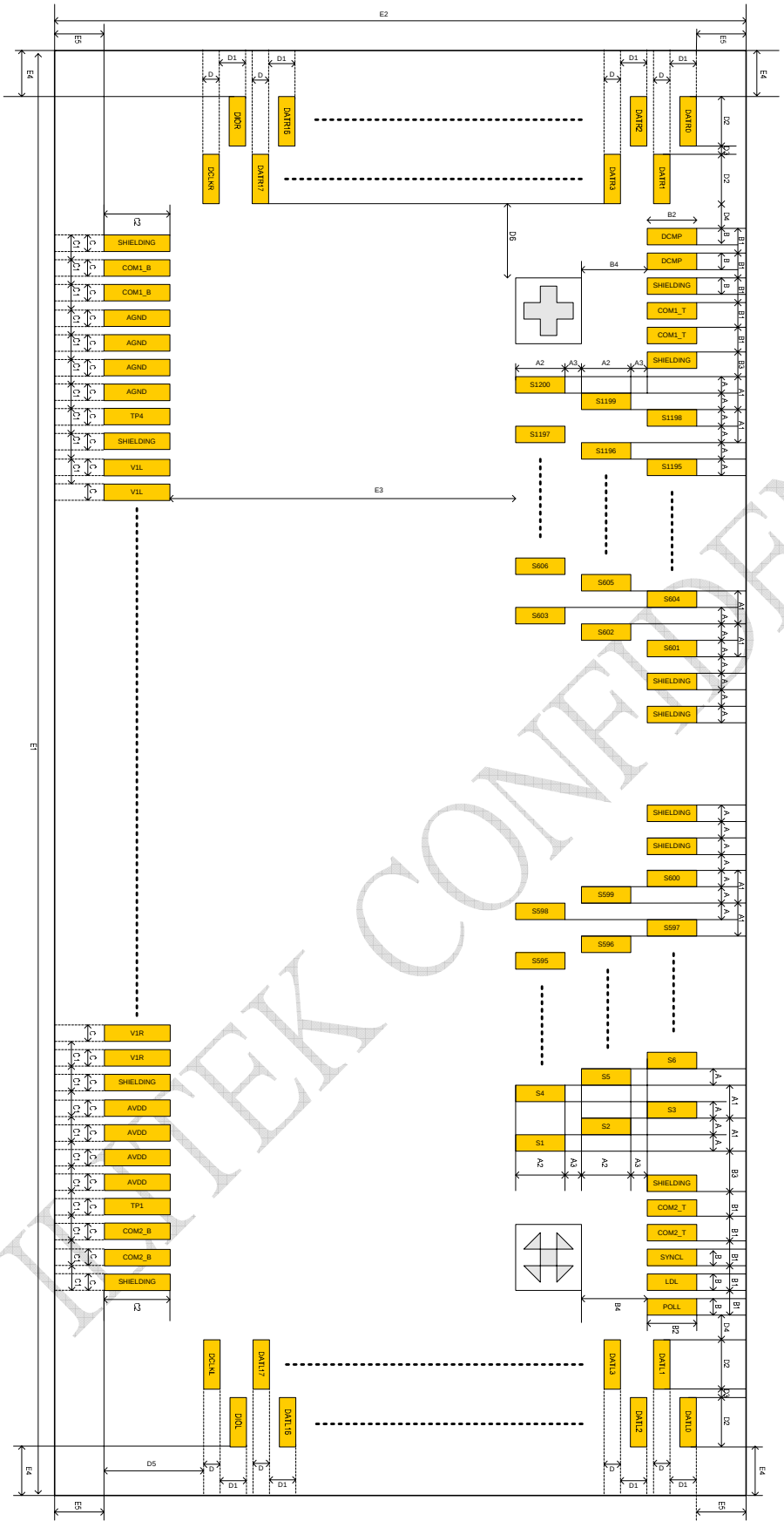
SPI Timing



Parameter	Symbol	Spec			Unit	Conditions
		Min.	Typ.	Max.		
SCL period	T_{CK}	60	--	--	ns	
SCL high width	T_{CKH}	30	--	--	ns	
SCL low width	T_{CKL}	30	--	--	ns	
Data setup time	T_{SU1}	12	--	--	ns	
Data hold time	T_{HD1}	12	--	--	ns	
CSX to SCL setup time	T_{CS}	20	--	--	ns	
CSX to SDA hold time	T_{CE}	20	--	--	ns	
SCX high pulse width	T_{CD}	50	--	--	ns	

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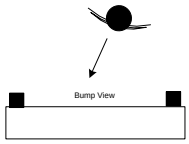
17. Pad Arrangement and Coordination



Symbol	Dimension (um)
A	17um
A1	34um
A2	110um
A3	30um
B	30um
B1	50um
B2	70um
B3	50um
B4	191.5um
C	65um
C1	85um
C2	110um

D	30um
D1	40um
D2	100um
D3	30um
D4	70um
D5	34um
D6	168.5um

E1	22572um (max.)
E2	938um (max.)
E3	324um
E4	57um (max.)
E5	57um (max.)



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number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
1	SHIELDING[69]	-10922.5	-357	61	BIST	-5822.5	-357	121	D25	-722.5	-357
2	SHIELDING[70]	-10837.5	-357	62	SHIELDING[21]	-5737.5	-357	122	D25	-637.5	-357
3	SHIELDING[1]	-10752.5	-357	63	AVDD	-5652.5	-357	123	D24	-552.5	-357
4	COM1_B	-10667.5	-357	64	AVDD	-5567.5	-357	124	D24	-467.5	-357
5	COM1_B	-10582.5	-357	65	AVDD	-5482.5	-357	125	DASHD[7]	-382.5	-357
6	AGND	-10497.5	-357	66	AVDD	-5397.5	-357	126	D23	-297.5	-357
7	AGND	-10412.5	-357	67	SHIELDING[22]	-5312.5	-357	127	D23	-212.5	-357
8	AGND	-10327.5	-357	68	AGND	-5227.5	-357	128	D22	-127.5	-357
9	AGND	-10242.5	-357	69	AGND	-5142.5	-357	129	D22	-42.5	-357
10	TP4	-10157.5	-357	70	AGND	-5057.5	-357	130	DASHD[8]	42.5	-357
11	SHIELDING[2]	-10072.5	-357	71	AGND	-4972.5	-357	131	D21	127.5	-357
12	V1R	-9987.5	-357	72	SHIELDING[23]	-4887.5	-357	132	D21	212.5	-357
13	V1R	-9902.5	-357	73	GND	-4802.5	-357	133	D20	297.5	-357
14	SHIELDING[3]	-9817.5	-357	74	GND	-4717.5	-357	134	D20	382.5	-357
15	V2R	-9732.5	-357	75	GND	-4632.5	-357	135	DASHD[9]	467.5	-357
16	V2R	-9647.5	-357	76	GND	-4547.5	-357	136	D17	552.5	-357
17	SHIELDING[4]	-9562.5	-357	77	SHIELDING[24]	-4462.5	-357	137	D17	637.5	-357
18	V3R	-9477.5	-357	78	BLKEN	-4377.5	-357	138	D16	722.5	-357
19	V3R	-9392.5	-357	79	BLKEN	-4292.5	-357	139	D16	807.5	-357
20	SHIELDING[5]	-9307.5	-357	80	SHIELDING[25]	-4207.5	-357	140	DASHD[10]	892.5	-357
21	V4R	-9222.5	-357	81	VDD	-4122.5	-357	141	D15	977.5	-357
22	V4R	-9137.5	-357	82	VDD	-4037.5	-357	142	D15	1062.5	-357
23	SHIELDING[6]	-9052.5	-357	83	VDD	-3952.5	-357	143	D14	1147.5	-357
24	V5R	-8967.5	-357	84	VDD	-3867.5	-357	144	D14	1232.5	-357
25	V5R	-8882.5	-357	85	TP3	-3782.5	-357	145	DASHD[11]	1317.5	-357
26	SHIELDING[7]	-8797.5	-357	86	DBGATE	-3697.5	-357	146	D13	1402.5	-357
27	V6R	-8712.5	-357	87	DBGATE	-3612.5	-357	147	D13	1487.5	-357
28	V6R	-8627.5	-357	88	CSX	-3527.5	-357	148	D12	1572.5	-357
29	SHIELDING[8]	-8542.5	-357	89	MASL	-3442.5	-357	149	D12	1657.5	-357
30	V7R	-8457.5	-357	90	MASL	-3357.5	-357	150	DASHD[12]	1742.5	-357
31	V7R	-8372.5	-357	91	SCL/DBCM[0]	-3272.5	-357	151	D11	1827.5	-357
32	SHIELDING[9]	-8287.5	-357	92	MASLOC	-3187.5	-357	152	D11	1912.5	-357
33	V8R	-8202.5	-357	93	MASLOC	-3102.5	-357	153	D10	1997.5	-357
34	V8R	-8117.5	-357	94	SDA/ DBCM[1]	-3017.5	-357	154	D10	2082.5	-357
35	SHIELDING[10]	-8032.5	-357	95	RES[0]	-2932.5	-357	155	DASHD[13]	2167.5	-357
36	V9R	-7947.5	-357	96	RES[0]	-2847.5	-357	156	D07	2252.5	-357
37	V9R	-7862.5	-357	97	CABC_PWM	-2762.5	-357	157	D07	2337.5	-357
38	SHIELDING[11]	-7777.5	-357	98	CABC_EN	-2677.5	-357	158	D06	2422.5	-357
39	V10R	-7692.5	-357	99	RES[1]	-2592.5	-357	159	D06	2507.5	-357
40	V10R	-7607.5	-357	100	RES[1]	-2507.5	-357	160	DASHD[14]	2592.5	-357
41	SHIELDING[12]	-7522.5	-357	101	DBC/3	-2422.5	-357	161	D05	2677.5	-357
42	V11R	-7437.5	-357	102	DBC/3	-2337.5	-357	162	D05	2762.5	-357
43	V11R	-7352.5	-357	103	DASHD[1]	-2252.5	-357	163	D04	2847.5	-357
44	SHIELDING[13]	-7267.5	-357	104	VSD	-2167.5	-357	164	D04	2932.5	-357
45	V12R	-7182.5	-357	105	VSD	-2082.5	-357	165	DASHD[15]	3017.5	-357
46	V12R	-7097.5	-357	106	DASHD[2]	-1997.5	-357	166	D03	3102.5	-357
47	SHIELDING[14]	-7012.5	-357	107	HSD	-1912.5	-357	167	D03	3187.5	-357
48	V13R	-6927.5	-357	108	HSD	-1827.5	-357	168	D02	3272.5	-357
49	V13R	-6842.5	-357	109	DASHD[3]	-1742.5	-357	169	D02	3357.5	-357
50	SHIELDING[15]	-6757.5	-357	110	DEN	-1657.5	-357	170	DASHD[16]	3442.5	-357
51	V14R	-6672.5	-357	111	DEN	-1572.5	-357	171	D01	3527.5	-357
52	V14R	-6587.5	-357	112	DASHD[4]	-1487.5	-357	172	D01	3612.5	-357
53	SHIELDING[16]	-6502.5	-357	113	CLKIN	-1402.5	-357	173	D00	3697.5	-357
54	TP0	-6417.5	-357	114	CLKIN	-1317.5	-357	174	D00	3782.5	-357
55	SHIELDING[17]	-6332.5	-357	115	DASHD[5]	-1232.5	-357	175	DASHD[17]	3867.5	-357
56	SHIELDING[18]	-6247.5	-357	116	D27	-1147.5	-357	176	SHIELDING[31]	3952.5	-357
57	SHIELDING[19]	-6162.5	-357	117	D27	-1062.5	-357	177	MODE	4037.5	-357
58	SHIELDING[20]	-6077.5	-357	118	D26	-977.5	-357	178	MODE	4122.5	-357
59	REV(TP5)	-5992.5	-357	119	D26	-892.5	-357	179	CLKPOL	4207.5	-357
60	BIST	-5907.5	-357	120	DASHD[6]	-807.5	-357	180	CLKPOL	4292.5	-357

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number	pad name	x	y
181	SHIELDING[32]	4377.5	-357
182	DITHB	4462.5	-357
183	DITHB	4547.5	-357
184	SHIELDING[33]	4632.5	-357
185	SHLR	4717.5	-357
186	SHLR	4802.5	-357
187	SHIELDING[34]	4887.5	-357
188	UPDN	4972.5	-357
189	UPDN	5057.5	-357
190	SHIELDING[35]	5142.5	-357
191	STBYB	5227.5	-357
192	STBYB	5312.5	-357
193	SHIELDING[36]	5397.5	-357
194	RSTB	5482.5	-357
195	RSTB	5567.5	-357
196	SHIELDING[37]	5652.5	-357
197	VDD	5737.5	-357
198	VDD	5822.5	-357
199	VDD	5907.5	-357
200	VDD	5992.5	-357
201	CAS	6077.5	-357
202	GND	6162.5	-357
203	GND	6247.5	-357
204	GND	6332.5	-357
205	GND	6417.5	-357
206	TP2	6502.5	-357
207	V14L	6587.5	-357
208	V14L	6672.5	-357
209	SHIELDING[38]	6757.5	-357
210	V13L	6842.5	-357
211	V13L	6927.5	-357
212	SHIELDING[39]	7012.5	-357
213	V12L	7097.5	-357
214	V12L	7182.5	-357
215	SHIELDING[40]	7267.5	-357
216	V11L	7352.5	-357
217	V11L	7437.5	-357
218	SHIELDING[41]	7522.5	-357
219	V10L	7607.5	-357
220	V10L	7692.5	-357
221	SHIELDING[42]	7777.5	-357
222	V9L	7862.5	-357
223	V9L	7947.5	-357
224	SHIELDING[43]	8032.5	-357
225	V8L	8117.5	-357
226	V8L	8202.5	-357
227	SHIELDING[44]	8287.5	-357
228	V7L	8372.5	-357
229	V7L	8457.5	-357
230	SHIELDING[45]	8542.5	-357
231	V6L	8627.5	-357
232	V6L	8712.5	-357
233	SHIELDING[46]	8797.5	-357
234	V5L	8882.5	-357
235	V5L	8967.5	-357
236	SHIELDING[47]	9052.5	-357
237	V4L	9137.5	-357
238	V4L	9222.5	-357
239	SHIELDING[48]	9307.5	-357
240	V3L	9392.5	-357

number	pad name	x	y
241	V3L	9477.5	-357
242	SHIELDING[49]	9562.5	-357
243	V2L	9647.5	-357
244	V2L	9732.5	-357
245	SHIELDING[50]	9817.5	-357
246	V1L	9902.5	-357
247	V1L	9987.5	-357
248	SHIELDING[51]	10072.5	-357
249	AVDD	10157.5	-357
250	AVDD	10242.5	-357
251	AVDD	10327.5	-357
252	AVDD	10412.5	-357
253	TP1	10497.5	-357
254	COM2_B	10582.5	-357
255	COM2_B	10667.5	-357
256	SHIELDING[52]	10752.5	-357
257	SHIELDING[53]	10837.5	-357
258	SHIELDING[54]	10922.5	-357
259	DCLKL	11049	-363
260	DIOL	11179	-323
261	DATL[17]	11049	-283
262	DATL[16]	11179	-243
263	DATL[15]	11049	-203
264	DATL[14]	11179	-163
265	DATL[13]	11049	-123
266	DATL[12]	11179	-83
267	DATL[11]	11049	-43
268	DATL[10]	11179	-3
269	DATL[9]	11049	37
270	DATL[8]	11179	77
271	DATL[7]	11049	117
272	DATL[6]	11179	157
273	DATL[5]	11049	197
274	DATL[4]	11179	237
275	DATL[3]	11049	277
276	DATL[2]	11179	317
277	DATL[1]	11049	357
278	DATL[0]	11179	397
279	POLL	10914	377
280	LDL	10864	377
281	SYNCL	10814	377
282	COM2_T	10764	377
283	COM2_T	10714	377
284	SHIELDING[55]	10664	377
285	S[1]	10620.5	77
286	S[2]	10603.5	217
287	S[3]	10586.5	357
288	S[4]	10569.5	77
289	S[5]	10552.5	217
290	S[6]	10535.5	357
291	S[7]	10518.5	77
292	S[8]	10501.5	217
293	S[9]	10484.5	357
294	S[10]	10467.5	77
295	S[11]	10450.5	217
296	S[12]	10433.5	357
297	S[13]	10416.5	77
298	S[14]	10399.5	217
299	S[15]	10382.5	357
300	S[16]	10365.5	77

number	pad name	x	y
301	S[17]	10348.5	217
302	S[18]	10331.5	357
303	S[19]	10314.5	77
304	S[20]	10297.5	217
305	S[21]	10280.5	357
306	S[22]	10263.5	77
307	S[23]	10246.5	217
308	S[24]	10229.5	357
309	S[25]	10212.5	77
310	S[26]	10195.5	217
311	S[27]	10178.5	357
312	S[28]	10161.5	77
313	S[29]	10144.5	217
314	S[30]	10127.5	357
315	S[31]	10110.5	77
316	S[32]	10093.5	217
317	S[33]	10076.5	357
318	S[34]	10059.5	77
319	S[35]	10042.5	217
320	S[36]	10025.5	357
321	S[37]	10008.5	77
322	S[38]	9991.5	217
323	S[39]	9974.5	357
324	S[40]	9957.5	77
325	S[41]	9940.5	217
326	S[42]	9923.5	357
327	S[43]	9906.5	77
328	S[44]	9889.5	217
329	S[45]	9872.5	357
330	S[46]	9855.5	77
331	S[47]	9838.5	217
332	S[48]	9821.5	357
333	S[49]	9804.5	77
334	S[50]	9787.5	217
335	S[51]	9770.5	357
336	S[52]	9753.5	77
337	S[53]	9736.5	217
338	S[54]	9719.5	357
339	S[55]	9702.5	77
340	S[56]	9685.5	217
341	S[57]	9668.5	357
342	S[58]	9651.5	77
343	S[59]	9634.5	217
344	S[60]	9617.5	357
345	S[61]	9600.5	77
346	S[62]	9583.5	217
347	S[63]	9566.5	357
348	S[64]	9549.5	77
349	S[65]	9532.5	217
350	S[66]	9515.5	357
351	S[67]	9498.5	77
352	S[68]	9481.5	217
353	S[69]	9464.5	357
354	S[70]	9447.5	77
355	S[71]	9430.5	217
356	S[72]	9413.5	357
357	S[73]	9396.5	77
358	S[74]	9379.5	217
359	S[75]	9362.5	357
360	S[76]	9345.5	77

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number	pad name	x	y
361	S[77]	9328.5	217
362	S[78]	9311.5	357
363	S[79]	9294.5	77
364	S[80]	9277.5	217
365	S[81]	9260.5	357
366	S[82]	9243.5	77
367	S[83]	9226.5	217
368	S[84]	9209.5	357
369	S[85]	9192.5	77
370	S[86]	9175.5	217
371	S[87]	9158.5	357
372	S[88]	9141.5	77
373	S[89]	9124.5	217
374	S[90]	9107.5	357
375	S[91]	9090.5	77
376	S[92]	9073.5	217
377	S[93]	9056.5	357
378	S[94]	9039.5	77
379	S[95]	9022.5	217
380	S[96]	9005.5	357
381	S[97]	8988.5	77
382	S[98]	8971.5	217
383	S[99]	8954.5	357
384	S[100]	8937.5	77
385	S[101]	8920.5	217
386	S[102]	8903.5	357
387	S[103]	8886.5	77
388	S[104]	8869.5	217
389	S[105]	8852.5	357
390	S[106]	8835.5	77
391	S[107]	8818.5	217
392	S[108]	8801.5	357
393	S[109]	8784.5	77
394	S[110]	8767.5	217
395	S[111]	8750.5	357
396	S[112]	8733.5	77
397	S[113]	8716.5	217
398	S[114]	8699.5	357
399	S[115]	8682.5	77
400	S[116]	8665.5	217
401	S[117]	8648.5	357
402	S[118]	8631.5	77
403	S[119]	8614.5	217
404	S[120]	8597.5	357
405	S[121]	8580.5	77
406	S[122]	8563.5	217
407	S[123]	8546.5	357
408	S[124]	8529.5	77
409	S[125]	8512.5	217
410	S[126]	8495.5	357
411	S[127]	8478.5	77
412	S[128]	8461.5	217
413	S[129]	8444.5	357
414	S[130]	8427.5	77
415	S[131]	8410.5	217
416	S[132]	8393.5	357
417	S[133]	8376.5	77
418	S[134]	8359.5	217
419	S[135]	8342.5	357
420	S[136]	8325.5	77

number	pad name	x	y
421	S[137]	8308.5	217
422	S[138]	8291.5	357
423	S[139]	8274.5	77
424	S[140]	8257.5	217
425	S[141]	8240.5	357
426	S[142]	8223.5	77
427	S[143]	8206.5	217
428	S[144]	8189.5	357
429	S[145]	8172.5	77
430	S[146]	8155.5	217
431	S[147]	8138.5	357
432	S[148]	8121.5	77
433	S[149]	8104.5	217
434	S[150]	8087.5	357
435	S[151]	8070.5	77
436	S[152]	8053.5	217
437	S[153]	8036.5	357
438	S[154]	8019.5	77
439	S[155]	8002.5	217
440	S[156]	7985.5	357
441	S[157]	7968.5	77
442	S[158]	7951.5	217
443	S[159]	7934.5	357
444	S[160]	7917.5	77
445	S[161]	7900.5	217
446	S[162]	7883.5	357
447	S[163]	7866.5	77
448	S[164]	7849.5	217
449	S[165]	7832.5	357
450	S[166]	7815.5	77
451	S[167]	7798.5	217
452	S[168]	7781.5	357
453	S[169]	7764.5	77
454	S[170]	7747.5	217
455	S[171]	7730.5	357
456	S[172]	7713.5	77
457	S[173]	7696.5	217
458	S[174]	7679.5	357
459	S[175]	7662.5	77
460	S[176]	7645.5	217
461	S[177]	7628.5	357
462	S[178]	7611.5	77
463	S[179]	7594.5	217
464	S[180]	7577.5	357
465	S[181]	7560.5	77
466	S[182]	7543.5	217
467	S[183]	7526.5	357
468	S[184]	7509.5	77
469	S[185]	7492.5	217
470	S[186]	7475.5	357
471	S[187]	7458.5	77
472	S[188]	7441.5	217
473	S[189]	7424.5	357
474	S[190]	7407.5	77
475	S[191]	7390.5	217
476	S[192]	7373.5	357
477	S[193]	7356.5	77
478	S[194]	7339.5	217
479	S[195]	7322.5	357
480	S[196]	7305.5	77

number	pad name	x	y
481	S[197]	7288.5	217
482	S[198]	7271.5	357
483	S[199]	7254.5	77
484	S[200]	7237.5	217
485	S[201]	7220.5	357
486	S[202]	7203.5	77
487	S[203]	7186.5	217
488	S[204]	7169.5	357
489	S[205]	7152.5	77
490	S[206]	7135.5	217
491	S[207]	7118.5	357
492	S[208]	7101.5	77
493	S[209]	7084.5	217
494	S[210]	7067.5	357
495	S[211]	7050.5	77
496	S[212]	7033.5	217
497	S[213]	7016.5	357
498	S[214]	6999.5	77
499	S[215]	6982.5	217
500	S[216]	6965.5	357
501	S[217]	6948.5	77
502	S[218]	6931.5	217
503	S[219]	6914.5	357
504	S[220]	6897.5	77
505	S[221]	6880.5	217
506	S[222]	6863.5	357
507	S[223]	6846.5	77
508	S[224]	6829.5	217
509	S[225]	6812.5	357
510	S[226]	6795.5	77
511	S[227]	6778.5	217
512	S[228]	6761.5	357
513	S[229]	6744.5	77
514	S[230]	6727.5	217
515	S[231]	6710.5	357
516	S[232]	6693.5	77
517	S[233]	6676.5	217
518	S[234]	6659.5	357
519	S[235]	6642.5	77
520	S[236]	6625.5	217
521	S[237]	6608.5	357
522	S[238]	6591.5	77
523	S[239]	6574.5	217
524	S[240]	6557.5	357
525	S[241]	6540.5	77
526	S[242]	6523.5	217
527	S[243]	6506.5	357
528	S[244]	6489.5	77
529	S[245]	6472.5	217
530	S[246]	6455.5	357
531	S[247]	6438.5	77
532	S[248]	6421.5	217
533	S[249]	6404.5	357
534	S[250]	6387.5	77
535	S[251]	6370.5	217
536	S[252]	6353.5	357
537	S[253]	6336.5	77
538	S[254]	6319.5	217
539	S[255]	6302.5	357
540	S[256]	6285.5	77

ILITEK CONFIDENTIAL

number	pad name	x	y
541	S[257]	6268.5	217
542	S[258]	6251.5	357
543	S[259]	6234.5	77
544	S[260]	6217.5	217
545	S[261]	6200.5	357
546	S[262]	6183.5	77
547	S[263]	6166.5	217
548	S[264]	6149.5	357
549	S[265]	6132.5	77
550	S[266]	6115.5	217
551	S[267]	6098.5	357
552	S[268]	6081.5	77
553	S[269]	6064.5	217
554	S[270]	6047.5	357
555	S[271]	6030.5	77
556	S[272]	6013.5	217
557	S[273]	5996.5	357
558	S[274]	5979.5	77
559	S[275]	5962.5	217
560	S[276]	5945.5	357
561	S[277]	5928.5	77
562	S[278]	5911.5	217
563	S[279]	5894.5	357
564	S[280]	5877.5	77
565	S[281]	5860.5	217
566	S[282]	5843.5	357
567	S[283]	5826.5	77
568	S[284]	5809.5	217
569	S[285]	5792.5	357
570	S[286]	5775.5	77
571	S[287]	5758.5	217
572	S[288]	5741.5	357
573	S[289]	5724.5	77
574	S[290]	5707.5	217
575	S[291]	5690.5	357
576	S[292]	5673.5	77
577	S[293]	5656.5	217
578	S[294]	5639.5	357
579	S[295]	5622.5	77
580	S[296]	5605.5	217
581	S[297]	5588.5	357
582	S[298]	5571.5	77
583	S[299]	5554.5	217
584	S[300]	5537.5	357
585	S[301]	5520.5	77
586	S[302]	5503.5	217
587	S[303]	5486.5	357
588	S[304]	5469.5	77
589	S[305]	5452.5	217
590	S[306]	5435.5	357
591	S[307]	5418.5	77
592	S[308]	5401.5	217
593	S[309]	5384.5	357
594	S[310]	5367.5	77
595	S[311]	5350.5	217
596	S[312]	5333.5	357
597	S[313]	5316.5	77
598	S[314]	5299.5	217
599	S[315]	5282.5	357
600	S[316]	5265.5	77

number	pad name	x	y
601	S[317]	5248.5	217
602	S[318]	5231.5	357
603	S[319]	5214.5	77
604	S[320]	5197.5	217
605	S[321]	5180.5	357
606	S[322]	5163.5	77
607	S[323]	5146.5	217
608	S[324]	5129.5	357
609	S[325]	5112.5	77
610	S[326]	5095.5	217
611	S[327]	5078.5	357
612	S[328]	5061.5	77
613	S[329]	5044.5	217
614	S[330]	5027.5	357
615	S[331]	5010.5	77
616	S[332]	4993.5	217
617	S[333]	4976.5	357
618	S[334]	4959.5	77
619	S[335]	4942.5	217
620	S[336]	4925.5	357
621	S[337]	4908.5	77
622	S[338]	4891.5	217
623	S[339]	4874.5	357
624	S[340]	4857.5	77
625	S[341]	4840.5	217
626	S[342]	4823.5	357
627	S[343]	4806.5	77
628	S[344]	4789.5	217
629	S[345]	4772.5	357
630	S[346]	4755.5	77
631	S[347]	4738.5	217
632	S[348]	4721.5	357
633	S[349]	4704.5	77
634	S[350]	4687.5	217
635	S[351]	4670.5	357
636	S[352]	4653.5	77
637	S[353]	4636.5	217
638	S[354]	4619.5	357
639	S[355]	4602.5	77
640	S[356]	4585.5	217
641	S[357]	4568.5	357
642	S[358]	4551.5	77
643	S[359]	4534.5	217
644	S[360]	4517.5	357
645	S[361]	4500.5	77
646	S[362]	4483.5	217
647	S[363]	4466.5	357
648	S[364]	4449.5	77
649	S[365]	4432.5	217
650	S[366]	4415.5	357
651	S[367]	4398.5	77
652	S[368]	4381.5	217
653	S[369]	4364.5	357
654	S[370]	4347.5	77
655	S[371]	4330.5	217
656	S[372]	4313.5	357
657	S[373]	4296.5	77
658	S[374]	4279.5	217
659	S[375]	4262.5	357
660	S[376]	4245.5	77

number	pad name	x	y
661	S[377]	4228.5	217
662	S[378]	4211.5	357
663	S[379]	4194.5	77
664	S[380]	4177.5	217
665	S[381]	4160.5	357
666	S[382]	4143.5	77
667	S[383]	4126.5	217
668	S[384]	4109.5	357
669	S[385]	4092.5	77
670	S[386]	4075.5	217
671	S[387]	4058.5	357
672	S[388]	4041.5	77
673	S[389]	4024.5	217
674	S[390]	4007.5	357
675	S[391]	3990.5	77
676	S[392]	3973.5	217
677	S[393]	3956.5	357
678	S[394]	3939.5	77
679	S[395]	3922.5	217
680	S[396]	3905.5	357
681	S[397]	3888.5	77
682	S[398]	3871.5	217
683	S[399]	3854.5	357
684	S[400]	3837.5	77
685	S[401]	3820.5	217
686	S[402]	3803.5	357
687	S[403]	3786.5	77
688	S[404]	3769.5	217
689	S[405]	3752.5	357
690	S[406]	3735.5	77
691	S[407]	3718.5	217
692	S[408]	3701.5	357
693	S[409]	3684.5	77
694	S[410]	3667.5	217
695	S[411]	3650.5	357
696	S[412]	3633.5	77
697	S[413]	3616.5	217
698	S[414]	3599.5	357
699	S[415]	3582.5	77
700	S[416]	3565.5	217
701	S[417]	3548.5	357
702	S[418]	3531.5	77
703	S[419]	3514.5	217
704	S[420]	3497.5	357
705	S[421]	3480.5	77
706	S[422]	3463.5	217
707	S[423]	3446.5	357
708	S[424]	3429.5	77
709	S[425]	3412.5	217
710	S[426]	3395.5	357
711	S[427]	3378.5	77
712	S[428]	3361.5	217
713	S[429]	3344.5	357
714	S[430]	3327.5	77
715	S[431]	3310.5	217
716	S[432]	3293.5	357
717	S[433]	3276.5	77
718	S[434]	3259.5	217
719	S[435]	3242.5	357
720	S[436]	3225.5	77

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number	pad name	x	y
721	S[437]	3208.5	217
722	S[438]	3191.5	357
723	S[439]	3174.5	77
724	S[440]	3157.5	217
725	S[441]	3140.5	357
726	S[442]	3123.5	77
727	S[443]	3106.5	217
728	S[444]	3089.5	357
729	S[445]	3072.5	77
730	S[446]	3055.5	217
731	S[447]	3038.5	357
732	S[448]	3021.5	77
733	S[449]	3004.5	217
734	S[450]	2987.5	357
735	S[451]	2970.5	77
736	S[452]	2953.5	217
737	S[453]	2936.5	357
738	S[454]	2919.5	77
739	S[455]	2902.5	217
740	S[456]	2885.5	357
741	S[457]	2868.5	77
742	S[458]	2851.5	217
743	S[459]	2834.5	357
744	S[460]	2817.5	77
745	S[461]	2800.5	217
746	S[462]	2783.5	357
747	S[463]	2766.5	77
748	S[464]	2749.5	217
749	S[465]	2732.5	357
750	S[466]	2715.5	77
751	S[467]	2698.5	217
752	S[468]	2681.5	357
753	S[469]	2664.5	77
754	S[470]	2647.5	217
755	S[471]	2630.5	357
756	S[472]	2613.5	77
757	S[473]	2596.5	217
758	S[474]	2579.5	357
759	S[475]	2562.5	77
760	S[476]	2545.5	217
761	S[477]	2528.5	357
762	S[478]	2511.5	77
763	S[479]	2494.5	217
764	S[480]	2477.5	357
765	S[481]	2460.5	77
766	S[482]	2443.5	217
767	S[483]	2426.5	357
768	S[484]	2409.5	77
769	S[485]	2392.5	217
770	S[486]	2375.5	357
771	S[487]	2358.5	77
772	S[488]	2341.5	217
773	S[489]	2324.5	357
774	S[490]	2307.5	77
775	S[491]	2290.5	217
776	S[492]	2273.5	357
777	S[493]	2256.5	77
778	S[494]	2239.5	217
779	S[495]	2222.5	357
780	S[496]	2205.5	77

number	pad name	x	y
781	S[497]	2188.5	217
782	S[498]	2171.5	357
783	S[499]	2154.5	77
784	S[500]	2137.5	217
785	S[501]	2120.5	357
786	S[502]	2103.5	77
787	S[503]	2086.5	217
788	S[504]	2069.5	357
789	S[505]	2052.5	77
790	S[506]	2035.5	217
791	S[507]	2018.5	357
792	S[508]	2001.5	77
793	S[509]	1984.5	217
794	S[510]	1967.5	357
795	S[511]	1950.5	77
796	S[512]	1933.5	217
797	S[513]	1916.5	357
798	S[514]	1899.5	77
799	S[515]	1882.5	217
800	S[516]	1865.5	357
801	S[517]	1848.5	77
802	S[518]	1831.5	217
803	S[519]	1814.5	357
804	S[520]	1797.5	77
805	S[521]	1780.5	217
806	S[522]	1763.5	357
807	S[523]	1746.5	77
808	S[524]	1729.5	217
809	S[525]	1712.5	357
810	S[526]	1695.5	77
811	S[527]	1678.5	217
812	S[528]	1661.5	357
813	S[529]	1644.5	77
814	S[530]	1627.5	217
815	S[531]	1610.5	357
816	S[532]	1593.5	77
817	S[533]	1576.5	217
818	S[534]	1559.5	357
819	S[535]	1542.5	77
820	S[536]	1525.5	217
821	S[537]	1508.5	357
822	S[538]	1491.5	77
823	S[539]	1474.5	217
824	S[540]	1457.5	357
825	S[541]	1440.5	77
826	S[542]	1423.5	217
827	S[543]	1406.5	357
828	S[544]	1389.5	77
829	S[545]	1372.5	217
830	S[546]	1355.5	357
831	S[547]	1338.5	77
832	S[548]	1321.5	217
833	S[549]	1304.5	357
834	S[550]	1287.5	77
835	S[551]	1270.5	217
836	S[552]	1253.5	357
837	S[553]	1236.5	77
838	S[554]	1219.5	217
839	S[555]	1202.5	357
840	S[556]	1185.5	77

number	pad name	x	y
841	S[557]	1168.5	217
842	S[558]	1151.5	357
843	S[559]	1134.5	77
844	S[560]	1117.5	217
845	S[561]	1100.5	357
846	S[562]	1083.5	77
847	S[563]	1066.5	217
848	S[564]	1049.5	357
849	S[565]	1032.5	77
850	S[566]	1015.5	217
851	S[567]	998.5	357
852	S[568]	981.5	77
853	S[569]	964.5	217
854	S[570]	947.5	357
855	S[571]	930.5	77
856	S[572]	913.5	217
857	S[573]	896.5	357
858	S[574]	879.5	77
859	S[575]	862.5	217
860	S[576]	845.5	357
861	S[577]	828.5	77
862	S[578]	811.5	217
863	S[579]	794.5	357
864	S[580]	777.5	77
865	S[581]	760.5	217
866	S[582]	743.5	357
867	S[583]	726.5	77
868	S[584]	709.5	217
869	S[585]	692.5	357
870	S[586]	675.5	77
871	S[587]	658.5	217
872	S[588]	641.5	357
873	S[589]	624.5	77
874	S[590]	607.5	217
875	S[591]	590.5	357
876	S[592]	573.5	77
877	S[593]	556.5	217
878	S[594]	539.5	357
879	S[595]	522.5	77
880	S[596]	505.5	217
881	S[597]	488.5	357
882	S[598]	471.5	77
883	S[599]	454.5	217
884	S[600]	437.5	357
885	SHIELDING[56]	403.5	357
886	SHIELDING[57]	369.5	357
887	SHIELDING[58]	335.5	357
888	SHIELDING[59]	301.5	357
889	SHIELDING[60]	267.5	357
890	SHIELDING[61]	233.5	357
891	SHIELDING[62]	-233.5	357
892	SHIELDING[63]	-267.5	357
893	SHIELDING[64]	-301.5	357
894	SHIELDING[65]	-335.5	357
895	SHIELDING[66]	-369.5	357
896	SHIELDING[67]	-403.5	357
897	S[601]	-437.5	357
898	S[602]	-454.5	217
899	S[603]	-471.5	77
900	S[604]	-488.5	357

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number	pad name	x	y
901	S[605]	-505.5	217
902	S[606]	-522.5	77
903	S[607]	-539.5	357
904	S[608]	-556.5	217
905	S[609]	-573.5	77
906	S[610]	-590.5	357
907	S[611]	-607.5	217
908	S[612]	-624.5	77
909	S[613]	-641.5	357
910	S[614]	-658.5	217
911	S[615]	-675.5	77
912	S[616]	-692.5	357
913	S[617]	-709.5	217
914	S[618]	-726.5	77
915	S[619]	-743.5	357
916	S[620]	-760.5	217
917	S[621]	-777.5	77
918	S[622]	-794.5	357
919	S[623]	-811.5	217
920	S[624]	-828.5	77
921	S[625]	-845.5	357
922	S[626]	-862.5	217
923	S[627]	-879.5	77
924	S[628]	-896.5	357
925	S[629]	-913.5	217
926	S[630]	-930.5	77
927	S[631]	-947.5	357
928	S[632]	-964.5	217
929	S[633]	-981.5	77
930	S[634]	-998.5	357
931	S[635]	-1015.5	217
932	S[636]	-1032.5	77
933	S[637]	-1049.5	357
934	S[638]	-1066.5	217
935	S[639]	-1083.5	77
936	S[640]	-1100.5	357
937	S[641]	-1117.5	217
938	S[642]	-1134.5	77
939	S[643]	-1151.5	357
940	S[644]	-1168.5	217
941	S[645]	-1185.5	77
942	S[646]	-1202.5	357
943	S[647]	-1219.5	217
944	S[648]	-1236.5	77
945	S[649]	-1253.5	357
946	S[650]	-1270.5	217
947	S[651]	-1287.5	77
948	S[652]	-1304.5	357
949	S[653]	-1321.5	217
950	S[654]	-1338.5	77
951	S[655]	-1355.5	357
952	S[656]	-1372.5	217
953	S[657]	-1389.5	77
954	S[658]	-1406.5	357
955	S[659]	-1423.5	217
956	S[660]	-1440.5	77
957	S[661]	-1457.5	357
958	S[662]	-1474.5	217
959	S[663]	-1491.5	77
960	S[664]	-1508.5	357

number	pad name	x	y
961	S[665]	-1525.5	217
962	S[666]	-1542.5	77
963	S[667]	-1559.5	357
964	S[668]	-1576.5	217
965	S[669]	-1593.5	77
966	S[670]	-1610.5	357
967	S[671]	-1627.5	217
968	S[672]	-1644.5	77
969	S[673]	-1661.5	357
970	S[674]	-1678.5	217
971	S[675]	-1695.5	77
972	S[676]	-1712.5	357
973	S[677]	-1729.5	217
974	S[678]	-1746.5	77
975	S[679]	-1763.5	357
976	S[680]	-1780.5	217
977	S[681]	-1797.5	77
978	S[682]	-1814.5	357
979	S[683]	-1831.5	217
980	S[684]	-1848.5	77
981	S[685]	-1865.5	357
982	S[686]	-1882.5	217
983	S[687]	-1899.5	77
984	S[688]	-1916.5	357
985	S[689]	-1933.5	217
986	S[690]	-1950.5	77
987	S[691]	-1967.5	357
988	S[692]	-1984.5	217
989	S[693]	-2001.5	77
990	S[694]	-2018.5	357
991	S[695]	-2035.5	217
992	S[696]	-2052.5	77
993	S[697]	-2069.5	357
994	S[698]	-2086.5	217
995	S[699]	-2103.5	77
996	S[700]	-2120.5	357
997	S[701]	-2137.5	217
998	S[702]	-2154.5	77
999	S[703]	-2171.5	357
1000	S[704]	-2188.5	217
1001	S[705]	-2205.5	77
1002	S[706]	-2222.5	357
1003	S[707]	-2239.5	217
1004	S[708]	-2256.5	77
1005	S[709]	-2273.5	357
1006	S[710]	-2290.5	217
1007	S[711]	-2307.5	77
1008	S[712]	-2324.5	357
1009	S[713]	-2341.5	217
1010	S[714]	-2358.5	77
1011	S[715]	-2375.5	357
1012	S[716]	-2392.5	217
1013	S[717]	-2409.5	77
1014	S[718]	-2426.5	357
1015	S[719]	-2443.5	217
1016	S[720]	-2460.5	77
1017	S[721]	-2477.5	357
1018	S[722]	-2494.5	217
1019	S[723]	-2511.5	77
1020	S[724]	-2528.5	357

number	pad name	x	y
1021	S[725]	-2545.5	217
1022	S[726]	-2562.5	77
1023	S[727]	-2579.5	357
1024	S[728]	-2596.5	217
1025	S[729]	-2613.5	77
1026	S[730]	-2630.5	357
1027	S[731]	-2647.5	217
1028	S[732]	-2664.5	77
1029	S[733]	-2681.5	357
1030	S[734]	-2698.5	217
1031	S[735]	-2715.5	77
1032	S[736]	-2732.5	357
1033	S[737]	-2749.5	217
1034	S[738]	-2766.5	77
1035	S[739]	-2783.5	357
1036	S[740]	-2800.5	217
1037	S[741]	-2817.5	77
1038	S[742]	-2834.5	357
1039	S[743]	-2851.5	217
1040	S[744]	-2868.5	77
1041	S[745]	-2885.5	357
1042	S[746]	-2902.5	217
1043	S[747]	-2919.5	77
1044	S[748]	-2936.5	357
1045	S[749]	-2953.5	217
1046	S[750]	-2970.5	77
1047	S[751]	-2987.5	357
1048	S[752]	-3004.5	217
1049	S[753]	-3021.5	77
1050	S[754]	-3038.5	357
1051	S[755]	-3055.5	217
1052	S[756]	-3072.5	77
1053	S[757]	-3089.5	357
1054	S[758]	-3106.5	217
1055	S[759]	-3123.5	77
1056	S[760]	-3140.5	357
1057	S[761]	-3157.5	217
1058	S[762]	-3174.5	77
1059	S[763]	-3191.5	357
1060	S[764]	-3208.5	217
1061	S[765]	-3225.5	77
1062	S[766]	-3242.5	357
1063	S[767]	-3259.5	217
1064	S[768]	-3276.5	77
1065	S[769]	-3293.5	357
1066	S[770]	-3310.5	217
1067	S[771]	-3327.5	77
1068	S[772]	-3344.5	357
1069	S[773]	-3361.5	217
1070	S[774]	-3378.5	77
1071	S[775]	-3395.5	357
1072	S[776]	-3412.5	217
1073	S[777]	-3429.5	77
1074	S[778]	-3446.5	357
1075	S[779]	-3463.5	217
1076	S[780]	-3480.5	77
1077	S[781]	-3497.5	357
1078	S[782]	-3514.5	217
1079	S[783]	-3531.5	77
1080	S[784]	-3548.5	357

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number	pad name	x	y
1081	S[785]	-3565.5	217
1082	S[786]	-3582.5	77
1083	S[787]	-3599.5	357
1084	S[788]	-3616.5	217
1085	S[789]	-3633.5	77
1086	S[790]	-3650.5	357
1087	S[791]	-3667.5	217
1088	S[792]	-3684.5	77
1089	S[793]	-3701.5	357
1090	S[794]	-3718.5	217
1091	S[795]	-3735.5	77
1092	S[796]	-3752.5	357
1093	S[797]	-3769.5	217
1094	S[798]	-3786.5	77
1095	S[799]	-3803.5	357
1096	S[800]	-3820.5	217
1097	S[801]	-3837.5	77
1098	S[802]	-3854.5	357
1099	S[803]	-3871.5	217
1100	S[804]	-3888.5	77
1101	S[805]	-3905.5	357
1102	S[806]	-3922.5	217
1103	S[807]	-3939.5	77
1104	S[808]	-3956.5	357
1105	S[809]	-3973.5	217
1106	S[810]	-3990.5	77
1107	S[811]	-4007.5	357
1108	S[812]	-4024.5	217
1109	S[813]	-4041.5	77
1110	S[814]	-4058.5	357
1111	S[815]	-4075.5	217
1112	S[816]	-4092.5	77
1113	S[817]	-4109.5	357
1114	S[818]	-4126.5	217
1115	S[819]	-4143.5	77
1116	S[820]	-4160.5	357
1117	S[821]	-4177.5	217
1118	S[822]	-4194.5	77
1119	S[823]	-4211.5	357
1120	S[824]	-4228.5	217
1121	S[825]	-4245.5	77
1122	S[826]	-4262.5	357
1123	S[827]	-4279.5	217
1124	S[828]	-4296.5	77
1125	S[829]	-4313.5	357
1126	S[830]	-4330.5	217
1127	S[831]	-4347.5	77
1128	S[832]	-4364.5	357
1129	S[833]	-4381.5	217
1130	S[834]	-4398.5	77
1131	S[835]	-4415.5	357
1132	S[836]	-4432.5	217
1133	S[837]	-4449.5	77
1134	S[838]	-4466.5	357
1135	S[839]	-4483.5	217
1136	S[840]	-4500.5	77
1137	S[841]	-4517.5	357
1138	S[842]	-4534.5	217
1139	S[843]	-4551.5	77
1140	S[844]	-4568.5	357

number	pad name	x	y
1141	S[845]	-4585.5	217
1142	S[846]	-4602.5	77
1143	S[847]	-4619.5	357
1144	S[848]	-4636.5	217
1145	S[849]	-4653.5	77
1146	S[850]	-4670.5	357
1147	S[851]	-4687.5	217
1148	S[852]	-4704.5	77
1149	S[853]	-4721.5	357
1150	S[854]	-4738.5	217
1151	S[855]	-4755.5	77
1152	S[856]	-4772.5	357
1153	S[857]	-4789.5	217
1154	S[858]	-4806.5	77
1155	S[859]	-4823.5	357
1156	S[860]	-4840.5	217
1157	S[861]	-4857.5	77
1158	S[862]	-4874.5	357
1159	S[863]	-4891.5	217
1160	S[864]	-4908.5	77
1161	S[865]	-4925.5	357
1162	S[866]	-4942.5	217
1163	S[867]	-4959.5	77
1164	S[868]	-4976.5	357
1165	S[869]	-4993.5	217
1166	S[870]	-5010.5	77
1167	S[871]	-5027.5	357
1168	S[872]	-5044.5	217
1169	S[873]	-5061.5	77
1170	S[874]	-5078.5	357
1171	S[875]	-5095.5	217
1172	S[876]	-5112.5	77
1173	S[877]	-5129.5	357
1174	S[878]	-5146.5	217
1175	S[879]	-5163.5	77
1176	S[880]	-5180.5	357
1177	S[881]	-5197.5	217
1178	S[882]	-5214.5	77
1179	S[883]	-5231.5	357
1180	S[884]	-5248.5	217
1181	S[885]	-5265.5	77
1182	S[886]	-5282.5	357
1183	S[887]	-5299.5	217
1184	S[888]	-5316.5	77
1185	S[889]	-5333.5	357
1186	S[890]	-5350.5	217
1187	S[891]	-5367.5	77
1188	S[892]	-5384.5	357
1189	S[893]	-5401.5	217
1190	S[894]	-5418.5	77
1191	S[895]	-5435.5	357
1192	S[896]	-5452.5	217
1193	S[897]	-5469.5	77
1194	S[898]	-5486.5	357
1195	S[899]	-5503.5	217
1196	S[900]	-5520.5	77
1197	S[901]	-5537.5	357
1198	S[902]	-5554.5	217
1199	S[903]	-5571.5	77
1200	S[904]	-5588.5	357

number	pad name	x	y
1201	S[905]	-5605.5	217
1202	S[906]	-5622.5	77
1203	S[907]	-5639.5	357
1204	S[908]	-5656.5	217
1205	S[909]	-5673.5	77
1206	S[910]	-5690.5	357
1207	S[911]	-5707.5	217
1208	S[912]	-5724.5	77
1209	S[913]	-5741.5	357
1210	S[914]	-5758.5	217
1211	S[915]	-5775.5	77
1212	S[916]	-5792.5	357
1213	S[917]	-5809.5	217
1214	S[918]	-5826.5	77
1215	S[919]	-5843.5	357
1216	S[920]	-5860.5	217
1217	S[921]	-5877.5	77
1218	S[922]	-5894.5	357
1219	S[923]	-5911.5	217
1220	S[924]	-5928.5	77
1221	S[925]	-5945.5	357
1222	S[926]	-5962.5	217
1223	S[927]	-5979.5	77
1224	S[928]	-5996.5	357
1225	S[929]	-6013.5	217
1226	S[930]	-6030.5	77
1227	S[931]	-6047.5	357
1228	S[932]	-6064.5	217
1229	S[933]	-6081.5	77
1230	S[934]	-6098.5	357
1231	S[935]	-6115.5	217
1232	S[936]	-6132.5	77
1233	S[937]	-6149.5	357
1234	S[938]	-6166.5	217
1235	S[939]	-6183.5	77
1236	S[940]	-6200.5	357
1237	S[941]	-6217.5	217
1238	S[942]	-6234.5	77
1239	S[943]	-6251.5	357
1240	S[944]	-6268.5	217
1241	S[945]	-6285.5	77
1242	S[946]	-6302.5	357
1243	S[947]	-6319.5	217
1244	S[948]	-6336.5	77
1245	S[949]	-6353.5	357
1246	S[950]	-6370.5	217
1247	S[951]	-6387.5	77
1248	S[952]	-6404.5	357
1249	S[953]	-6421.5	217
1250	S[954]	-6438.5	77
1251	S[955]	-6455.5	357
1252	S[956]	-6472.5	217
1253	S[957]	-6489.5	77
1254	S[958]	-6506.5	357
1255	S[959]	-6523.5	217
1256	S[960]	-6540.5	77
1257	S[961]	-6557.5	357
1258	S[962]	-6574.5	217
1259	S[963]	-6591.5	77
1260	S[964]	-6608.5	357

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number	pad name	x	y
1261	S[965]	-6625.5	217
1262	S[966]	-6642.5	77
1263	S[967]	-6659.5	357
1264	S[968]	-6676.5	217
1265	S[969]	-6693.5	77
1266	S[970]	-6710.5	357
1267	S[971]	-6727.5	217
1268	S[972]	-6744.5	77
1269	S[973]	-6761.5	357
1270	S[974]	-6778.5	217
1271	S[975]	-6795.5	77
1272	S[976]	-6812.5	357
1273	S[977]	-6829.5	217
1274	S[978]	-6846.5	77
1275	S[979]	-6863.5	357
1276	S[980]	-6880.5	217
1277	S[981]	-6897.5	77
1278	S[982]	-6914.5	357
1279	S[983]	-6931.5	217
1280	S[984]	-6948.5	77
1281	S[985]	-6965.5	357
1282	S[986]	-6982.5	217
1283	S[987]	-6999.5	77
1284	S[988]	-7016.5	357
1285	S[989]	-7033.5	217
1286	S[990]	-7050.5	77
1287	S[991]	-7067.5	357
1288	S[992]	-7084.5	217
1289	S[993]	-7101.5	77
1290	S[994]	-7118.5	357
1291	S[995]	-7135.5	217
1292	S[996]	-7152.5	77
1293	S[997]	-7169.5	357
1294	S[998]	-7186.5	217
1295	S[999]	-7203.5	77
1296	S[1000]	-7220.5	357
1297	S[1001]	-7237.5	217
1298	S[1002]	-7254.5	77
1299	S[1003]	-7271.5	357
1300	S[1004]	-7288.5	217
1301	S[1005]	-7305.5	77
1302	S[1006]	-7322.5	357
1303	S[1007]	-7339.5	217
1304	S[1008]	-7356.5	77
1305	S[1009]	-7373.5	357
1306	S[1010]	-7390.5	217
1307	S[1011]	-7407.5	77
1308	S[1012]	-7424.5	357
1309	S[1013]	-7441.5	217
1310	S[1014]	-7458.5	77
1311	S[1015]	-7475.5	357
1312	S[1016]	-7492.5	217
1313	S[1017]	-7509.5	77
1314	S[1018]	-7526.5	357
1315	S[1019]	-7543.5	217
1316	S[1020]	-7560.5	77
1317	S[1021]	-7577.5	357
1318	S[1022]	-7594.5	217
1319	S[1023]	-7611.5	77
1320	S[1024]	-7628.5	357

number	pad name	x	y
1321	S[1025]	-7645.5	217
1322	S[1026]	-7662.5	77
1323	S[1027]	-7679.5	357
1324	S[1028]	-7696.5	217
1325	S[1029]	-7713.5	77
1326	S[1030]	-7730.5	357
1327	S[1031]	-7747.5	217
1328	S[1032]	-7764.5	77
1329	S[1033]	-7781.5	357
1330	S[1034]	-7798.5	217
1331	S[1035]	-7815.5	77
1332	S[1036]	-7832.5	357
1333	S[1037]	-7849.5	217
1334	S[1038]	-7866.5	77
1335	S[1039]	-7883.5	357
1336	S[1040]	-7900.5	217
1337	S[1041]	-7917.5	77
1338	S[1042]	-7934.5	357
1339	S[1043]	-7951.5	217
1340	S[1044]	-7968.5	77
1341	S[1045]	-7985.5	357
1342	S[1046]	-8002.5	217
1343	S[1047]	-8019.5	77
1344	S[1048]	-8036.5	357
1345	S[1049]	-8053.5	217
1346	S[1050]	-8070.5	77
1347	S[1051]	-8087.5	357
1348	S[1052]	-8104.5	217
1349	S[1053]	-8121.5	77
1350	S[1054]	-8138.5	357
1351	S[1055]	-8155.5	217
1352	S[1056]	-8172.5	77
1353	S[1057]	-8189.5	357
1354	S[1058]	-8206.5	217
1355	S[1059]	-8223.5	77
1356	S[1060]	-8240.5	357
1357	S[1061]	-8257.5	217
1358	S[1062]	-8274.5	77
1359	S[1063]	-8291.5	357
1360	S[1064]	-8308.5	217
1361	S[1065]	-8325.5	77
1362	S[1066]	-8342.5	357
1363	S[1067]	-8359.5	217
1364	S[1068]	-8376.5	77
1365	S[1069]	-8393.5	357
1366	S[1070]	-8410.5	217
1367	S[1071]	-8427.5	77
1368	S[1072]	-8444.5	357
1369	S[1073]	-8461.5	217
1370	S[1074]	-8478.5	77
1371	S[1075]	-8495.5	357
1372	S[1076]	-8512.5	217
1373	S[1077]	-8529.5	77
1374	S[1078]	-8546.5	357
1375	S[1079]	-8563.5	217
1376	S[1080]	-8580.5	77
1377	S[1081]	-8597.5	357
1378	S[1082]	-8614.5	217
1379	S[1083]	-8631.5	77
1380	S[1084]	-8648.5	357

number	pad name	x	y
1381	S[1085]	-8665.5	217
1382	S[1086]	-8682.5	77
1383	S[1087]	-8699.5	357
1384	S[1088]	-8716.5	217
1385	S[1089]	-8733.5	77
1386	S[1090]	-8750.5	357
1387	S[1091]	-8767.5	217
1388	S[1092]	-8784.5	77
1389	S[1093]	-8801.5	357
1390	S[1094]	-8818.5	217
1391	S[1095]	-8835.5	77
1392	S[1096]	-8852.5	357
1393	S[1097]	-8869.5	217
1394	S[1098]	-8886.5	77
1395	S[1099]	-8903.5	357
1396	S[1100]	-8920.5	217
1397	S[1101]	-8937.5	77
1398	S[1102]	-8954.5	357
1399	S[1103]	-8971.5	217
1400	S[1104]	-8988.5	77
1401	S[1105]	-9005.5	357
1402	S[1106]	-9022.5	217
1403	S[1107]	-9039.5	77
1404	S[1108]	-9056.5	357
1405	S[1109]	-9073.5	217
1406	S[1110]	-9090.5	77
1407	S[1111]	-9107.5	357
1408	S[1112]	-9124.5	217
1409	S[1113]	-9141.5	77
1410	S[1114]	-9158.5	357
1411	S[1115]	-9175.5	217
1412	S[1116]	-9192.5	77
1413	S[1117]	-9209.5	357
1414	S[1118]	-9226.5	217
1415	S[1119]	-9243.5	77
1416	S[1120]	-9260.5	357
1417	S[1121]	-9277.5	217
1418	S[1122]	-9294.5	77
1419	S[1123]	-9311.5	357
1420	S[1124]	-9328.5	217
1421	S[1125]	-9345.5	77
1422	S[1126]	-9362.5	357
1423	S[1127]	-9379.5	217
1424	S[1128]	-9396.5	77
1425	S[1129]	-9413.5	357
1426	S[1130]	-9430.5	217
1427	S[1131]	-9447.5	77
1428	S[1132]	-9464.5	357
1429	S[1133]	-9481.5	217
1430	S[1134]	-9498.5	77
1431	S[1135]	-9515.5	357
1432	S[1136]	-9532.5	217
1433	S[1137]	-9549.5	77
1434	S[1138]	-9566.5	357
1435	S[1139]	-9583.5	217
1436	S[1140]	-9600.5	77
1437	S[1141]	-9617.5	357
1438	S[1142]	-9634.5	217
1439	S[1143]	-9651.5	77
1440	S[1144]	-9668.5	357

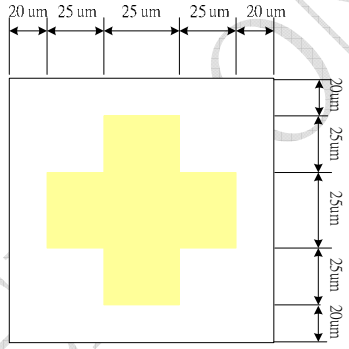
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number	pad name	x	y
1441	S[1145]	-9685.5	217
1442	S[1146]	-9702.5	77
1443	S[1147]	-9719.5	357
1444	S[1148]	-9736.5	217
1445	S[1149]	-9753.5	77
1446	S[1150]	-9770.5	357
1447	S[1151]	-9787.5	217
1448	S[1152]	-9804.5	77
1449	S[1153]	-9821.5	357
1450	S[1154]	-9838.5	217
1451	S[1155]	-9855.5	77
1452	S[1156]	-9872.5	357
1453	S[1157]	-9889.5	217
1454	S[1158]	-9906.5	77
1455	S[1159]	-9923.5	357
1456	S[1160]	-9940.5	217
1457	S[1161]	-9957.5	77
1458	S[1162]	-9974.5	357
1459	S[1163]	-9991.5	217
1460	S[1164]	-10008.5	77
1461	S[1165]	-10025.5	357
1462	S[1166]	-10042.5	217
1463	S[1167]	-10059.5	77
1464	S[1168]	-10076.5	357
1465	S[1169]	-10093.5	217
1466	S[1170]	-10110.5	77
1467	S[1171]	-10127.5	357
1468	S[1172]	-10144.5	217
1469	S[1173]	-10161.5	77
1470	S[1174]	-10178.5	357

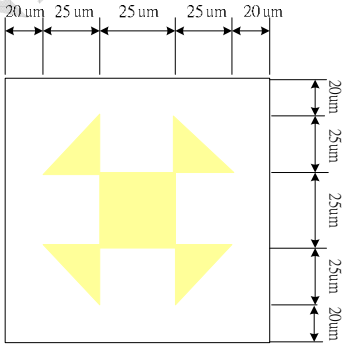
number	pad name	x	y
1471	S[1175]	-10195.5	217
1472	S[1176]	-10212.5	77
1473	S[1177]	-10229.5	357
1474	S[1178]	-10246.5	217
1475	S[1179]	-10263.5	77
1476	S[1180]	-10280.5	357
1477	S[1181]	-10297.5	217
1478	S[1182]	-10314.5	77
1479	S[1183]	-10331.5	357
1480	S[1184]	-10348.5	217
1481	S[1185]	-10365.5	77
1482	S[1186]	-10382.5	357
1483	S[1187]	-10399.5	217
1484	S[1188]	-10416.5	77
1485	S[1189]	-10433.5	357
1486	S[1190]	-10450.5	217
1487	S[1191]	-10467.5	77
1488	S[1192]	-10484.5	357
1489	S[1193]	-10501.5	217
1490	S[1194]	-10518.5	77
1491	S[1195]	-10535.5	357
1492	S[1196]	-10552.5	217
1493	S[1197]	-10569.5	77
1494	S[1198]	-10586.5	357
1495	S[1199]	-10603.5	217
1496	S[1200]	-10620.5	77
1497	SHIELDING[68]	-10664	377
1498	COM1_T	-10714	377
1499	COM1_T	-10764	377
1500	SYNCR	-10814	377

number	pad name	x	y
1501	LDR	-10864	377
1502	POLR	-10914	377
1503	DATAR[0]	-11179	397
1504	DATAR[1]	-11049	357
1505	DATAR[2]	-11179	317
1506	DATAR[3]	-11049	277
1507	DATAR[4]	-11179	237
1508	DATAR[5]	-11049	197
1509	DATAR[6]	-11179	157
1510	DATAR[7]	-11049	117
1511	DATAR[8]	-11179	77
1512	DATAR[9]	-11049	37
1513	DATAR[10]	-11179	-3
1514	DATAR[11]	-11049	-43
1515	DATAR[12]	-11179	-83
1516	DATAR[13]	-11049	-123
1517	DATAR[14]	-11179	-163
1518	DATAR[15]	-11049	-203
1519	DATAR[16]	-11179	-243
1520	DATAR[17]	-11049	-283
1521	DIOR	-11179	-323
1522	DCLKR	-11049	-363

Alignment Mark



Alignment Mark: Left



Alignment Mark: Right

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18. Revision History

Version No.	Date	Page	Description
ILI6123H_0.01	2009/06/15	All	New Build Specification
ILI6123H_0.02	2009/07/22	5	Modified logic operation Voltage Level
ILI6123H_0.03	2009/10/13	5	Modified TCON Function Description
		6	Modified Block Diagram for SCL/DCBM[0], SDA/DCBM[1], DBC/3 and REV(TP5) Function Pin
		8/9	Modified Cascade and Dual-Gate Application Block for CABC Control Pin Name.
		10	Modified Pad Name
		11	Modified SPI CSX/SCL/SDA Pin Description Replaced CFSEL to DBC/3 Function Pin.
		12	Add REV(TP5) Function Pin.
		13	Add DBC/3 for CABC Function Control description Table
		14	Add CSX, CABC_PWM, SCL/DBCM[0], SDA/DBCM[1] wiring resistance
		37	Modified DC Electrical Characteristics
		45	Modified REV (TP5), SCL/DBCM[0], SDA/DBCM[1] & DBC/3 PAD Pin Name.

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